Partitioned gate tunnelling current model considering distributed effect for CMOS devices with ultra-thin (1 nm) gate oxide

C.H. Lin, J.B. Kuo, K.W. Su and S. Liu

The partitioned gate tunnelling current model considering the distributed effect for CMOS devices with an ultra-thin (1 nm) gate oxide is reported. As verified by the experimentally measured data, the partitioned gate tunnelling current model considering the distributed effect provides a better prediction of the total gate, drain and source currents as compared to the BSIM4 model.

Introduction: Gate leakage current due to tunnelling through the gate oxide has become a serious phenomenon for advanced CMOS devices with an ultra-thin gate oxide [1]. The impacts of the gate tunnelling current on the performance of the circuits using nanometre CMOS devices with an ultra-thin gate oxide cannot be neglected [2]. In fact, the gate tunnelling current is distributed along the channel, which makes the gate tunnelling current difficult to model. For good assessment of the influence of the gate tunnelling current, an accurate gate tunnelling current model is required. In this Letter, following a double integral approach as for deriving the partitioned-charge model [3], the partitioned gate tunnelling current model considering the distributed effect is reported. It is shown that, as verified by the experimentally measured data, the partitioned gate tunnelling current model considering the distributed effect provides a better prediction of the total gate, drain and source currents as compared to the BSIM4 model.

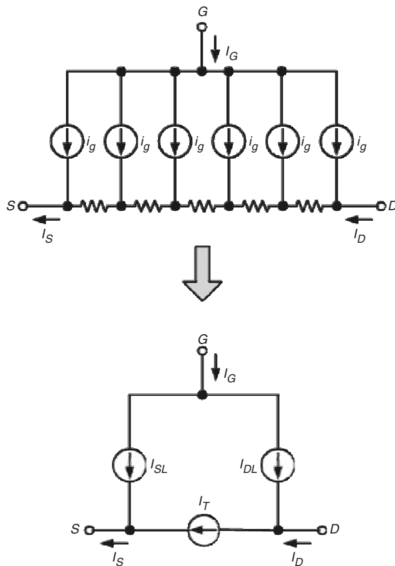

Fig. 1 *Distributed and partitioned gate tunnelling current models*

Partitioned I_G model: Fig. 1*a* shows the distributed gate tunnelling current model. Depending on the location in the lateral channel, the local gate tunnelling current varies. Considering the distributed tunnelling current, the total gate current is divided into the source-side component (I_{SL}) and the drain-side one (I_{DL}) in the partitioned gate tunnelling current model, as shown in Fig. 1*b*. Following the approach for deriving the partitioned charge model for MOS transistors [3], the total gate tunnelling current is expressed as $I_G = W/L \int_0^L \int_0^L J_G(y) dy\, dy$, where $J_G(y) = J_{G0} e^{-B^* V(y)}$ [4] is the local gate tunnelling current density location at location y in the lateral channel, and B^* is a fitting parameter with a nonzero value. From the above equations with the channel drift current, the total gate tunnelling current is:

$$I_G = \frac{J_{G0} WL}{B^*[(V_G - V_T)V_{DS} - (m/2)V_{DS}^2]} \times \left\{ V_G - V_T - \frac{m}{B^*} + e^{-B^* V_{DS}} \left[m V_{DS} - (V_G - V_T) + \frac{m}{B^*} \right] \right\}$$

where J_{G0} is the J_G at $V_{DS} = 0$ V, and m is a fitting parameter with a nonzero value. Similarly, the drain component of the gate tunnelling current is expressed as $I_{DL} = W/L \int_0^L \int_y^L J_G(y) dy\, dy$, which could be simplified using integral by parts as:

$$\begin{aligned} I_{DL} = & \frac{J_{G0} WL}{B^*[(V_G - V_T)V_{DS} - (m/2)V_{DS}^2]^2} \\ & \times \left\{ \frac{1}{B^*}(V_G - V_T)^2 \right. \\ & - \frac{3m}{B^{*2}}(V_G - V_T) + \frac{3m^2}{B^{*3}} + e^{-B^* V_{DS}} \left\{ -\frac{m^2}{2} V_{DS}^3 \right. \\ & + \left[\frac{3m}{2}(V_G - V_T) - \frac{3m^2}{2B^*} \right] V_{DS}^2 \\ & + \left[-(V_G - V_T)^2 + \frac{3m}{B^*}(V_G - V_T) - \frac{3m^2}{B^{*2}} \right] V_{DS} \\ & \left. \left. - \frac{1}{B^*}(V_G - V_T)^2 + \frac{3m}{B^{*2}}(V_G - V_T) - \frac{3m^2}{B^{*3}} \right\} \right\} \end{aligned}$$

and the source component of the gate tunnelling current is:

$$I_{SL} = \frac{W}{L} \int_0^L \int_0^y J_G(y) dy\, dy$$

Thus

$$\begin{aligned} I_{SL} = & \frac{J_{G0} WL}{B^*[(V_G - V_T)V_{DS} - (m/2)V_{DS}^2]^2} \\ & \times \left\{ -\frac{1}{B^*}(V_G - V_T)^2 + \frac{3m}{B^{*2}}(V_G - V_T) - \frac{3m^2}{B^{*3}} \right. \\ & + \left(V_G - V_T - \frac{m}{B^*} \right) \left(V_G - V_T - \frac{m}{2} V_{DS} \right) V_{DS} \\ & + e^{-B^* V_{DS}} \left[\frac{1}{B^*}(V_G - V_T)^2 - \frac{3m}{B^{*2}}(V_G - V_T) \right. \\ & \left. \left. + \frac{3m^2}{B^{*3}} + \frac{3m^2}{B^{*2}} V_{DS} - \frac{2m}{B^*}(V_G - V_T)V_{DS} + \frac{m^2}{B^*} V_{DS}^2 \right] \right\} \end{aligned}$$

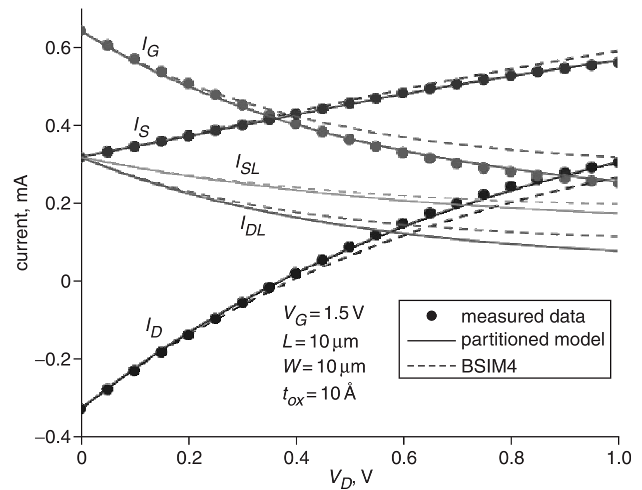

Fig. 2 *Total gate tunnelling current (I_G), partitioned gate tunnelling currents (I_{SL}, I_{DL}), total drain current (I_D), and total source current (I_S) against drain voltage of NMOS device with 1 nm gate oxide and aspect ratio of 10 µm/10 µm biased at gate voltage of 1.5 V, based on experimentally measured data (dots), BSIM4 (dashed lines) and partitioned model result (solid lines)*

Model evaluation and discussion: To assess the effectiveness of this partitioned gate tunnelling current model, the model results have been compared with the experimentally measured data of a test NMOS device with an ultra-thin gate oxide of 1 nm and an aspect ratio of 10 µm/10 µm. Fig. 2 shows the total gate tunnelling current (I_G), the partitioned gate tunnelling currents (I_{SL}, I_{DL}), the total drain current (I_D), and the total source current (I_S) against the drain voltage of the NMOS test device, biased at a gate voltage of 1.5 V, based on the experimentally measured data (dots) and the partitioned model result (solid lines). Also shown in the Figure is the result based on the BSIM4 model (dashed lines) [5]. As shown in the Figure, as verified by the experimentally measured data, the partitioned gate tunnelling current model could provide a more accurate prediction of I_G, I_S, I_D,

I_{SL}, and I_{DL} as compared to the BSIM4 model [5]. In addition, at a higher V_D the effectiveness of the partitioned charge model is higher.

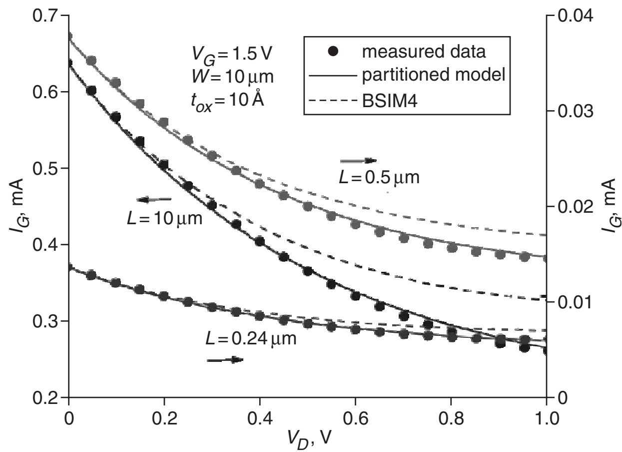

Fig. 3 *Total gate tunnelling current (I_G) against drain voltage of NMOS device with 1 nm gate oxide, channel width of 10 µm, and various channel lengths of 10, 0.5 and 0.24 µm, biased at gate voltage of 1.5 V, based on experimentally measured data (dots), BSIM4 (dashed lines) and partitioned model result (solid lines)*

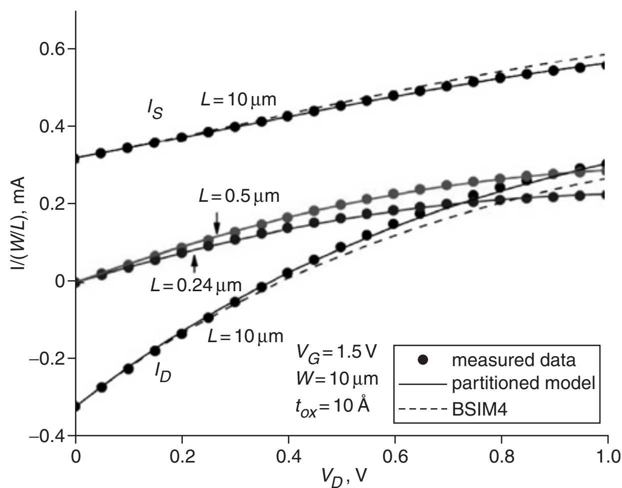

Fig. 4 *Total drain current (I_D) and total source current (I_S) against gate voltage of NMOS device with 1 nm gate oxide, a channel width of 10 µm, and various channel lengths of 10, 0.5 and 0.24 µm, biased at gate voltage of 1.5 V, based on experimentally measured data (dots), BSIM4 (dashed lines) and partitioned gate tunnelling current model result (solid lines)*

Fig. 3 shows the total gate tunnelling current (I_G) and the total source/drain current (I_S/I_D) against the drain voltage of the NMOS test device with a 1 nm gate oxide, a channel width of 10 µm, and various channel lengths of 10, 0.5 and 0.24 µm, biased at a gate voltage of 1.5 V, based on the experimentally measured data (dots), BSIM4 (dashed lines) and the partitioned model result (solid lines). Fig. 4 shows the total drain current (I_D) and the total source current (I_S) against the drain voltage of the NMOS device with a 1 nm gate oxide, a channel width of 10 µm, and various channel lengths of 10, 0.5 and 0.24 µm, biased at a gate voltage of 1.5 V, based on the experimentally measured data (dots), BSIM4 (dashed lines) and the partitioned gate tunnelling current model result (solid lines). As shown in the Figures, the partitioned charge model could provide a better prediction of the current behaviour as verified by the experimentally measured data while compared to the BSIM4 model [5]. Its effectiveness is greater at a higher V_D.

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