CMOS low dropout linear regulator with single Miller capacitor

W.-J. Huang, S.-H. Lu and S.-I. Liu

A 2–5 V 150 mA CMOS low dropout (LDO) linear regulator with a single Miller capacitor of 4 pF is presented. The proposed LDO regulator with a bandgap voltage reference has been fabricated in a 0.35 μm CMOS process and the active chip area is 485 × 586 μm. The maximum output current is 150 mA and the regulated output voltage is 1.8 V.

Introduction: Integrated low dropout (LDO) linear regulators [1–4] are widely used in portable battery-operated electronic devices such as mobile phones and PDAs. The required regulator has to have low static power and low noise, a small active area, a small dip at the output voltage and a fast transient response. To have the appropriate open-loop gain in deep submicron-metre CMOS process, the LDO linear regulator is realised by a multi-stage amplifier which needs complex frequency compensation [3, 5]. In general, there are two or three Miller capacitors in an LDO linear regulator, which is a three-stage amplifier. To guarantee the stability for the heavy and light current loads, tens-pF Miller capacitors have to be used. However, dips of the output voltage and the transient response time of an LDO linear regulator are dependent on the bandwidth. In this Letter, a bandwidth extension method using only a single Miller frequency compensation capacitor of 4 pF is presented and the dips of the output voltage are also reduced.

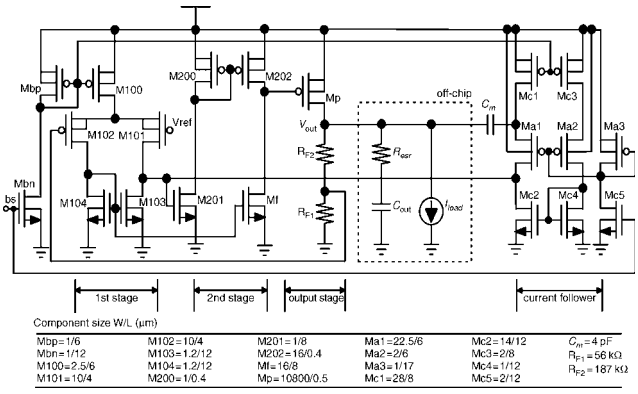

Fig. 1 *Proposed LDO regulator*

Circuit description: Fig. 1 shows the proposed LDO linear regulator (the bandgap voltage reference is not shown). This regulator is composed of three gain stages and a current follower (CF). The CF is composed of Mc1–Mc5 and Ma1–Ma3, which is inserted between the output of the first stage and the Miller compensation capacitor, C_m. This technique is similar to the common-gate frequency compensation method [6]. To analyse the stability of the proposed LDO linear regulator, the loop-gain frequency responses should be investigated. g_{m1}, g_{m2} and g_{mp} are the transconductance of the first, second and the output stage, respectively. g_{ma} is the transconductance of the transistor Ma1. $1/g_{o1}$ and $1/g_{o2}$ are the output parasitic resistance of the first and second stage, respectively. C_{p1} and C_g are the lumped output parasitic capacitance of the first and second stage. R_{esr} is the equivalent series resistance (ESR) of C_{out} and g_{mf} is the transconductance of the transistor Mf. $1/g_{\text{out}}$ ($=R_L//R_{\text{opass}}//(R_{F1}+R_{F2})$) is the equivalent open-loop output resistance of the LDO linear regulator where R_L is the load resistance, R_{opass} is the output resistance of the power transistor, Mp, and R_{F1} and R_{F2} are the feedback resistors.

Assume $C_{\text{out}} \gg (C_m,\ C_a \text{ and } C_g) \gg C_{p1},\ g_{mp} \gg (g_{m1},\ g_{mf},\ g_{m2})$, and $g_{m1}/g_{o1} \gg 1$ and $g_{m2}/g_{o2} \gg 1$. The small-signal transfer function of the LDO linear regulator in the heavy load (I_{load} is large) is given as

$$L_{hl}(s) = \frac{-A_o[1+s(C_m/g_{ma})]}{[1+s(g_{mf}C_{p1}/g_{m2}g_{m1})]} \frac{}{[1+(s/|p_{-3\,\text{dB\_heavy\_load}}|)]} \frac{}{[1+s(C_gC_{p1}/C_mg_{m2}g_{mp}R_{esr})]} \frac{}{+s^2(C_gC_{p1}/g_{m2}g_{mp}g_{ma}R_{esr})]} \quad (1)$$

where $A_o=(R_{F1}/(R_{F1}+R_{F2}))g_{m1}g_{m2}g_{mp}/(g_{o1}g_{o2}g_{\text{out}})$ is the DC loop gain and $p_{-3\,\text{dB\_heavy\_load}}=-g_{o1}g_{o2}g_{\text{out}}/C_mg_{m2}g_{mp}$ is the dominant pole of the LDO linear regulator in the heavy load. The second non-dominant pole is much larger than the first one, which is in the order of MHz. The second-order polynomial in the denominator is decomposed into $[1+s(C_gC_{p1}/C_mg_{m2}g_{mp}R_{esr})][1+s(C_m/g_{ma})]$. Then, (1) is rewritten as

$$L_{hl}(s) \simeq \frac{-A_o[1+s(g_{mf}C_{p1}/g_{m2}g_{m1})]}{[1+(s/|p_{-3\,\text{dB\_heavy\_load}}|)][1+s(C_gC_{p1}/C_mg_{m2}g_{mp}R_{esr})]} \quad (2)$$

Therefore, a smaller Miller compensation capacitor is used to extend the bandwidth in the heavy load.

Two cases are considered for the LDO operating in the light load (I_{load} is small) with small and large ESRs, respectively. As a small ESR is used, the transfer function for the light load is given as

$$\begin{aligned} L_{ll}(s) = {} & \frac{-A_o(1+sC_{\text{out}}R_{esr})[1+s(C_m/g_{ma})]}{[1+s(g_{mf}C_{p1}/g_{m2}g_{m1})]} \\ & \frac{}{\{1+s[(C_mg_{m2}g_{mp}/g_{\text{out}}g_{o1}g_{o2})+(C_{\text{out}}/g_{\text{out}})]\}} \\ & \times\{1+s[[(C_g/C_m)(g_{o1}/g_{o2})+(C_{p1}/C_m)] \\ & \times C_{\text{out}}g_{o2}]/[g_{m2}g_{mp}+(C_{\text{out}}/C_m)g_{o1}g_{o2})] \\ & +s^2[C_{\text{out}}C_gC_{p1}/(C_mg_{m2}g_{mp}+C_{\text{out}}g_{o1}g_{o2})] \\ & +s^3[C_mC_{\text{out}}C_gC_{p1}/g_{ma}(C_mg_{m2}g_{mp}+C_{\text{out}}g_{o1}g_{o2})]\} \end{aligned} \quad (3)$$

From (3), if the second non-dominant pole is apart from the first non-dominant pole, they are given as

$$\begin{aligned} P_{nd1\_ll\_lowESR} &\simeq \frac{g_{m2}g_{mp}+(C_{\text{out}}/C_m)g_{o1}g_{o2}}{[(C_g/C_m)(g_{o1}/g_{o2})+(C_{p1}/C_m)]C_{\text{out}}g_{o2}} \quad \text{and} \\ P_{nd2\_lowESR} &\simeq \frac{g_{o1}}{C_{p1}}+\frac{g_{o2}}{C_g} \end{aligned} \quad (4)$$

However, as C_m is decreased, the dominant pole increases and the first non-dominant pole decreases, and then the phase margin is decreased. Therefore, the minimum Miller compensation capacitor is needed to have an appropriate phase margin in the light load with a small ESR.

If a higher ESR output capacitor is used, the first and second non-dominant poles are given as

$$\begin{aligned} P_{nd1\_ll\_highESR} &\simeq \frac{g_{m2}g_{mp}+(C_{\text{out}}/C_m)g_{o1}g_{o2}}{[(C_g/C_m)(g_{o1}/g_{o2})+(C_{p1}/C_m)} \quad \text{and} \\ & \qquad +(g_{m2}g_{mp}/g_{o2})R_{esr}]C_{\text{out}}g_{o2} \\ P_{nd2\_ll\_highESR} &\simeq \frac{g_{o1}}{C_{p1}}+\frac{g_{o2}}{C_g}+\frac{C_mg_{m2}g_{mp}R_{esr}}{C_{p1}C_g} \end{aligned} \quad (5)$$

The first non-dominant pole is slightly decreased to a lower frequency and the second non-dominant pole is slightly increased to a higher frequency. Thus the complex poles are avoided for the light load with a large ESR, meaning the LDO regulator for the light load has a large ESR. In general, only a Miller capacitor of 4 pF is used to achieve stability for all the above analyses in our design.

Experimental results: This LDO regulator has been fabricated in a 0.35 μm CMOS process. The die photo is shown in Fig. 2; the active area is 485 × 586 μm^2. The maximum output current is 150 mA with a dropout voltage of 220 mV. R_{F1} and R_{F2} are 56 and 187 kΩ, respectively. The proposed LDO regulator with 1.8 V output operates from 2 to 5 V and its static power is 0.265 mW with 53 μA quiescent current (where the bandgap voltage reference consumes 26 μA) in a 5 V supply voltage. The measured line regulations at the load current $I_{load}=0$ and $I_{load}=150$ mA are 0.045 and 0.143%/V, respectively. The measured load regulation is 92.8 ppm/mA at 3.3 V. Fig. 3 shows the measured transient responses of the LDO regulator at 3.3 V and the load current switching from 0 and 150 mA for the output capacitor of (Fig. 3*a*) $C_{\text{out}}=10$ μF with ESR = 0.8 Ω, (Fig. 3*b*) $C_{\text{out}}=1$ μF with ESR = 0.3 Ω and (Fig. 3*c*) $C_{\text{out}}=1$ μF with ESR = 1 Ω, respectively. The experimental results show that the proposed LDO can recover to the preset output voltage within 3.2 μs under $C_{\text{out}}=1$ μF with ESR = 0.3 Ω. In addition, the dips of the output voltage are reduced to 130 mV owing to the wide bandwidth of the proposed LDO linear regulator.

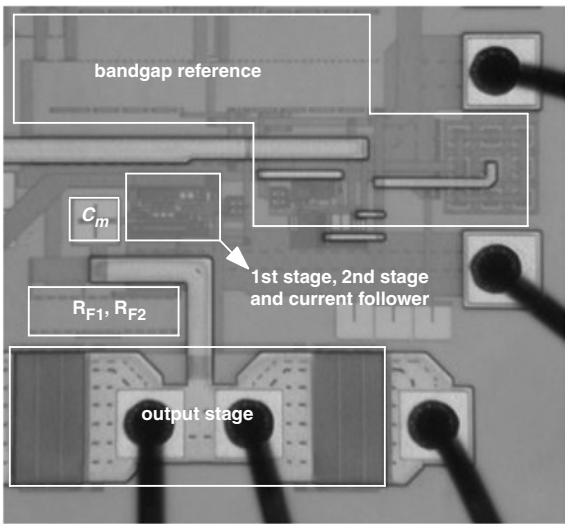

Fig. 2 *Die photo*

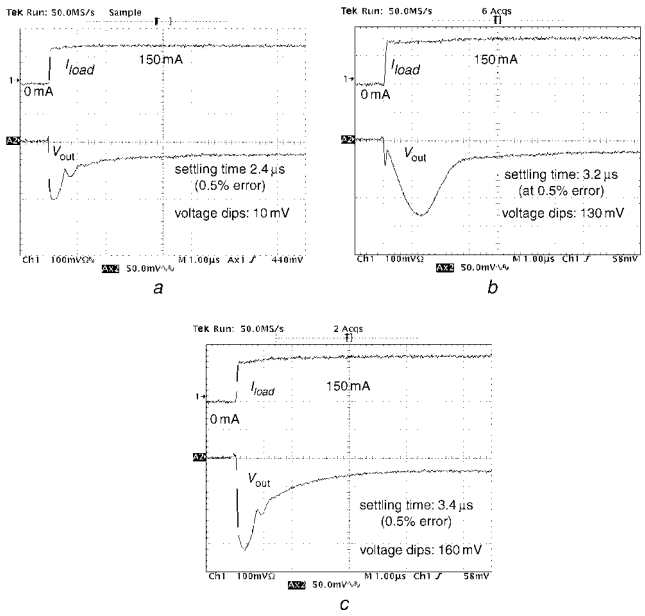

Fig. 3 *Transient response of LDO regulator for $C_{out} = 10$ µF and ESR = 0.8 Ω (Fig. 3a), $C_{out} = 1$ µF and ESR = 0.3 Ω (Fig. 3b), $C_{out} = 1$ µF and ESR = 1 Ω (Fig. 3c)*

V_{out}: 50 mV/div., 1 µs/div.

Conclusion: A CMOS LDO linear regulator with a single Miller capacitor is presented. Experimental results confirmed that the dips and peaks of the output voltage are reduced simultaneously owing to the larger bandwidth. Moreover, the settling time is also reduced significantly.

Acknowledgment: The authors thank the National Chip Implementation Center (CIC), Hsinchu, Taiwan, for chip implementation.

20 November 2005
Electronics Letters online no: 20064062
doi: 10.1049/el:20064062

W.-J. Huang, S.-H. Lu and S.-I. Liu (*Graduate Institute of Electronics Engineering and Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan 10617, Republic of China*)

E-mail: lsi@cc.ee.ntu.edu.tw

References

1 Rincon-Mora, G.A., and Allen, P.E.: 'A low-voltage, low quiescent current, low drop-out regulator', *IEEE J. Solid-State Circuits*, 1998, **33**, pp. 36–44
2 Rincon-Mora, G.A., and Allen, P.E.: 'Optimized frequency-shaping circuit topologies for LDO's', *IEEE Trans. Circuits Syst. II*, 1998, **45**, pp. 703–708
3 Leung, K.N., and Mok, P.K.T.: 'A capacitor-free CMOS low-dropout regulator with damping-factor-control frequency compensation', *IEEE J. Solid-State Circuits*, 2003, **38**, pp. 1691–1702
4 Hazucha, P., Karnik, Y., Bloechel, B., Parsons, C., Finan, D., and Borkar, S.: 'An area-efficient integrated linear regulator with ultra-fast load regulation'. Symp. on VLSI Circuits Dig. Tech. Pprs, June 2004, pp. 218–221
5 Lee, H., and Mok, P.K.T.: 'Advances in active-feedback frequency compensation with power optimization and transient improvement', *IEEE Trans. Circuits Syst. I*, 2004, **51**, pp. 1690–1696
6 Ahuja, B.K.: 'An improved frequency compensation technique for CMOS operational amplifiers', *IEEE J. Solid-State Circuits*, 1983, **18**, pp. 629–633