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A Low-Cost Jitter Measurement Technique for BIST Applications*

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Abstract. In this paper, we present a BIST technique that measures the RMS value of a Gaussian distribution period jitter. In the proposed approach, the signal under test is delayed by two different delay values and the probabilities it leads the two delayed signals are measured. The RMS jitter can then be derived from the probabilities and the delay values. Behavior and circuit simulations are performed to validate the proposed technique and analyze the design tradeoffs, and preliminary measurement results on FPGA are also presented.

Keywords: random jitter, built-in self-test, jitter measurement

1. Introduction

Quality of the clock signal plays an import role in modern high-speed systems because most activities are synchronized to the clock. However, in the existence of jitter, the clock edges may deviate from their ideal positions. To tolerate this, one has to lengthen the clock period, which degrades the system performance. As the clock frequency keeps growing, the clock jitter becomes a severe problem because it can easily consume a large portion of the already tight jitter tolerance budget.

Measuring high-speed clock jitters is a difficult task. It usually relies on expensive ATE (automatic test equipment) and can easily consume long test time. Furthermore, the situation is getting worse as the trend of system integration onto a single chip continues. First, access to deeply embedded signals is not always possible. Secondly, the trend of replacing parallel ports with high-speed serial ports posts a stringent challenge on the ATE because the system under test may possess tens or even hundreds of high-speed serial I/O channels.

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One promising solution to alleviating these problems is built-in self-test (BIST). Since on-chip BIST circuitry can be made close to the signal sources under test, accessing embedded signals becomes much easier and not limited by the bandwidth of the I/O pins. Also, the BIST and functional circuits are manufactured using the same process technology, which keeps them at the same speed and performance level. The main concern of BIST is the incurred area/performance overhead and the achievable test accuracy.

Many research efforts have been devoted to jitter testing. In [9], the authors employ a variable delay line to record the 15.9 and 84.1% points of the jitter's cumulative distribution function (CDF) curve from which the RMS jitter value can be derived. (The jitter is assumed to be a Gaussian random variable.) The main advantage is that the BIST circuit is fully digital, and thus can be more easily integrated into the design flow. The technique reported in [4] is similar to [9]; however, only two points along the CDF curve are sampled to derived the RMS jitter.

High-resolution time-to-digital techniques can also be used for jitter measurement. For example, the methods reported in [3] and [11] achieve high-resolution jitter

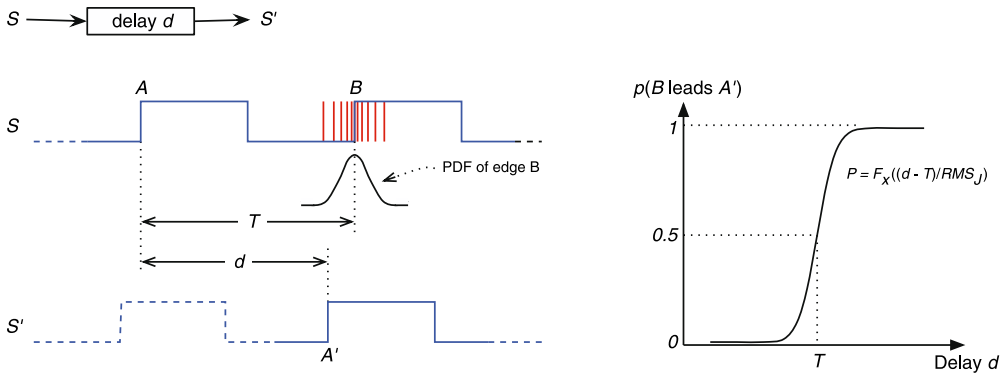

Fig. 1. The basic idea.

measurement with a vernier delay line. The limitation is the large hardware overhead and the stringent delay line linearity requirement. The technique reported in [1] intends to solve the linearity problem by using a component-invariant vernier delay line. The main limitation is the associated long test time. To resolve this problem, the authors propose a test time reduction method at the expense of more hardware. In [10], the authors solve the delay line linearity problem by characterizing the non-linearity and incorporating this information during the analysis phase.

In [12] and [13], an analytic signal method to extract peak-to-peak and RMS jitter is proposed and validated with commercial processors. The technique can reduce the test time significantly, but is not suitable for BIST applications. The method is further extended in [14]. Application of the Morlet wavelet transform to detect the phase and frequency variations of radio-frequency signals are reported in [8]. However, the technique is more suitable for ATE.

In [2], the authors propose to use the signal under test as the clock signal to an ADC which samples a sinusoidal signal. This way, the jitter information can be extracted from the ADC outputs.

In this paper, we present a BIST technique that measures the RMS value of a Gaussian distribution period jitter. In the proposed approach, the signal under test is delayed by two different delays and the probabilities that the signal under test leads the two delayed versions are measured. The RMS jitter can then be derived from the probabilities and the delay values. The proposed jitter measurement circuitry is quite simple. It utilizes a two-tap delay line and a phase comparator to extract and digitize the jitter information, and relies on digital resources to record the probabilities and to perform post-analysis.

The main advantages of the proposed period jitter measurement technique include:

1. The employed variable delay line is only two-valued; therefore, there is no linearity requirement on the variable delay line.
2. We only need to know the difference between instead of the actual values of the two delays, which is more feasible in a BIST environment.

One of the disadvantages, however, is the required post-processing which involves solving the inverse Gaussian CDF. To conquer this problem, we propose to store an inverse CDF lookup table in either the chip-under-test, if there are sufficient digital resources, or the ATE. Behavior simulations are performed to analyze the non-ideal factors, and the circuit simulations show promising results. Preliminary measurement results on an commercial FPGA platform are also presented to validate the proposed technique.

This paper is organized as follows. In Section 2, we introduce the proposed technique. In Section 3, practical design issues are discussed. The circuit simulation and FPGA measurement results are shown in Section 4. Finally, we conclude this paper in Section 5.

2. The Proposed Technique

Assuming that the period jitter associated with the signal under test is a zero-mean Gaussian random variable, the objective of the proposed technique is to derive the period jitter's RMS value.

In the following discussion, for convenience, the term "jitter'' corresponds to "period jitter,'' and below is a list of notations used throughout this paper.

$F_X(x)$: The normalized Gaussian CDF.
S, S': S is the signal under test, and S' is S delayed by d_1 or d_2.
T: The ideal period of S.
d_1, d_2, Δd: $d_1$and d_2 are the two delay values associated with the two-tap variable delay line, and $\Delta d = |d_1 - d_2|$.
p_1, p_2: $p_1$and p_2 are the probabilities that S leads S' when the delay line value is d_1 and d_2, respectively.
x_1, x_2, Δx: $x_1 = F_X^{-1}(p_1)$, $x_2 = F_X^{-1}(p_2)$, and $\Delta x = |x_1 - x_2|$.

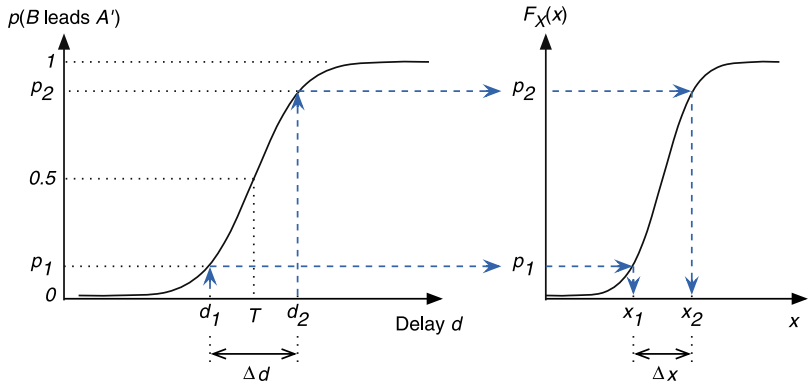

Fig. 2. The proposed method.

J, RMS_J: J denotes the period jitter associated with S, and RMS_J is the RMS value of J. Under the assumption that J is zero-mean, RMS_J equals J's standard deviation.

2.1. The Basic Idea

The basic idea of our approach is depicted in Fig. 1. On the left hand side of Fig. 1, S is the signal under test of which the ideal period is T, S' is a delayed version of S by d, A and B are two consecutive rising edges of S, and A' is the rising edge of S' corresponding to A. Since S is with Gaussian period jitter, the position of B relative to A is also a Gaussian distribution centered at T.

Now, let's consider the phase relationship between B and A'. Obviously, if S is jitter-free, the relationship between B and A' is constant and depends on d and T—B will lead/coincide with/lag A' if d is greater than/equal to/less than T. However, in the existence of jitter, the time duration between A and B, and accordingly the phase relationship (lead or lag) between B and A', will depend on the period jitter associated with that cycle and is no longer constant. In fact, the probability p that B leads A' is

$$p = F_X\left(\frac{d-T}{RMS_J}\right) \tag{1}$$

and is shown on the right hand side of Fig. 1. One can see that $p = 0.5$ when $d = T$, and increases/decreases as one increases/decreases d.

At first sight, it seems that RMS_J can be derived once p and d are known, i.e.,

$$RMS_J = \frac{d-T}{F_X^{-1}(p)} \tag{2}$$

However, this intuitive approach is not suitable for BIST applications because it is difficult to measure d accurately with on-chip resources.

To avoid measuring the actual delay value, we propose to delay S by two different delays, d_1 and d_2, and measure the corresponding probabilities, p_1 and p_2, that B leads A' (Fig. 2). Rearranging Eq. (2) for d_1 and d_2, one has

$$d_1 - T = RMS_J \cdot F_X^{-1}(p_1) \tag{3}$$

$$d_2 - T = RMS_J \cdot F_X^{-1}(p_2) \tag{4}$$

From Eqs. (3) and (4), RMS_J can be derived:

$$RMS_J = \frac{d_1 - d_2}{F_X^{-1}(p_1) - F_X^{-1}(p_2)} \tag{5}$$

$$= \frac{d_1 - d_2}{x_1 - x_2} \tag{6}$$

$$= \frac{\Delta d}{\Delta x} \tag{7}$$

Note that in Eq. (7), Δd, instead of the actual values of d_1 and d_2, is employed to solve RMS_J. As will be shown later, this is a more feasible solution when only on-chip resources are available.

2.2. Solving the Inverse Gaussian CDF

The main difficulty of deriving RMS_J using Eq. (7) is how to solve F_X^{-1} efficiently and accurately. Clearly, solving $x_i = F_X^{-1}(p_i)$ using either F_X or the approximation function (due to Brjesson and Sundberg, 1979 [7] and with a maximum absolute error of 0.27% for any $x \geq 0$) is too computation intensive to be a practical solution. Therefore, in our approach, we propose to use a pre-computed lookup table stored on-chip or in the external ATE to realize the inverse CDF function. We will discuss trade-offs between the table size and the resulting accuracy in later discussions.

In [9], the authors also derive the RMS jitter value from the CDF curve. Compared to their method, ours is simper

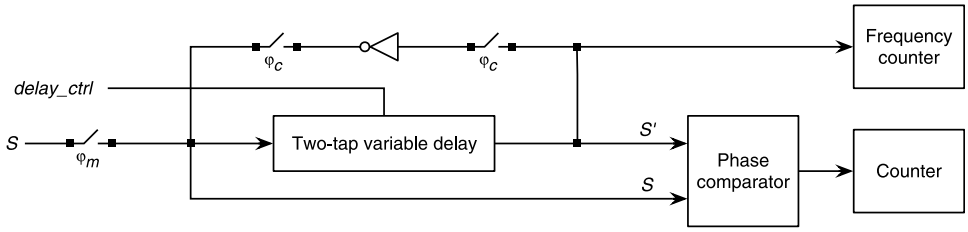

Fig. 3. The proposed BIST circuitry.

in that only two points along the CDF curve are needed to derive the RMS value. However, our method requires higher post-processing efforts, i.e., solving the inverse CDF.

2.3. The BIST Architecture

The proposed BIST architecture is shown in Fig. 3. The main components are:

Two-tap variable delay. The variable delay has two different delay values, d_1 and d_2, controlled by the signal *delay_ctrl*.

Phase comparator. The phase comparator determines whether the rising edge of S leads or lags that of S'. Its output is high if S leads S', and low otherwise.

Inverter. In the calibration mode, the inverter together with the variable delay forms an oscillator whose oscillation period is measured by the frequency counter.

Counter. During the measurement mode, the counter keeps track of the number of times S leads S'.

Frequency counter. One possible implementation of the frequency is shown in Fig. 4 where f and f_{ref} are the unknown and the reference frequencies, respectively. The unknown frequency can be expressed by

$$f = \frac{count \cdot Y \cdot f_{ref}}{Z}$$

Control switches. The control switches are properly opened or closed to set the BIST circuitry to different operation modes.

2.3.1. BIST Circuitry Operations. The BIST circuitry has two operation modes—the calibration mode and the measurement mode.

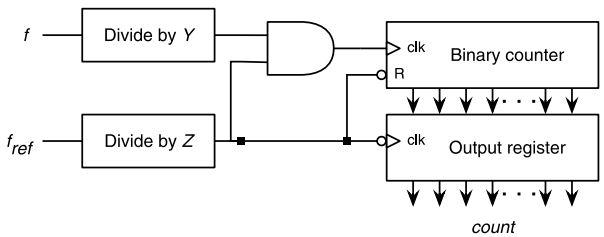

Fig. 4. The frequency counter.

Calibration mode. In the calibration mode, ϕ_m is low and ϕ_c is high. This way, the inverter together with the variable delay forms a ring oscillator. Let the inverter delay be d_{inv}. The *delay_ctrl* signal is set to low and high to measure $(d_1 + d_{inv})$ and $(d_2 + d_{inv})$, respectively.

Measurement mode. In the measurement mode, ϕ_m is high and ϕ_c is low. N phase comparisons between S and S' are performed for low and high *delay_ctrl* values, and the number of times S leads S', denoted by n_1 and n_2, respectively, are counted and stored for later analysis.

2.3.2. The Measurement Flow. The jitter measurement flow consists of the two BIST modes and a following analysis phase. In the analysis phase, Δd, p_1, and p_2 are first derived, i.e.,

$$\begin{aligned} \Delta d &= (d_1 + d_{inv}) - (d_2 + d_{inv}) \\ p_i &= \tfrac{n_i}{N} \end{aligned}$$

x_1 and x_2 are then derived using the pre-computed inverse CDF table. Finally, RMS_J is computed using Eq. (7).

2.3.3. An Example. In this section, we will use an example to illustrate the proposed technique. The signal and BIST circuitry specifications are as follows:

- The ideal period of S is T = 1 ns.
- d_1 and d_2 are *designed* to be 990 and 1,010 ps, respectively. We will discuss how to determine the target values of d_1 and d_2 later.
- $N = 5,000$ phase comparisons are made for each delay value.

In the calibration phase, the two delays are measured:

$$\begin{aligned} d_1 + d_{inv} &= 1,351\text{ps} \\ d_2 + d_{inv} &= 1,361\text{ps} \end{aligned}$$

Then, in the measurement phase, n_1 and n_2 are counted:

$$\begin{aligned} n_1 &= 3,000 \\ n_2 &= 3,200 \end{aligned}$$

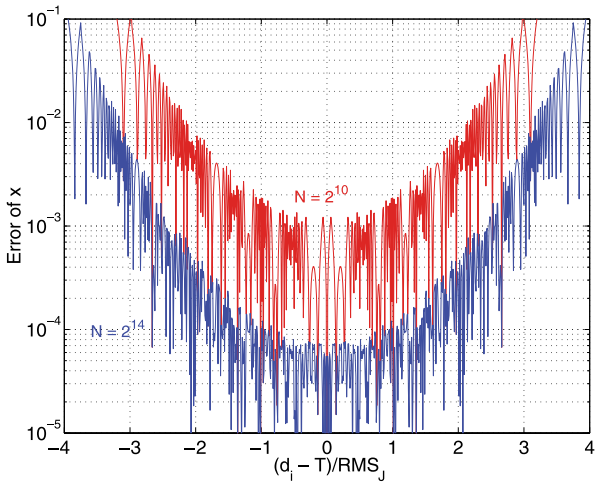

Fig. 5. Quantization error.

Finally, in the analysis phase, $p_1 = 0.6$ and $p_2 = 0.62$ are derived, and x_1 and x_2 are looked up:

$$\begin{aligned} x_1 &= 0.2513 \\ x_2 &= 0.3559 \end{aligned}$$

and we have

$$\begin{aligned} RMS_J &= \frac{|1,351 - 1,361|}{|0.2513 - 0.3559|}\,\text{ps} \\ &= 95.6ps \end{aligned}$$

3. Design Considerations

In this section, we will analyze the sources of errors and perform behavior simulations to determine the key parameters of the BIST circuitry, i.e., $d_1$and d_2. In addition, a calibration technique to remove the BIST circuitry induced jitter from the measurement results is introduced.

3.1. Error Analysis and Simulation

From Eq. (7), the overall jitter measurement accuracy is limited by errors associated with Δd and Δx. Thus, the main sources of errors include

- The finite sample size.
- The numerical error associated with the inverse CDF lookup table.
- The measurement error of Δd.
- The jitter associated with the BIST circuitry itself.

In the following, we will analyze these factors, and discuss their impacts on the BIST circuitry design parameters.

3.1.1. The Finite Sample Size. Ideally, the number of phase comparisons, N, should be as large as possible so that the sample distribution is close enough to the theoretical one. In reality, N is nevertheless limited by the available test time, which causes the sampled CDF to deviate from the ideal one. In our method, this deviation results in errors in p_i's, and eventually in x_i's. The incurred error can be reduced by using the largest possible N.

Another effect of the finite N on p_i's is the quantization error. As $p_i = n_i/N, 0 \le n_i \le N$, p_i can assume only the $N+1$ discrete values, i.e., $\left\{\frac{0}{N}, \frac{1}{N}, \frac{2}{N}, \cdots, 1\right\}$; thus, the quantization error associated with the measured p_i's is bounded by $\frac{1}{N}$. The errors of p_is are later translated to errors in x_i's. In Fig. 5, the x-axis is $(d_i - T)/RMS_J$, the y-axis is the resulting errors in x_i, and the two curves correspond to $N = 2^{10}$ (top) and $N = 2^{14}$ (bottom), respectively. The bathtub-like curves are due to the very steep tails in both directions (positive and negative) of the inverse Gaussian CDF function, and suggest that $|d_i - T|$ should be within a few RMS_J's of T so that the errors of x_i,s are acceptable. Take $N = 2^{10}$ for example, if d_i's are selected such that

$$|d_i - T| \le 2 \cdot RMS_J \tag{8}$$

then the induced error in Δwill be bounded by 2%. Clearly, the errors can be effectively reduced by increasing N. It should be noticed that as Δx is the divider of Eq. (7), while constraining d_i's reduces the quantization error, d_i's should be kept far enough so that the resulting Δx is sufficiently large.

3.1.2. The Inverse CDF Lookup Table. To solve for F_X^{-1}, it is suggested that a pre-computed lookup table be stored in the chip-under-test or the ATE. In either environment, it is crucial to reduce the lookup table size.

Since p_i can assume only $N + 1$discrete values, the lookup table will store at most $N + 1$entries. Besides, after examining the inverse Gaussian CDF curve, one can further reduce the table size in the following ways:

- Since F_X^{-1} is symmetric about $(0.5, 0)$, only half of the curve needs to be stored.
- The steep tails of the inverse CDF curve can be truncated because it suffers the quantization-induced errors discussed in Sec. 3.1.1 and should not be used.
- The entries can be stored as integers in lieu of floating point numbers.

Note that, at the cost of slightly more complex lookup process, the first two methods reduce the table size without incurring errors. The last approach, however, will introduce quantization error. Assuming that k-bit unsigned integers are used and the maximum entry value,

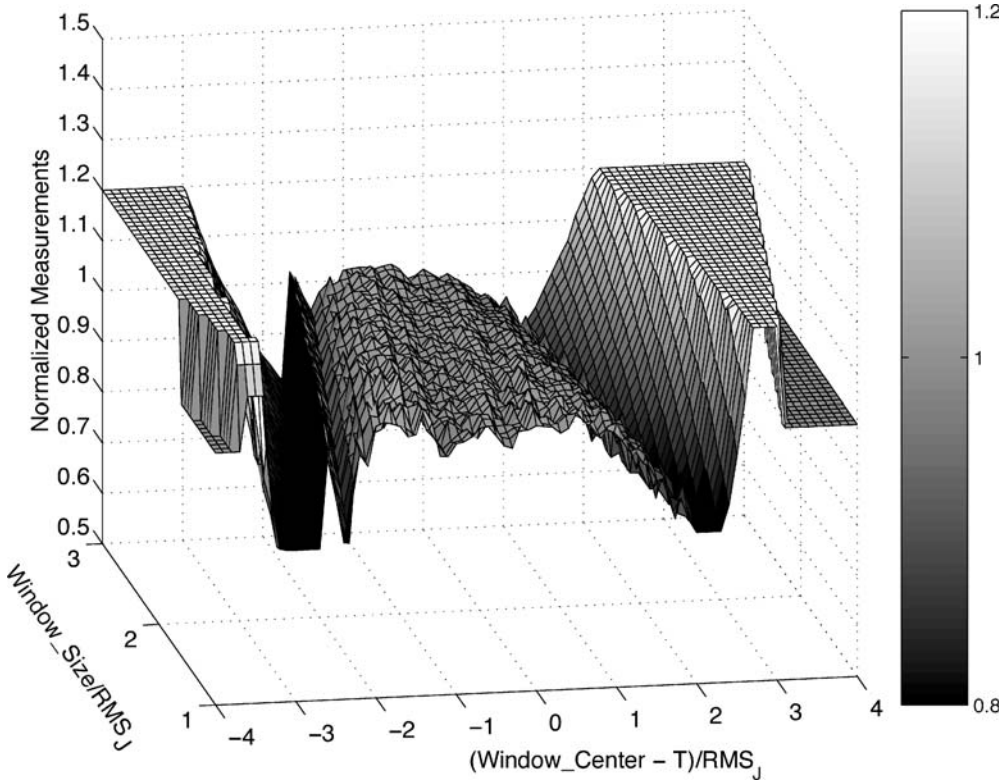

Fig. 6. Behavior simulation for $N = 2^{10}$.

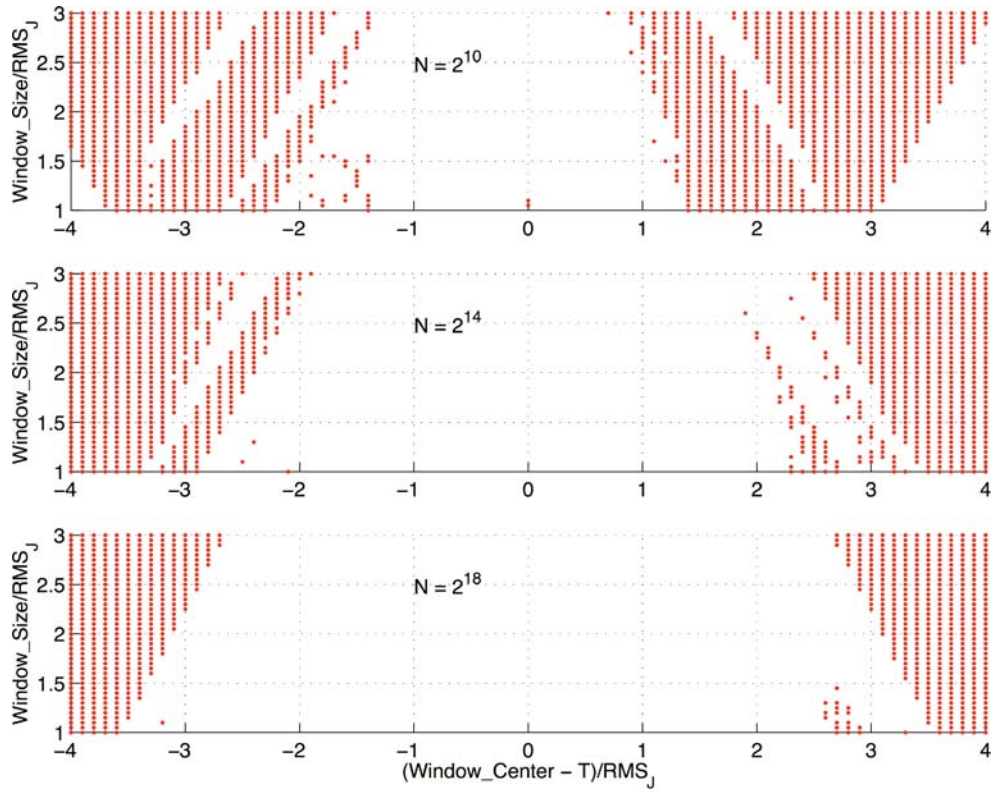

Fig. 7. Determining the d_i values.

$2^k - 1$, corresponds to $x_i = M$, then the induced error of x_i by this table will be bounded by $M \times 2^{-k}$. As an example, suppose $N = 2^{16}$, $M = 6$ (well suited in most cases as it corresponds to 6σ), and $k = 10$, the table size will be 32K by 10-bit words and the maximum error is 0.0078.

3.1.3. The Measurement Error of Δd. From Eq. (7), the error of RMS_J is proportional to that of Δd. Thus, one should increase the frequency counting duration to enhance the accuracy.

3.1.4. Behavior Simulation. For convenience, we define *window_center* and *window_size* as:

$$\begin{aligned} window\_center &= \frac{d_1 + d_2}{2} \\ window\_size &= |d_1 - d_2| \end{aligned}$$

A behavior model of the proposed BIST circuitry is constructed to evaluate the effect of the limited sample size, and the measurement results for $N = 2^{10}$ are shown in Fig. 6. In Fig. 6, the x and y axes correspond to $(window\_center - T)/RMS_J$ and $window\_size/RMS_J$, respectively, and the z axis is the measurement results normalized by RMS_J For ease of visualization, results greater than 1.2 or less than 0.8 are clipped. Figure 6 shows that the measurement result is more stable when the window center is around T, and the measurement errors increase dramatically after the window center moves outside the stable region. Note that the width of the stable region decreases with growing window size.

To determine the design values of d_i's we set the acceptable measurement error to be $0.05 \cdot RMS_J$. (In practice, the threshold is determined by the designer or the test engineer according to the applications and test requirements.) The results are shown in Fig. 7 for N equals 2^{10}, 2^{14}, and 2^{18}. In Fig. 7, each dot corresponds to a (d_1, d_2) combination that doesn't meet the accuracy requirement. From Fig. 7, the pass region is approximately a trapezoid symmetric about zero which corresponds to a window center of T. The pass region decreases as the window size multiplies because one or both d_i's are pushed toward the steep tails of the inverse Gaussian CDF curve where the error caused by the limited sample size is considerably amplified.

Based on Fig. 7, a good choice of the window center and size is at the center of the pass region, i.e., $window\_center = T$ and $window\_size = 2 \cdot RMS_J$, so that the resulting BIST circuitry is more tolerant from process variations. The selected window center and size correspond to

$$d_1 = T + RMS_J \tag{9}$$

$$d_2 = T - RMS_J \tag{10}$$

Equations (9) and (10) look odd because they both contain the term RMS_J that is to be measured! In practice, one can substitute RMS_J in the two equations with the specified pass/fail threshold. For example, for a 1 GHz signal, if the pass/fail threshold is 40 ps, the two-tap variable delay line should be designed to have delay values of 960 and 1,040 ps, respectively.

In reality, RMS_J differs from the pass/fail threshold. When RMS_J increases/decreases, the design point will move downwards/upwards in Fig. 7. If only the difference is such that the design parameters are within the pass region, the measurement error will still be acceptable.

3.2. The BIST Circuit Non-Idealities

In addition to the numerical errors, the BIST circuitry non-idealities such as device noise and bandwidth limitation also result in jitter measurement errors. In the following, the delay line and phase comparator induced jitter measurement errors will be discussed, and a jitter calibration method is proposed.

3.2.1. The Delay Line Induced Errors. Due to the inevitable device noise, the delay line introduces jitter to the S' signal that passes through it. Due to the circuit noise nature, the delay line induced jitter is modeled as a Gaussian distribution random variable, and its effect on the jitter measurement results can be removed through calibration.

Another effect of the delay line on $S'$is *duty cycle distortion*. Because of the non-symmetry between the charging and discharging paths of the delay line elements, the duty cycles of S' may differ from that of S, which leads to a *constant* offset of the transition edges of S'. The effect of the delay line induced duty cycle distortion can be modeled as the variable delay line offset which, according to Eq. (7), does not affect the measurement results.

3.2.2. The Comparator Induced Errors. The possible error sources associated with the phase comparator include comparator offset, comparator induced jitter, and comparator metastability.

Due to mismatch of its differential input stage, the phase comparator exhibits input offset. Like the delay line induced duty cycle distortion, the input offset can be modeled as the delay line offset and does not affect the measurement results.

The general operation principle of a phase comparator is to convert the phase difference to a voltage difference, and then pull the voltage difference to logic levels, called *regeneration*. Clearly, the regeneration process suffers comparator circuit noise—in the worst case, the polarity of the developed voltage difference is altered and the phase comparison result becomes incorrect. From [5], the noise effect during the regeneration process can be

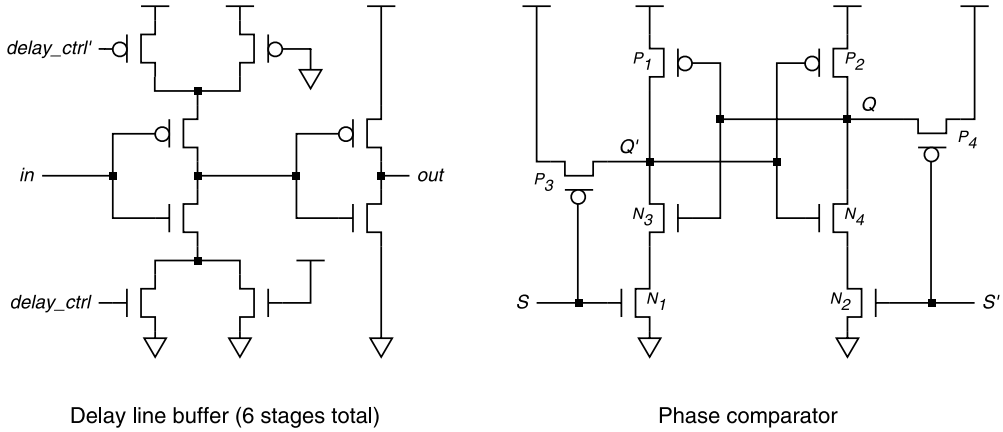

Fig. 8. The two-tap delay line and the phase comparator.

modeled as comparator induced jitters at its inputs which, similar to delay line induced jitter, can be removed via calibration.

In addition to circuit noise, the phase comparator output becomes unpredictable if the input phase difference is so small that its outputs fail to reach logic levels within the given regeneration time window, which is called *metastability*. Since the metastability probability can be effectively reduced by lengthening the regeneration time [6], one simple way to reduce the metastability probability is to divide the signal under test in advance. Note that the RMS jitter value will be scaled by the square root of the division ratio. The divider induced jitter will become part of the measurement errors and can be removed via calibration.

3.2.3. BIST Jitter Calibration. Assume that the overall BIST induced jitter, denoted by RMS_{BIST}, is Gaussian, the measured jitter can be expressed by

$$RMS_{measured} = \sqrt{RMS_J^2 + RMS_{BIST}^2} \qquad (11)$$

RMS_{BIST} if known, can be utilized to calibrate the measurement results. To derive RMS_{BIST}, one may use the BIST circuitry to test a signal of which the jitter is Gaussian and characterized in advance. Let the RMS jitter value of the calibration signal be RMS_{cal}, and the measured jitter value be $RMS_{BIST+cal}$. The RMS jitter associated with the BIST circuitry is then

$$RMS_{BIST} = \sqrt{RMS_{BIST+cal}^2 - RMS_{cal}^2} \qquad (12)$$

Once RMS_{BIST} is available, one may use Eq. (11) to calibrate the measurement results. Although the calibration process will add to the total test time and the ATE cost, if the number of signal under tests is sufficiently large, the incurred calibration overhead will be justified.

4. Implementation and Simulation Results

In this section, we will show the BIST circuitry implementation, circuit simulation results, and hardware validation results.

4.1. BIST Circuitry Implementation

As shown in Fig. 3, the only analog components of the proposed BIST circuitry are the two-tap variable delay and the phase comparator. In our design, the two-tap delay line consists of six buffers each of which possesses two delay values controlled by *delay_ctrl* (left hand side of Fig. 8). The circuit schematic of the phase comparator is illustrated on the right hand side of Fig. 8. The operation of the phase comparator consists of three phases:

Reset. When both S and S' are low, both Q and Q' are charged to V_{DD}.

Compare. As the signals rise, Q and Q' will be discharged by MOSFET's N_2 and N_1, respectively. If S leads S', the voltage at Q will be greater than that at Q', and vice versa.

Latch. When both signals are high, the voltage difference between Q and Q' will be pulled apart to be logic outputs.

4.2. Circuit Simulation Results

To validate the proposed technique, Spice simulations are performed with the following setup:

- T = 1 ns.
- The jitter pass/fail threshold is 40 ps.
- $N = 1,000$.

Based on the specification, the BIST circuitry design parameter is $(d_1, d_2) = (960, 1040)$ ps.

In the calibration mode, the measurement results are

$$(d_1 + d_{inv}) = 1,152 \text{ ps} \quad (13)$$

$$(d_2 + d_{inv}) = 1,230 \text{ ps} \quad (14)$$

Thus, we have Δd = 78.7 ps which is quite close to the design target of 80 ps.

The simulation results for different RMS jitter values are shown in Table 1. In Table 1, the first column lists the injected RMS jitter values, the second and third columns are n_1 and n_2, respectively, the fourth column is $\Delta x = (x_1 - x_2)$, and the last two columns are the absolute and relative errors. From the n_1 and n_2 values, we can see that d_1 and d_2 are not symmetric about 1,000 ps. The RMS jitter measurement errors are within 5% for 40–60 ps RMS jitter; however, the errors grow as the difference between RMS_J and the pass/fail threshold increases.

4.3. Hardware Validation Results

The proposed technique is realized on the Altera Straix^{TM} FPGA for preliminary hardware validation. The phase comparator is realized using a D type flip-flop and the variable delay line is realized with two fixed delay lines. The frequency of the signal under test is 100 MHz.

Using the oscillation approach, the two delay line values are measured to be $d_1 = 11.12$ and $d_2 = 11.55$ ns, respectively. The delay value difference is thus $\Delta d = 430$ ps. Table 2 shows the measurement results. In Table 2, the first column lists the actual RMS jitter values ranging from 130 to 670 ps. (Tektronix AWG-520 is utilized to generate the jittery signal, and Tektronix DSO 7404 to measure the jitter RMS for reference.) The second column is the RMS jitter measured by the proposed technique. In column three, the relative measurement errors are shown. It can be seen that the measurement error is less than 10% when the actual jitter value is from 280 to 490 ps which agrees with our analysis result that Δd (430 ps) should be about twice the RMS jitter value. After examining the DSO obtained jitter histograms, the negative measurement errors should be caused by the non-Gaussian jitter distributions produced by the test setup.

Table 1. Simulation results.

					Error	
RMS jitter (ps)	n_1	n_2	Δx	Result (ps)	ps	%
30	99	866	2.395	32.8	2.8	9.5
40	154	813	1.9084	41.2	1.2	3.1
50	204	775	1.5828	49.7	0.2	0.5
60	239	712	1.2688	62.0	2.0	3.3
70	293	684	1.0237	76.8	6.8	9.8

Table 2. FPGA measurement results.

Actual (ps)	Measured (ps)	Error (%)
138.70	166.76	20.23
162.50	189.42	16.57
194.30	219.99	13.22
218.50	246.30	12.72
247.10	273.65	10.74
280.80	301.16	7.25
317.50	327.26	3.07
357.40	353.77	−1.02
399.80	378.36	−5.36
451.10	417.06	−7.55
489.30	446.86	−8.67
537.60	476.02	−11.45
580.40	503.82	−13.19
609.60	529.89	−13.08
668.50	556.52	−16.75

4.4. Discussion

The simulation results in Table 1 show that the measurement errors of this technique grows with increasing difference between RMS_J and the pass/fail threshold, which seems to be a limitation. Indeed, this makes the proposed technique less suitable for characterization testing. However, the technique can work well in pass/fail testing because the accurate measurement around the test specification reduces the chance of mis-classifying devices close to the specification. On the other hand, for devices well above or below the test specification, the measurement error is small enough so that they won't be mis-classified, either.

Deviations of d_1 and d_2 from their desired values due to process and/or temperature variations can also lead to test inaccuracies. To solve this problem, we may modify the variable delay so that it has more than two different delay values. This way, if only two of the delay values are close to the desired values, the test accuracy can be ensured.

5. Conclusion

In this paper, we present an RMS period jitter measurement technique intended for BIST applications. By comparing the phases of the signal under test and two of its delayed versions, information about the jitter's CDF curve is extracted and RMS jitter can thus be derived. Since only two points on the CDF curve are needed, the

test circuitry is quite simple. Behavior simulations have been performed to analyze the limitation of the proposed technique, and preliminary hardware measurement results are shown. In the future, we will investigate techniques that enhance the dynamic range of the proposed jitter measurement method.

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