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Quasi-static capacitance–voltage characterizations of carrier accumulation and depletion phenomena in pentacene thin film transistors

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Abstract

We analyze charge accumulation and depletion behaviors from *C–V* curves at various gate voltages, ramp rates and sweep directions in pentacene OTFTs. The polycrystalline property of the pentacene layer has lead to carrier charge and discharge processes in the channel layer by a trap-controlled transport mechanism. We apply such processes to describe *C–V* profiles at various ramp rates. Hysteresis can be observed from *C–V* curves at faster ramp rates. The phenomenon can be attributed to the difference of the relaxation time of carrier trap and detrap processes. As the ramp rate becomes slower, hysteresis disappears since most carriers are able to interact with the gate stress. And beyond this ramp rate, the corresponding threshold voltages are then kept at constant values, despite the existence of traps. Furthermore, low-mobility carriers (mobile ions or impurities) participate in the charge accumulation and depletion when the ramp rate is even slower, which results in a skew of *C–V* profiles. Finally, we extend the *C–V* measurement to devices with different channel lengths.

Keywords: Organic semiconductor; Thin film transistors; *C–V* measurement

1. Introduction

Over the past several years, organic thin film transistors (OTFTs) have become popular due to their unique properties compared with other semiconductor electronic devices [1–3]. The fabrication of OTFT devices and circuits on large-area substrates is one of the cost advantages that typical semiconductor cannot compete. In addition, low-temperature process of OTFTs on substrates with structural flexibility makes all previous impractical semiconductor applications become real. For example, OTFT circuits can be applied to flexible circuit boards for mobile phones, digital cameras, and identification tags, opening up a new arena for flexible electronics in the consumer market.

Traditional device physics and formulas originally developed for conventional metal–oxide–semiconductor field effect transistors (MOSFETs) have found their difficulties in describing the electrical properties of OTFTs, especially in defining important parameters, such as threshold voltages, mobilities and contact resistivities, of these devices [4–6]. For example, the presence of trapping centers in the channel of an OTFT causes the trap-filling transition as the gate voltage is applied. This effect has resulted in a significant variation of the effective mobility and threshold voltage with gate signals. Thus, traditional physical interpretation of the capacitance–voltage (*C–V*) profiles of MOSFETs using a simple resistance–capacitance (RC) circuit model can not be applied to those of OTFTs.

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Typically, MOSFETs experience accumulation, depletion and inversion stages as the gate voltage swings at a low frequency [7]. However, the low-intrinsic-density organic material has prohibited the appearance of an inversion layer in most, if not all of them, OTFT capacitors [8]. As a result, the definition of the threshold voltage in an OTFT depends on the charge carriers injected from the contacts, not on the formation of an inversion layer in the channel [9]. *C–V* measurements have been conducted by some groups to understand the carrier transport behavior in the channel layer of an OTFT [8–11]. For example, Scheinert et. al. concluded that the measured *C–V* profiles of an OTFT depend on the direction of gate voltage swing [9]. The effect of the hysteresis is related to the mobile ions, the kinetics of incomplete ionization and chemical reactions in the organic channel layer. Fujisaki et. al. also demonstrated a hysteresis in the *C–V* measurement [10]. They inferred that this phenomenon is caused by mobile ions in the insulators or by charge injections. Furthermore, Ryu et. al. calculated carrier mobilities based on quasi-static *C–V* (QSCV) and current–voltage measurements [11].

As for the carrier transport in the pentacene OTFTs, the polycrystalline property of the pentacene layer has lead to the development of the concept of the grain-boundary barrier with an energy distribution of the interfacial traps to describe the carrier transport [12]. The carrier density in the pentacene channel layer is related to the injection of carriers from source and drain electrodes, gate bias voltages and relaxation time of trap and detrap processes. In an accumulation mode TFT, since carriers interact with the trap and detrap processes, carrier mobilities vary over a wide range depending on the applied electric field and stress duration.

In this paper, we conduct a full analysis of charge accumulation and depletion behaviors from the *C–V* curves at various gate voltages, ramp rates and sweep directions in pentacene OTFTs. We first describe the carrier charge and discharge processes in the channel layer using a trap-controlled transport mechanism. The carrier/mobile ion charge and discharge processes are then applied to describe *C–V* profiles at various ramp rates. Hysteresis can be observed from *C–V* curves at most ramp rates investigated. We next compare extracted threshold voltages at various ramp rates. And finally, we extend the *C–V* measurement to devices with different channel lengths for comparisons.

2. Device fabrication

Fig. 1 schematically shows the structure of a bottom gate OTFT. First, a 1500 Å metal layer of ITO (indium tin oxide) was sputtered on a glass substrate and patterned by photolithography as the gate electrode. Subsequently, the SiO_2 dielectric layer was coated by PECVD (plasma enhanced chemical vapor deposition) and the ITO source-drain electrodes were deposited on the surface of the pentacene film with a shadow mask. We next deposited the channel layer with a 1000 Å thickness of pentacene. We

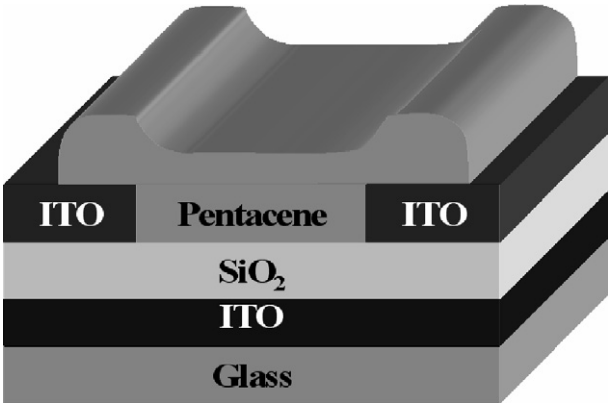

Fig. 1. Schematic cross section of a pentacene OTFT.

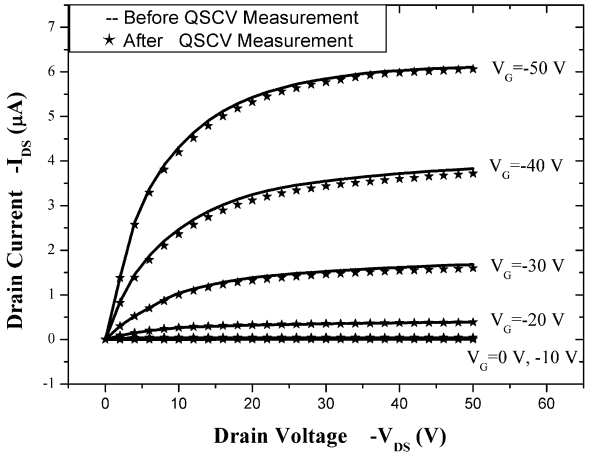

Fig. 2. I_{DS}–V_{DS} curves of an OTFT before (solid lines) and after (stars) *C–V* measurement.

have designed OTFT devices with different channel lengths (57 μm, 37 μm, 17 μm, respectively) but all with a fixed channel width at 10,000 μm.

Once the samples were fabricated, we used an HP4155C precision semiconductor parameter analyzer to measure the electrical characteristics of OTFTs. To obtain a consistent performance of *C–V* profiles, the devices were placed in a box purged with dry air for several weeks. We monitored the I_{DS}–V_{DS} curves every 24 h until the day-to-day variation is less than 5%. For the samples that *C–V* measurement was conducted later, they were sitting in the dry box longer than 80 days. Also, the variation of I_{DS}–V_{DS} curves before and after the *C–V* measurement has to be less than 2% to be counted as a reliable OTFT device (see Fig. 2). Even though the discussion of stability is not the main topic of this paper, the purpose of the test is to minimize the potential variations of *C–V* profiles incurred from the device instability.

3. *C–V* measurement

Quasi-stable *C–V* (QSCV) measurement was also performed with an HP4155C semiconductor parametric ana-

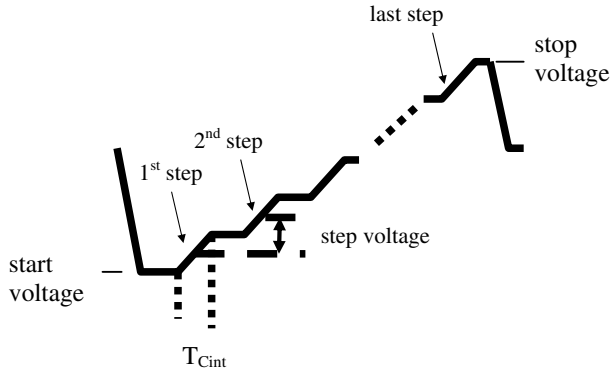

Fig. 3. QSCV measurement sequence. In this measurement, capacitance is extracted by considering the additional charges at each step interval (T_{Cint}) and leakage currents before and after each step.

lyzer. The voltage ramp profile is illustrated in Fig. 3. In this measurement, we set the step voltage to 3 V and vary T_{Cint}, the integration time for the capacitance measurement. For instance, 3 V/33 ms indicates that the capacitance is extracted every 33 ms (T_{Cint}) with a step voltage increase (or decrease) of 3 V. The capacitance is calculated from the differential charge required to change the capacitor voltage over T_{Cint} and is carried out automatically by the machine. Detailed calculations of QSCV measurement can be referred from [13].

4. Results and discussions

We start from a faster gate signal swept in both directions. As shown in Fig. 4, at a ramp rate 3 V/33 ms, when the gate voltage is swept from negative to positive, holes and positive carriers will be first induced and accumulated in the channel layer. On the other hand, while the gate bias is scanned from positive, the channel starts from the depletion region. Therefore, the capacitance of the device at an accumulation stage (V_{GS} from −50 V to +49 V) is clearly higher than that of the depletion stage (V_{GS} from +50 V to −49 V). Interestingly, the capacitance is kept at a constant value for both cases, indicating carriers cannot accumulate (or deplete) in the channel as the gate voltage swings from positive (or negative). The phenomenon is attributed to a much longer relaxation time of the carriers in the polycrystalline pentacene channel layer than the duration of the scan. In other words, most carriers in the channel are not able to respond to the gate signal at 3 V/33 ms.

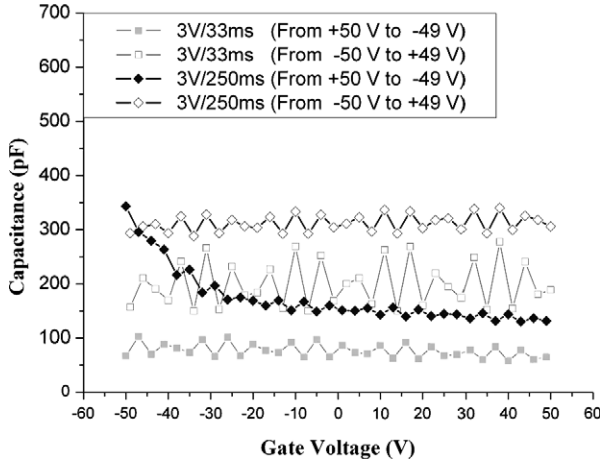

Fig. 4. QSCV curves for ramp rates between 3 V/33 ms and 3 V/250 ms.

As the ramp rate decreases to 3 V/250 ms, the effect of charge accumulation begins to take place for the case that the gate voltage sweeps from positive to negative, which means carriers can be accumulated during the measurement. From Fig. 4, the threshold voltage, V_T, defined from the onset gate voltage of accumulation of carriers from depletion mode, is around −33 V at 3 V/250 ms from positive to negative direction. Such a ramp rate can not only recover carriers from depletion, but also allows positive carriers to accumulate if the attracting voltage is high enough. On the contrary, as the gate voltage is scanned in the reversed direction at 3 V/250 ms, the transition from the accumulation to depletion is not observed. In either sweep direction, the capacitance is higher at 3 V/250 ms than that at 3 V/33 ms, indicating that more carriers are able to respond to the slower gate signals.

We then further slow down the gate sweeping signals. Both sweep directions simultaneously show accumulation and depletion modes in Fig. 5, but the threshold voltages in both directions do not match each other as they should in typical MOSFETs. To understand the hysteresis of the C–V curves, we first look at the charge and discharge process in an OTFT channel. The transition from an accumulation to a depletion stage or vise versa is determined by the duration and strength of the gate voltages to stress and interact with carriers. The relationship of ramp rates and threshold voltages can be verified from QSCV profiles in Figs. 4 and 5. When the device is scanned at 3 V/33 ms from the negative direction, the depletion can't be seen in

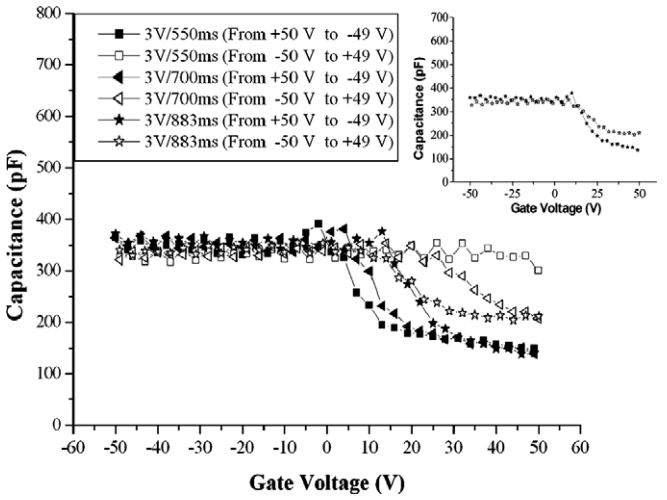

Fig. 5. QSCV curves for ramp rates between 3 V/550 ms and 3 V/883 ms. Inlet: At 3 V/866 ms, QSCV curves at both sweep directions coincide and possess the same threshold voltage.

Fig. 4 since V_G has to be larger than +50 V to initiate the transition from accumulation to depletion. As the ramp rate becomes slower, more and more carriers are able to respond to the gate voltages. Thus, less bias is required to deplete the channel and V_T becomes smaller. On the other hand, for the gate voltages scanned from positive to negative, the channel is initially at a depletion stage. V_G has to be either (negatively) large enough or slow enough to attract holes (or positive carriers) for the OTFT to be at an accumulation mode. Therefore, again, the transition can't be seen in the QSCV profiles until the scanning rate is slower. When we decrease the ramp rate to 3 V/866 ms, both scanning directions share the same threshold voltage (see the inlet of Fig. 5) even though the capacitances at depletion are slightly off. We believe 3 V/886 ms is the scanning rate that all of the carriers in the channel can respond to the gate signals. That is, even though the mobility of the carriers in the channel is strongly correlated to the trap and detrap processes during the stress of the gate signal, the scanning rate 3 V/886 ms scanning rate, is slower than the relaxation time of both processes and thus the carrier transition–depletion process of OTFTs behaves similar to that of conventional FETs. From Figs. 4 and 5, for the QSCV curves with ramp rates between 3 V/33 ms and 3 V/886 ms, hysteresis behaves similar to that illustrated in Fig. 6. At first, large hysteresis between both sweep directions can be observed for QSCV curves at a fast ramp rate. As the ramp rate decreases, the hysteresis becomes smaller until it disappears at 3 V/886 ms. The hysteresis of the QSCV profiles can be attributed to the difference of the relaxation time of the trap and detrap process in the polycrystalline pentacene layer.

As we decrease the ramp rate beyond 3 V/886 ms, both profiles at 3 V/3 s and 3 V/5 s in Fig. 7 demonstrate a skew in QSCV curves that are different from those in Figs. 4 and 5. Such phenomena can also be seen in [9] for OTFTs and in [14] for MOSFETs. In the MOSFET structure, the skew of the QSCV profiles suggests a shunt path from the leaky oxide layer or the alternative carrier flow starts to occur when the stress is strong enough [14]. However, in our OTFTs, the dependence of the slope of the QSCV profile

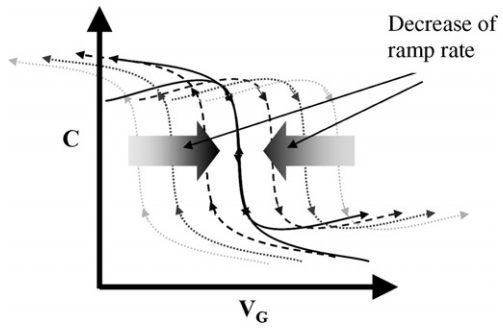

Fig. 6. Schematic diagram that shows the trend of QSCV curves with the decrease of ramp rates at both sweep directions. Small arrows: gate signal sweep directions, and large arrow bars: direction of decrease of ramp rates.

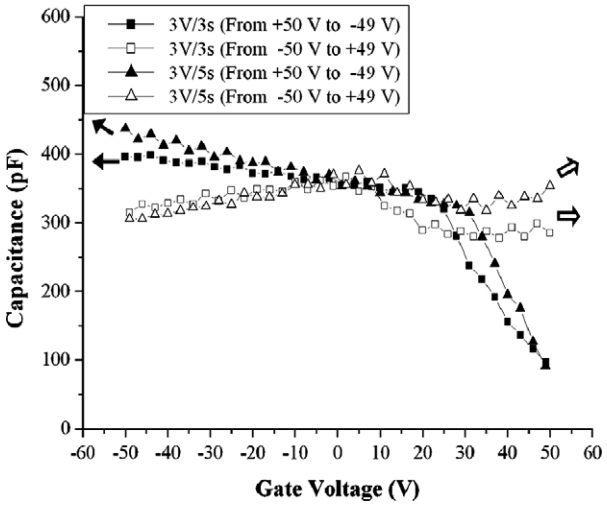

Fig. 7. QSCV curves for ramp rates at 3 V/3 s and 3 V/5 s.

on the sweep direction implies that both positive and negative carriers participate in the gate stress process. We believe that at such low ramp rates low-mobility carriers such as mobile ions or impurities start to interact with gate signals. For both sweep directions, in addition to the accumulation–depletion mode profiles in QSCV curves, low-mobility positive carriers are induced in the negative gate voltage range while low-mobility negative carriers are accumulated in the positive sweep range. Thus, as the gate voltage is applied in either direction, an increase of capacitance can be seen in both 3 V/3 s and 3 V/5 s ramp rates.

We next plot V_T as a function of QSCV ramp rates for both sweep directions (see Fig. 8). In this figure, threshold voltages at 3 V/3 s and 3 V/5 s are discarded to avoid distortion of the trend of V_T with ramp rates. Threshold voltages are cramped at a constant value for ramp rates slower than 3 V/1000 ms, a little bit longer than the crossing point of 3 V/866 ms. The saturation of threshold voltages supports the explanation that almost all the carriers are able to interact with gate signals beyond 3 V/886 ms ~3 V/

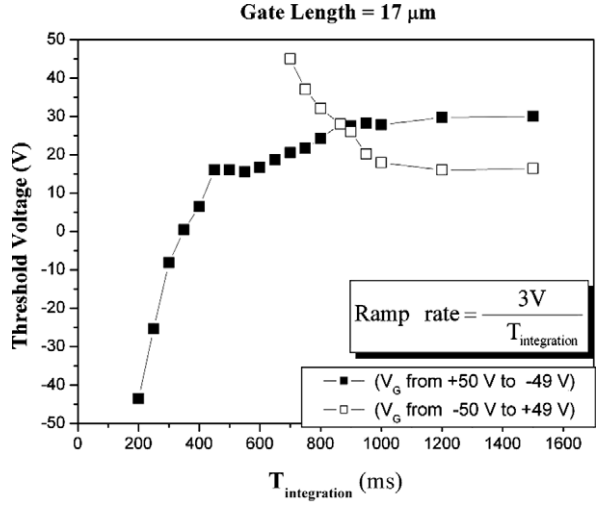

Fig. 8. V_T vs. ramp rate for a device with a 17 μm channel length.

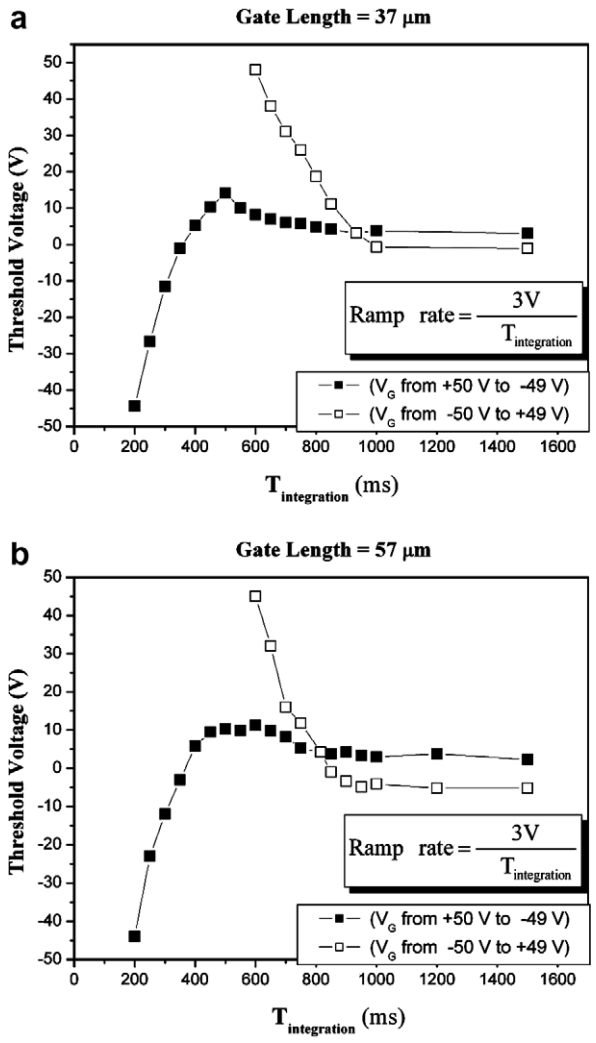

Fig. 9. V_T vs. ramp rate for a device with a 37 μm channel length (a) and a 57 μm channel length (b).

1000 ms, despite the existence of trap and detrap processes. The transition between accumulation and depletion modes of OTFTs is similar to that of MOSFETs in this range since all of the carriers can be modulated by field effects. Furthermore, the offset of the saturated voltage between different sweep directions is attributed to the leaky shunt path from mobile ions or impurities.

We further extend our C–V measurement to OTFT devices with longer channel lengths. Since the thickness of the OTFT channel layer is unchanged, the profile behaves similarly. Fig. 9a shows V_T as a function of ramp rates for a device with a channel length 37 μm and Fig. 9b demonstrates that for the 57 μm case. From the figure, the threshold voltage becomes constant for ramp rates slower than 3 V/933 ms and 3 V/816 ms for devices with channel lengths 37 μm and 57 μm, respectively.

5. Conclusion

We analyze carrier charge and discharge behaviors from QSCV profiles at various gate voltages, ramp rates and sweep directions in pentacene OTFTs. In an accumulation mode TFT, since carriers interact with trap and detrap processes, carrier mobilities vary over a wide range depending on the applied electric field and stress duration. During the stress, hysteresis can be found when most carriers in the channel are not able to respond to the scanning gate signals. The hysteresis is attributed to the difference of the relaxation time between the trap and detrap process in the polycrystalline pentacene layer. For OTFTs with a channel length 17 μm, the threshold voltages of both sweep directions coincide at 3 V/886 ms. The threshold voltages are then kept at constant values, indicating that all of the carriers in the channel can respond to the gate signals, despite the existence of traps. Furthermore, low-mobility carriers (mobile ions or impurities) participate in the charge accumulation and depletion processes when the ramp rate is even slower, which results in a skew of C–V profiles. We also compare threshold voltages of several ramp rates. Finally, we extend the C–V measurement to devices with 37 μm and 57 μm channel lengths. Since the pentacene layer thickness is the same as that of the 17 μm case, the QSCV profiles behave similarly.

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