nating z- and w-terminals with proper resistors and taking the current through a w-terminal resistor as the output, it is always possible to provide a gain for the all-pass responses.

As an interesting application of the proposed all-pass networks, a new bandpass configuration is given. This circuit operates in current-mode and offers a simpler circuit configuration compared with its voltage-mode counterparts in [1]–[4], [16]. As expected from the above discussion, the numbers of the passive and active components are reduced significantly, while the circuit still offers the main advantages of the CM operation.

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A CMOS Pulse-Shrinking Delay Element For Time Interval Measurement

Poki Chen, Shen-Iuan Liu, and Jingshown Wu

***Abstract*—A deep sub-nanosecond resolved CMOS pulse-shrinking delay element used in the time-to-digital converter (TDC) is proposed. The pulse-shrinking capability of the element is controlled by the dimension ratio of the adjacent gates. This control mechanism is completely different from the bias adjustment adopted in the conventional pulse-shrinking element. Without the need of continuous calibration, the presented element possesses not only extremely fine resolution, small single-shot errors, low power consumption, but also good insensitivity to the supply voltage variation. Being fabricated with 0.35-μm CMOS technologies, the TDC made of the new elements has been measured to have a resolution of 68 ps. The effective resolution only varies 1.5 ps for a rather large supply voltage range from 3.5 to 4.5 V. The size of the circuit is 0.35 mm $\times$ 0.09 mm only, excluding the I/O pads. Under a single 3.3-V power supply, the static power dissipation, including the I/O pads, is 1 μW. The average power consumption is measured to be merely 1.2 mW under a measurement rate of 100 ksps.**

***Index Terms*—Delay line, pulse-shrinking delay, TDC, time interval measurement.**

I. INTRODUCTION

Time-interval digitization is an important technique for many applications, such as laser range finders, phase meters, and PM or FM demodulators, etc. [1]–[3]. The conventional un-integrated TDC circuit is very bulky and has high power consumption. At the end of 1995, a novel CMOS time-to-digital converter (TDC) circuit with a linear delay line structure was proposed to get 780-ps resolution, and 15-mW power consumption at the expense of 3-ns single-shot accuracy [5]. The mismatch among the pulse-shrinking delay elements severely limits the TDC accuracy. And, the power-wasting calibration of the TDC must be done continuously.

Another kind of CMOS TDC with a cyclic delay line, called cyclic TDC, was announced to greatly improve the linearity [6], [7]. The effective resolution was measured to be 286 picoseconds. Without any continuous calibration, the single-shot errors are measured to be less than 1/2 the least significant bit (LSB) width. Its structure is replotted in Fig. 1(a). The same pulse-shrinking delay element used as that of the linear CMOS TDC [4] is shown in Fig. 1(b). By adjusting the bias voltage $V_{\rm bias}$, the pulse-shrinking time per cycle can be varied. The input pulse will visit every element in the cyclic delay line once per cycle. The pulse-shrinking time must be the same from cycle to cycle, and the cyclic TDC has no nonlinearity problem. But, at the initial calibration, $V_{\rm bias}$ must be adjusted externally to make the resolution fine enough. It is inconvenient for measurement automation.

Later, a FPGA-based TDC without the need of any continuous calibration or external bias adjustment was proposed in 1997 [8]. The resolution is as low as 200 ps, but the measured single-shot errors are larger than 1/2 LSB width. Furthermore, too many trial-and-errors must be adopted in the design phase to get satisfactory implementation for each TDC. Another major disadvantage is that it is more difficult to control the element matching in FPGA than in customer-designed ICs. It will further limit the FPGA TDC in finer resolution applications.

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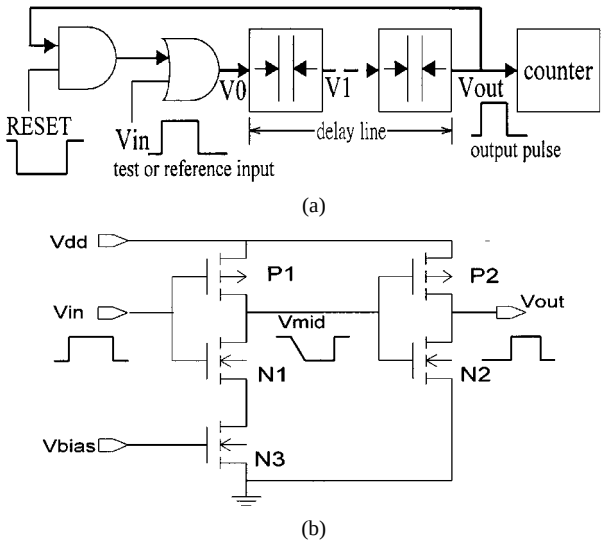

Fig. 1. (a) Structure of conventional (a) cyclic TDC and (b) pulse-shrinking delay element

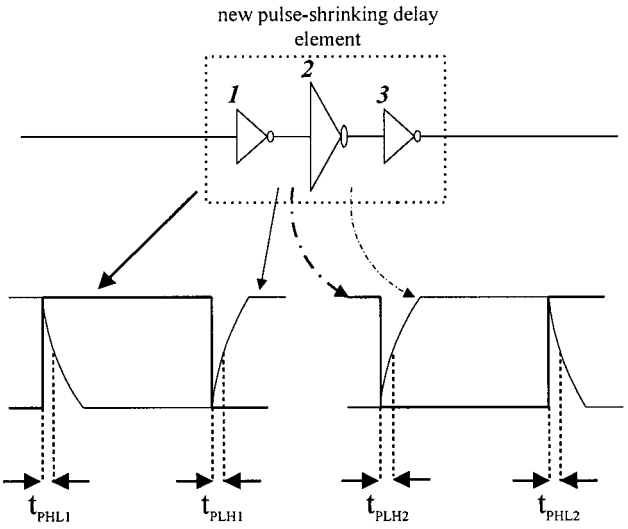

Fig. 2. Proposed dimension-controlled pulse-shrinking delay element

To overcome all the shortcomings, a new CMOS pulse-shrinking delay element is proposed in this paper to alleviate the need of continuous calibration, external bias adjustment, or trial-and-error implementation of the TDCs realized.

II. Operation Principles

Fig. 2 shows the conceptual block diagram of the proposed pulse-shrinking delay element. The circuit is fully digital, and no bias adjustment is needed for pulse-shrinking control. The dimensions of the gates **1** and **3** are the same. Only that of the gate **2** is different. The inhomogeneous dimension of the gates makes the input pulse undergo different rising and falling time at the interface boundaries among the gates. This mechanism can be used to accurately control the pulse shrinking of this new element. To simplify the derivation, the input pulse is supposed to be stepwise at each stage for the first-order approximation only. When

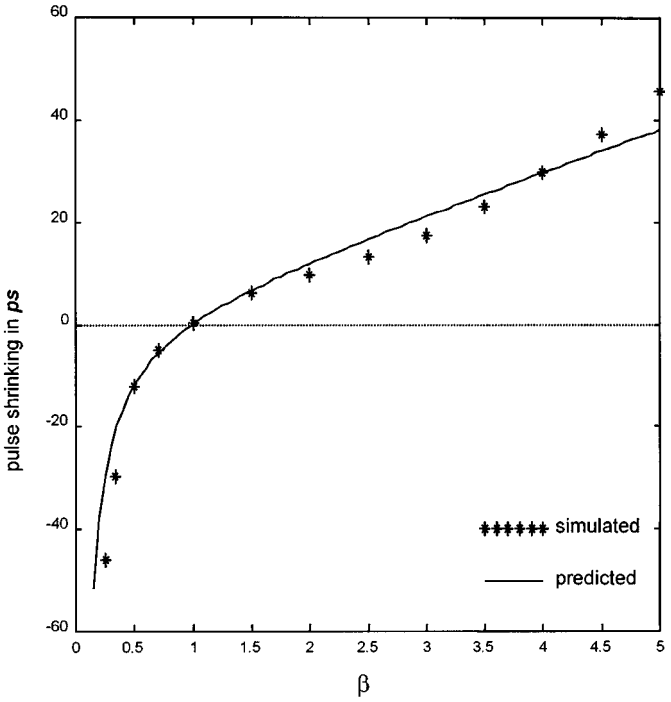

Fig. 3. Influence of the dimension ratio on the pulse shrinking of the new element

the pulse goes from gate **1** to gate **2**, the falling time and the rising time can be given [9]

$$t_{PHL1} = \frac{2C_2V_{TN}}{k_{N_1}(V_{DD}-V_{TN})^2} + \frac{C_2}{k_{N_1}(V_{DD}-V_{TN})} \cdot \ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right) \quad (1)$$

$$t_{PLH1} = \frac{-2C_2V_{TP}}{k_{P_1}(V_{DD}+V_{TP})^2} + \frac{C_2}{k_{P_1}(V_{DD}+V_{TP})} \cdot \ln\left(\frac{1.5V_{DD}+2V_{TP}}{0.5V_{DD}}\right) \quad (2)$$

where k_{N_1}, k_{P_1} are the transconductance parameters of the gate **1**, and C_2 is the effective input capacitance of the gate **2**. Assume $-V_{TP} = V_{TN}$, then the pulse-shrinking time from gate **1** to gate **2** can be analyzed as $t_{PLH1} - t_{PHL1}$

$$\Delta W_1 = C_2\left(\frac{1}{k_{P_1}} - \frac{1}{k_{N_1}}\right)\left[\frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{(V_{DD}-V_{TN})} \cdot \ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right] \quad (3)$$

Similarly, the pulse-shrinking time from gate 2 to gate 3 can be analyzed as $t_{PHL2} - t_{PLH2}$

$$\Delta W_2 = -C_3\left(\frac{1}{k_{P_2}} - \frac{1}{k_{N_2}}\right)\left[\frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{(V_{DD}-V_{TN})} \cdot \ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)\right] \quad (4)$$

where $C_3 = C_1$. The total pulse-shrinking time can be found as

$$\Delta W = \Delta W_1 + \Delta W_2 = \partial_i\left[C_2\left(\frac{1}{k_{P_1}} - \frac{1}{k_{N_1}}\right) - C_1\left(\frac{1}{k_{P_2}} - \frac{1}{k_{N_2}}\right)\right] \quad (5)$$

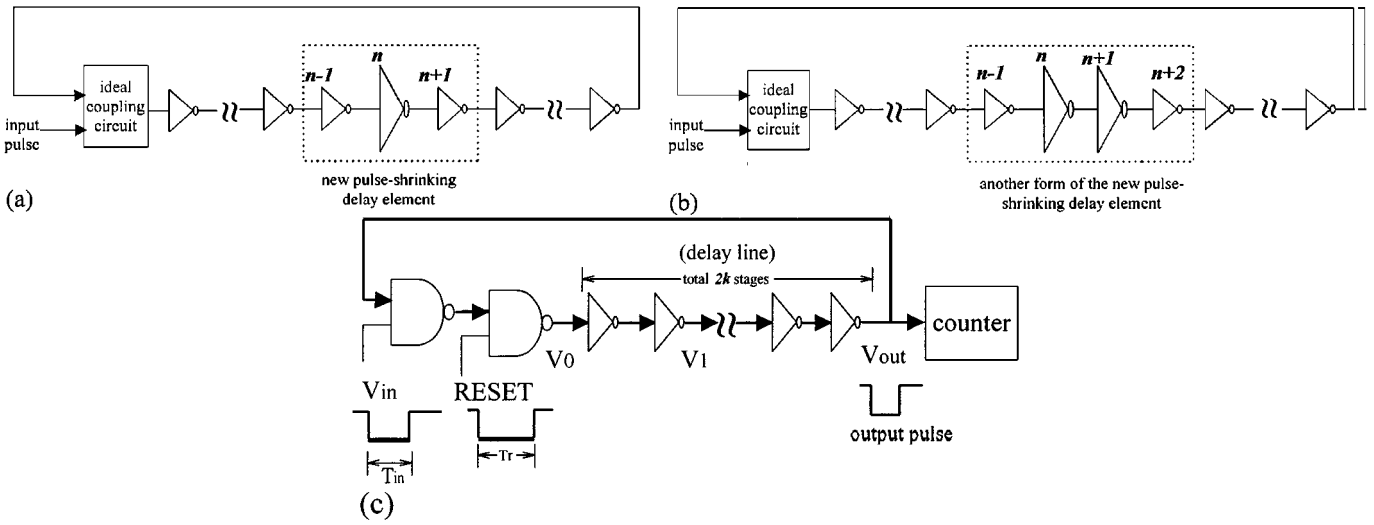

Fig. 4. (a) Improved cyclic delay line with the new element. (b) Extension of the improved cyclic delay line in Fig. 4(a). (c) Realized cyclic TDC with a delay line in Fig. 4(b)

where

$$\partial_i = \frac{2V_{TN}}{(V_{DD}-V_{TN})^2} + \frac{1}{(V_{DD}-V_{TN})} \cdot \ln\left(\frac{1.5V_{DD}-2V_{TN}}{0.5V_{DD}}\right)$$

is a constant factor which is more or less layout independent. By varying the dimension ratio of the NOT gates, the pulse-shrinking time can be easily controlled. For example, let the length and the width of the gates are $\boldsymbol{L_1 = L_2 = L_3}$ and $\boldsymbol{W_2 = \beta W_1 = \beta W_3}$. Then we have $k_{N_2} = \beta k_{N_1}$, $k_{P_2} = \beta k_{P_1}$, $C_2 = \beta C_1 = \beta C_3$, and the total pulse-shrinking time can be further simplified to be

$$\Delta W = \left(\beta - \frac{1}{\beta}\right) C_1 \left(\frac{1}{k_{P_1}} - \frac{1}{k_{N_1}}\right) \partial_i. \tag{6}$$

To verify the derivation, the simulation result for different β value is shown in Fig. 3. The device sizes used for the gates **1** and **3** are 3 μm/1 μm for pMOS, and 1 μm/1 μm for nMOS. The simulation result matches the prediction curve well.

With the newly proposed pulse-shrinking delay element, one can improve the structure of the cyclic TDC to have finer resolution and get rid of the external bias adjustment. The new cyclic delay line, shown in Fig. 4(a), is derived from the new element directly. The gate ***n*** is the only inhomogeneous element, and its dimension is used to control the pulse-shrinking capability. The circuit in Fig. 4(b) is merely an extension of Fig. 4(a). Though the number of inhomogeneous gates in the delay line is increased to two, the input pulse still undergoes different rising and falling time around the inhomogeneous gate boundaries. In reality, no mater how many inhomogeneous gates exist in the delay line, the pulse-shrinking mechanism still works. Fig. 4(c) plots the realized cyclic TDC with a cyclic delay line in Fig. 4(b). The only two NAND gates in the delay line are implemented to be the inhomogeneous gates as well as the coupling circuit.

Similar to the influence of the inhomogeneity, the supply-voltage variation will also affect the rising and falling times of the gates. This affection will be somehow canceled by the reverse operation modes between the adjacent gates. Consequently, the new pulse-shrinking element will become less sensitive to supply voltage variation.

For the last few cycles, the input pulse will become too narrow to make the counter toggle its states. A big offset error occurs when the pulse-shrinking time per cycle is relatively small. However, the offset error can be eliminated by a careful calibration process. First, feed two

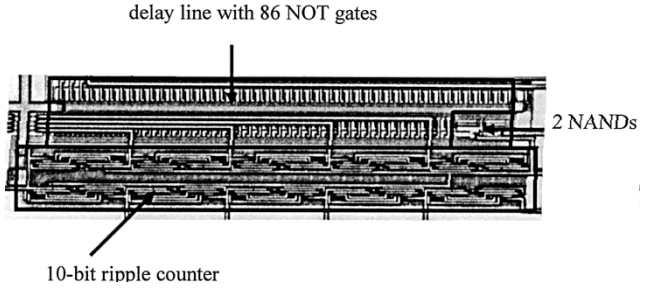

Fig. 5. Photomicrograph of the new TDC

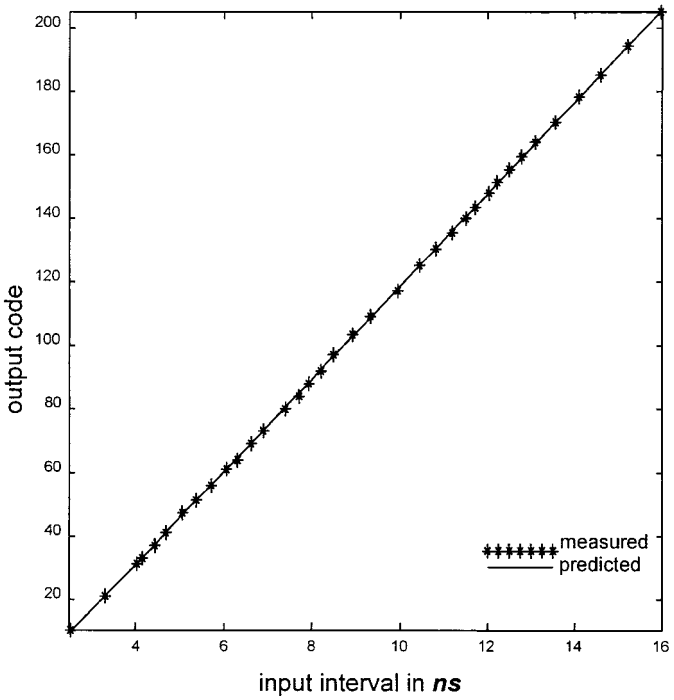

Fig. 6. Result of the single-shot measurements

TABLE I
PERFORMANCE OF SEVERAL REPRESENTATIVE TDCS

item	linear TDC[5]	FPGA-based TDC[8]	proposed TDC
LSB width	780 *ps*	200 *ps*	68 *ps*
single-shot accuracy	3.8 LSB (3 *ns*)	< 1.3 LSB	< 0.8 LSB
continuous calibration	Yes	No	No
bias control	Yes	No	No
trial-and-error design	No	Yes	No
supply voltage	4.5-5.5 V	NA	1.5-4.5 V
power consumption	15 *m*W	NA	1.2 *m*W
chip size	2.9*m*m × 2.5*m*m	NA	0.35*m*m × 0.09*m*m

reference periods $\boldsymbol{T_{ref1}}$ and $\boldsymbol{T_{ref2}}$ to the TDC input. Assume that the circuit gets $\boldsymbol{N}$ and $\boldsymbol{N'}$ counts respectively. Then

$$T_{\rm ref1} = \alpha N + T_{\rm offset} \quad \text{and} \quad T_{\rm ref2} = \alpha N' + T_{\rm offset}$$

Where $\boldsymbol{\alpha}$ is the effective resolution, and $\boldsymbol{T_{offset}}$ is the measurement offset. By resolving $\boldsymbol{\alpha}$ and $\boldsymbol{T_{offset}}$ from the above equations, the measured width of an input pulse $\boldsymbol{T_{in}}$ with output code $\boldsymbol{M}$ can be calculated as

$$T_{\rm in} = \alpha M + T_{\rm offset} = \frac{(M-N)T_{\rm ref2} + (N'-M)T_{\rm ref1}}{N'-N}. \tag{7}$$

If $\boldsymbol{T_{ref2}}$ is realized as twice of $\boldsymbol{T_{ref1}}$ by dividing the stable reference frequency of $\boldsymbol{T_{ref1}}$ by 2, we will have $T_{\rm ref2} = 2T_{\rm ref1} = 2T_{\rm ref}$ and

$$T_{\rm in} = \frac{M + N' - 2N}{N' - N} T_{\rm ref}. \tag{8}$$

When necessary, the calibration can be redone just before measurement to get the best accuracy.

III. MEASURED RESULTS

To evaluate the performance of the proposed pulse-shrinking delay element, the new cyclic TDC in Fig. 4(c) has been fabricated with the standard 0.35-μm SPDM CMOS process. The cyclic delay line is composed of 86 NOT gates and 2 NAND gates. The aspect ratios are 12 μm/1 μm, 8 μm/1 μm for pMOS and nMOS transistors in NAND gates; 6 μm/1 μm, 2 μm/1 μm for pMOS and nMOS transistors in NOT gates. The photomicrograph of the new TDC is shown in Fig. 5. With transistors of nonminimal length 1 μm, the size of the circuit is 0.35 mm × 0.09 mm only, excluding the I/O pads. The static dissipation current, including the I/O pads, is 0.3 μA only. The average current consumption is measured to be 370 μA under a measurement rate of 100 ksps, and a single 3.3-V supply.

To find out the effective resolution of the new cyclic TDC, a series of pulses with different width were sent to this TDC for coding. The same input pulses were also measured with a Standford Research Systems SR620 universal counter and a Tektronix TDS680B real-time digital oscilloscope. The measured results of single-shots along with the theoretical prediction line are depicted in Fig. 6. Due to the implemented TDC with a short delay line of 43 buffers only, the output code is limited around 200. The valid output code range can be further increased by lengthening the delay line. Though no calibration as in (7) is done during the whole measurement process, the experimental data agrees with the linear prediction very well. The effective resolution α and the measurement offset $\boldsymbol{T_{offset}}$ are calculated to be 68 ps and 1.86 ns, respectively. All the single-shot errors are around 1/2 LSB width. In reality, the TDC with cyclic delay line structure possesses perfect linearity. It is reasonable to believe that the errors, corresponding to such deep sub-nanosecond resolution, may be mostly induced by the jitter effect of the pulse generator and the inherent measurement error of the universal counter. The dead time of the single-shot measurement is at most a few microseconds, depending on the width of the measured pulse. A measurement rate of at least 100 kHz is promised for the realized TDC.

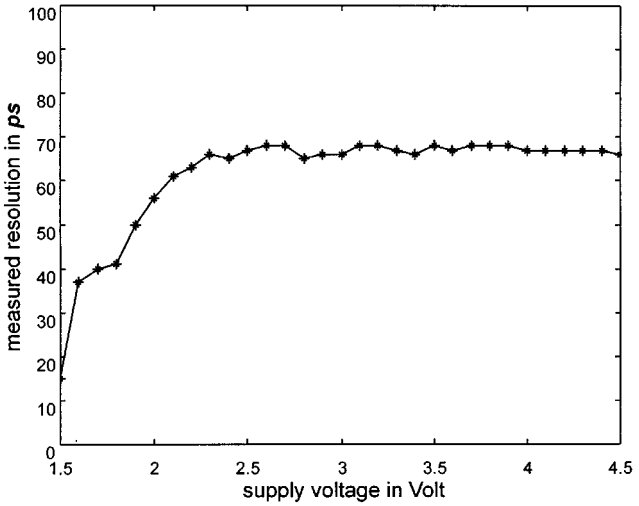

Fig. 7. Measured result of the supply voltage dependence of the new cyclic TDC.

To verify the supply voltage dependence of the new TDC, another series of experiments were conducted for supply voltage ranging from 1.5 to 4.5 V with 0.1-V increments. For each supply voltage, only two different single-shot pulses were coded by the TDC and the effective resolution was estimated as the ratio of the pulse width difference over the output code difference. The corresponding results without calibration are shown in Fig. 7. The effective resolution only varies 1.5 ps for a rather large supply voltage range from 3.5 to 4.5 V.

IV. CONCLUSION

A novel dimension-controlled CMOS pulse-shrinking delay element has been presented. The pulse-shrinking capability of the element is controlled by the relative dimension ratio of the adjacent gates. Being fabricated in a 0.35-μm SPDM process, the cyclic TDC composed of the new element can reach an exceedingly accurate resolution of 68 ps by experiments. No bias adjustment or continuous calibration is needed. With its extreme simplicity, miniature size, and voltage insensitivity, the TDC is the best solution for accurate portable applications. The performances of several representative TDCs with different pulse-shrinking delay elements are summarized in Table I.

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RDS and IRDS Filters for High-Speed CCD Video Sensors

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***Abstract*—In this brief, we present two filters called "reflection delayed noise suppression" (RDS) and "integration reflection delayed noise suppression" (IRDS) which are useful to increase dynamics of video charge-coupled device (CCD) cameras. The RDS is a band-pass filter built with a parallel short-circuited line. It significantly lowers the most important noise, called reset noise. Unfortunately, this signal processing unit increases the contribution of thermal fluctuations by at least 3 dB. To overcome this disadvantage, a reset low-pass filter can be added to the RDS cell, which leads to the IRDS method. For both methods, we will describe the principle and compare their effects in a theoretical way, and by experimentation on sensing-node amplifier and reset noise in the CCD sensor.**

***Index Terms*—CCD digital, high-speed electronics, IRDS filter, noise measurement and suppression, RDS filter, .**

I. INTRODUCTION

Assessment of charge-coupled device (CCD) noise is important in establishing dynamic range and low-light level sensitivity of CCD image sensors. Floating-diffusion reset noise and sensing-amplifier noise are serious limitations in these domains of application [1]. It is, therefore, desirable to remove these kinds of noises to obtain low-light-level performance.

Reset noise, or KT/C noise, is associated with resetting the sense node capacitor. It is due to thermal noise generated by the static drain-source on-state resistance $R_{\rm on}$ within the resetting MOSFET.

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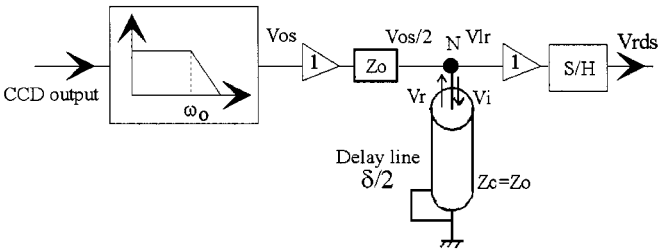

Fig. 1. Circuit diagram of RDS.

This noise is sampled and held by the floating capacitor which is periodically reset.

Sensing amplifier noise consists of two components, namely thermal-channel noise and $1/f$ noise. Thermal-channel noise, which is a white noise, is generated by the MOSFET transistors of the sensor readout stage. It is equivalent to an input noise resistance R_n given by $R_n = \beta/g_{mo}$, where g_{mo} is the amplifier transconductance and β varies between 2/3 and 10, and depends upon gate and drain voltage, oxide capacitance, and substrate doping. The other well-known source is the $1/f$ noise generally associated with fast interface state trapping. This kind of noise has a zero mean value and a $1/f$ power spectral density. It is highly visible in the displayed image as a series of streaks across the field, and hence is strongly disturbing for the human eye.

Reset noise and video signals are correlated in that both video and reset levels have the same fluctuation within one pixel cycle. Theoretically, by subtraction between floating and video levels within each pixel cycle, resetting noise should be suppressed.

A well-known technique for this purpose is the correlated double sampling (CDS) [2]. Moreover, it practically cancels the low-frequency $1/f$ noise generated by the output amplifier, but it increases the thermal fluctuations by at least 3 dB. The reflection delayed noise suppression (RDS), which is a single-sampled circuit, theoretically gives the same result [3]. Experimentally, it ensures a better attenuation of reset and $1/f$ noises [1] and its conception is easier to achieve. As it can run at frequencies greater than 20 MHz, it has been integrated in a digital high-speed camera operating at 1000 frames per second [4].

In order to reduce this thermal noise accentuation, Y. Nishida *et al.* [5] developed the "ICDS" filter by inserting, in both channels of the CDS, a low-pass circuit in which the capacitor was discharged before every pixel readout. We used the same principle for the RDS system by adding a reset low-pass filter which integrates the signal and the remaining noise during the 2/5 of the pixel period T_e. This system, called "integration reflection delayed noise suppression" (IRDS) is equivalent to the ICDS circuit, but its simple structure allows it be used in high-speed video cameras.

In this brief, all calculations and measurements have been made taking account of the characteristics of the black and white CCD HS0512J from the EG&G-Reticon firm. The pixel frequency used is 10 MHz, which permits reaching a rate of 500 frames per second.

II. RDS

A. Principle

The diagram of RDS is shown in Fig. 1. It consists of a parallel short-circuited stub of characteristic impedance Z_c ($=Z_0$ so that the line is matched at the input) and propagation time $\delta/2$. It is inserted between two buffers with low output and high input impedance, an anti-aliasing low-pass filter of cutoff angular frequency ω_0 and a zero order sample and hold (S/H).