Thermal Stress Analysis for Rapid Thermal Processor

Ching-Kong Chao, Shih-Yu Hung, and Cheng-Ching Yu

***Abstract*—Within the framework of linearized thermoelasticity theory, the temperature and thermal stresses on the wafer for the rapid thermal processor are solved by using the finite-difference approach and a trapezoidal integration technique, respectively. Although the equations governing the present thermoelastic system are coupled in nature, the temperature can still be obtained independently due to the fact that the coupling term is negligible as a result of the strain rate being extremely small as compared with unity. Based on the maximum shear stress failure criterion, the calculated results show that material failure always occurs at the edge of the wafer at the beginning of cooling processes. Furthermore, the maximum stress control scheme is proved to be more efficient that it can significantly reduce the required cooling time and thermal budgets. Thus, the conventional constant cooling-rate control scheme or linear temperature ramp-down scheme is not appropriate for the rapid thermal processor.**

***Index Terms*—Cooling control, rapid thermal processor, thermal stress, transient heat transfer.**

I. Introduction

THE CONTINUING miniaturization of IC components and the increasing function and performance of a single IC chip are the recent trends in the semiconductor industry. The quality control of the wafer is becoming more and more important as the wafer becomes larger and the feature size shrinks. Rapid thermal processing (RTP) is used for various single-wafer thermal treatment processes including annealing, cleaning, oxidation, and chemical vapor deposition. Because wafers processed using RTP have the advantage of fast ramp-up and -down time compared to conventional batch furnaces, it permits processes to be accomplished with minimal dopant redistribution and uniform deposition quality by the smaller thermal budget. However, poor RTP system design can lead to significant temperature difference in the wafer. One of the main shortcomings that RTP must overcome is that of heating (or cooling) the wafers ununiformly which would result in material failure due to increasing of thermal stresses or serious warpage. The damage due to the presence of thermal stresses can represent a limit to the applicability of the rapid thermal processing.

The temperature nonuniformity in the wafer is caused by three factors: edge effect, pattern effect, and heat source. In this analysis, we consider only the edge effect. The higher heat loss from the wafer edge was found to result in a radial temperature gradient in the wafer. Hu [1] found that the temperature gradient induces a thermal stress which is compressive in the central region of the wafer but is tensile toward the edge of the wafer and can often exceed the yield stress in silicon wafers, causing plastic deformation. To improve the wafer temperature nonuniformity produced by the edge effect, several radiative shields were placed at the edge of the wafer to reduce the heat loss from the wafer edge and reflect the radiative energy back into the wafer during the cooling process [2]. By varying the angle of the shield, an optimal shield configuration can be found to minimize the induced thermal stress [3]. However, this pattern would overheat the wafer edges during heating processes leading to a high stress level [4]. Hebb and Jensen [5] showed that pattern-induced temperature nonuniformity can cause plastic deformation during an RTP cycle and the problem is exacerbated by single-side heating, increased processing temperature, and ramp rate. Bentini *et al.* [6] found the strip heater induces much lower thermal stresses than the irradiation of a free wafer. Furthermore, Perkins *et al.* [7] used a nodal analysis to discuss the thermal uniformity and stress minimization during the steady state and transient phase of RTP. Jan and Lin [8] studied lamp configuration design for RTP systems to achieve the necessary temperature uniformity. Lin and Chu [9] presented a systematic inverse-modeling analysis, compared to the purely trial-and-error approach, to determine the incident heat flux over a silicon wafer intuitively to ensure thermal uniformity during processing of the ramp-up and steady phase of RTP. Huang *et al.* [10] obtained the optimal arrangement of lamp rings and measurement locations on the wafer for the control of rapid thermal processor. Their results show that a 42% improvement in temperature uniformity can be achieved using the proposed design procedure.

The temperature nonuniformity and discontinuous manufacture procedure (compared with batch furnace) are two limits to the applicability of the rapid thermal processing. In this work, we aim to provide reliable physical and mathematical models to obtain the temperature distribution and thermal stresses throughout the wafer under rapid thermal processing. The objective of this work is to find the optimum cooling control method in the cooling process, which ensures that material failure does not take place and the required cooling time is minimal.

II. Theoretical Analysis

The physical model of the present study is shown in Fig. 1. The wafer is enclosed in a cylinderical chamber, where the oven is axis-symmetric in geometry and the governing equations are then developed in a cylinderical coordinate system. The wafer thickness is assumed to be thin enough as compared to the radius of the wafer r_o, so we can regard this work as a one-dimensional plane-stress problem, that is, both the temperature T and radial

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C.-K. Chao and S.-Y. Hung are with the Department of Mechanical Engineering, National Taiwan University of Science and Technology, Taipei 106, Taiwan, R.O.C. (e-mail: mailto:ckchao@mail.ntust.edu.tw).

C.-C. Yu is with the Department of Chemical Engineering, National Taiwan University, Taipei, Taiwan 106-17, R.O.C.

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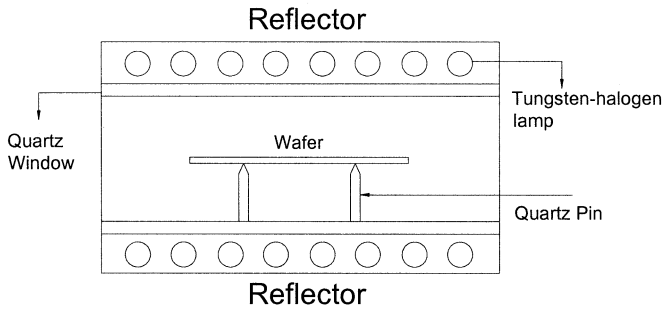

Fig. 1. Physical model of RTP.

displacement u_r are dependent of r only. The partial differential equations of the present thermoelastic problem can be written as [11]

$$k\left(\frac{1}{r}\frac{\partial T}{\partial r}+\frac{\partial^2 T}{\partial r^2}\right)-q^{\mathrm{rad}}-q^{\mathrm{conv}}-\frac{E\alpha T_o}{(1-2\nu)}\frac{\partial}{\partial t}(\varepsilon_{rr}+\varepsilon_{\theta\theta}) =\rho C_p\frac{\partial T}{\partial t} \quad (1)$$

$$\frac{\partial^2 u_r}{\partial r^2}+\frac{1}{r}\frac{\partial u_r}{\partial r}-\frac{u_r}{r^2}-(1+\nu)\,\alpha\frac{\partial T}{\partial r}=\frac{\rho\left(1-\nu^2\right)}{E}\frac{\partial^2 u_r}{\partial t^2} \quad (2)$$

where ρ, C_p, and k are density, specific heat, and thermal conductivity of silicon, respectively. T_o denotes the reference temperature, α the linear thermal expansion coefficient, ν Poisson's ratio and E Young's modulus. q^{rad} and q^{conv} represent the radiative and convective heat flux leaving a wafer surface per unit wafer thickness, respectively.

Since the dilatational strain rate $\partial(\varepsilon_{rr}+\varepsilon_{\theta\theta})/\partial t$ in (1) and the temperature gradient $\partial T/\partial r$ in (2) are responsible for the present coupled thermoelastic system, the solutions T and u_r must proceed simultaneously. The complexity of the coupled thermoelastic problem makes an analytical solution difficult and often beyond reach. In order to make the solution accessible, we first examine the order of the coupling term $E\alpha T_o/(1-2\nu)[\partial(\varepsilon_{rr}+\varepsilon_{\theta\theta})/\partial t]$ compared with other terms. In the present work, the material physical properties of the silicon wafer are given in Table I and the reference temperature is fixed at $T_o=1200$ °C. Table I shows the material physical properties are weakly dependent on temperature between 600 °C and 1200 °C, which can be regarded as temperature-independence constants except for the thermal conductivity and specific heat. For this reason, the material physical properties are taken as the average values but the thermal conductivity and specific heat are considered using the reported data [9].

At the beginning of cooling processes, the radiation term q^{rad} can be approximately estimated by $\sigma\left(T_s^4-T_r^4\right)$, where σ is the Stefan–Boltzmann constant, the temperature of the wafer on the steady-state $T_s=1200$ °C, and the room temperature $T_r=27$ °C. The strain-rate $\partial(\varepsilon_{rr}+\varepsilon_{\theta\theta})/\partial t$ is still only about 10^{-6}/s even though the lamp's power decreases instantaneously to zero, i.e., power off. This amounts to the value of coupling term $E\alpha T_o/(1-2\nu)[\partial(\varepsilon_{rr}+\varepsilon_{\theta\theta})/\partial t]$ being the order of 2×10^3, which is far less than the value of order 2×10^5 for the radiation term q^{rad}. It therefore allows us to discard the coupling term from (1) such that the energy equation for the present transient heat transfer problem becomes uncoupled and the temperature can be solved independently from (1).

TABLE I
MATERIAL PHYSICAL PROPERTIES OF SILICON WAFER

Physical properties	600°C	1200°C	Avg.	Ref.
Thermal conductivity, k (W/m/K)	41	23	32	[9]
Density, ρ (kg/m^3)	2330	2330	2330	[9]
Thermal expansion coefficient, α (/K)	4.2×10^{-6}	4.6×10^{-6}	4.4×10^{-6}	[16]
Specific heat, C_p (J/kg/K)	857	1005	931	[9]
Young's modulus, E (Pa)	2.0×10^{11}	1.9×10^{11}	1.95×10^{11}	[16]
Poisson's ratio, ν	0.18	0.18	0.18	[6]
Emissivity, ε	0.7	0.7	0.7	[9]

A. Temperature Analysis

With the absence of the coupling term $E\alpha T_o/(1-2\nu)[\partial(\varepsilon_{rr}+\varepsilon_{\theta\theta})/\partial t]$, the governing equation (see (1)) of the present transient heat transfer problem can thus be written as

$$k\left(\frac{1}{r}\frac{\partial T}{\partial r}+\frac{\partial^2 T}{\partial r^2}\right)-q^{\mathrm{rad}}-q^{\mathrm{conv}}=\rho C_p\frac{\partial T}{\partial t} \quad (3)$$

with boundary conditions given by

$$\frac{\partial T}{\partial r}=0,\ \text{at } r=0 \quad (4)$$

$$-k\frac{\partial T}{\partial r}=q_{\mathrm{edge}},\ \text{at } r=r_o \quad (5)$$

where the quantity q_{edge} is the heat flux at the wafer edge that includes the heat loss of convection and radiation.

Since no analytical solution is available for the present problem, a numerical solution is sought to this set of equations. The approach used is to divide the wafer and oven into n and m concentric annular elements, respectively. Within each annular element, the wafer temperature or lamp power is assumed to be uniform. In the present study, the lamps are assumed to be a flat black body radiation source, the sidewall is assumed to be adiabatic, and the wafer is assumed to be gray and diffusive. Radiation energy interchange between the oven and the wafer can be evaluated by the following network theory [12]:

$$q_i^{\mathrm{rad}}=\sum_{j=1}^{m}\frac{E_{bi}-E_{bj}}{\frac{1-\varepsilon_i}{\varepsilon_i}+\frac{1}{F_{i-j}}} \quad (6)$$

where F_{i-j} and ε_i are the view factor from the wafer element i to the oven element j and the wafer emissivity, respectively, while E_{bi} and E_{bj} represent the blackbody emissive power of the wafer element i and the oven element j, respectively (Fig. 2).

The wafer is 200 mm (about 8 in) in diameter held by three quartz pins and 24 mm above the bottom of a rapid thermal processing oven that is 560 mm in diameter and 100 mm in height. The convective heat transfer coefficient h_i can be evaluated from an equation experimented by Lord [2]

$$h_i=14.2+8.6\left(\frac{r_i}{r_o}\right)^4\ (\mathrm{W/m^2/^\circ C}) \quad (7)$$

$$h_{\mathrm{edge}}=11.4\ (\mathrm{W/m^2/^\circ C}) \quad (8)$$

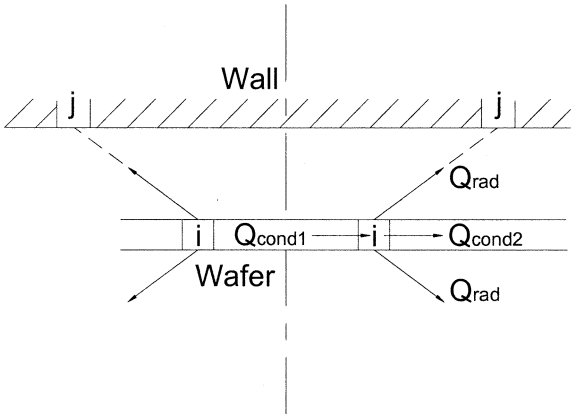

Fig. 2. Schematic representation of energy flux in an Si wafer.

where r_i/r_o denotes the normalized radius and h_{edge} stands for the convective heat transfer coefficient at the edge of the wafer. The convective effect can be represented as

$$q_i^{\text{conv}} = h_i(T_i - T_\infty) \tag{9}$$

with T_∞ being the temperature of the reaction vapor.

We now consider the lamps blackbody emissive power E_{bls} on the steady state. The lamp's power of the oven and the temperature distribution on the wafer are assumed to be uniform, thus the steady-state lamps blackbody emissive power can be written in the form

$$E_{\text{bls}} = E_{\text{bws}} + \frac{1}{A}\left(\frac{1-\varepsilon}{\varepsilon} + \frac{1}{F}\right)\sum_{i=1}^{n} h_i(T_s - T_\infty)A_i \tag{10}$$

where E_{bws} is the steady-state wafer blackbody emissive power, A is the surface area of wafer, and the F is the global view factor from the wafer to the lamps which is found to be 0.925 in this work.

The numerical solution is carried out by using a fully implicit algorithm and computed by marching forward from the initial condition

$$T = T_s, \text{ for all } r \text{ on the wafer at } t = 0. \tag{11}$$

The consistency and convergence of the present numerical solution can be achieved by refining the mesh and time step. Since the nonlinear equations represented above are solved by a linear algorithm, the whole process needs a series of iterations. The convergence of the iterations is defined by

$$\frac{|T_{k+1} - T_k|_{\max}}{|T_{k+1}|_{\max}} < 10^{-6} \tag{12}$$

where the subscript k stands for the number of iterations.

B. Stress Analysis

Once the temperature has been obtained, the displacement u_r can be solved directly from (2). In the present study, the changes of thermal condition are assumed to proceed slowly such that the inertia term $\partial^2 u_r/\partial t^2$ in (2) can be discarded [10]. With this assumption, the displacement u_r can be readily found as

$$u_r = \frac{(1+\nu)\alpha}{r}\int_0^r T(\eta)\eta d\eta + \left[\frac{(1+\nu)\alpha}{r_o^2}\int_0^{r_o} T(\eta)\eta d\eta + \alpha T_o\right] r \tag{13}$$

and the components of stresses are obtained as

$$\sigma_{rr} = \alpha E\left(\frac{1}{r_o^2}\int_0^{r_o} T(\eta)\eta d\eta - \frac{1}{r^2}\int_0^r T(\eta)\eta d\eta\right) \tag{14}$$

$$\sigma_{\theta\theta} = \alpha E\left(-T + \frac{1}{r_o^2}\int_0^{r_o} T(\eta)\eta d\eta + \frac{1}{r^2}\int_0^r T(\eta)\eta d\eta\right) \tag{15}$$

$$\sigma_{r\theta} = 0 \tag{16}$$

where σ_{rr} and $\sigma_{\theta\theta}$ are the radial and tangential stress components, respectively. Since the obtained temperature is expressed in a discrete manner, both the displacement in (13) and the stresses in (14) and (15) are determined by a trapezoidal integration technique.

In the present study, the maximum shear stress failure criterion is used which assumes that the wafer fails in shear when

$$S = \frac{\tau_{\max} \cdot F_s}{\tau_{yp}} > 1 \tag{17}$$

where S is the normalized maximum resolved stress, F_S is the safety factor which is usually taken to be two, and the maximum shear stress is calculated using Mohr's circle as [13]

$$\tau_{\max} = \frac{1}{2}\left|\sigma_{rr} - \sigma_{\theta\theta}\right|. \tag{18}$$

At high temperatures, silicon behaves like a viscous material, the yield stress in shear can be expressed in terms of the temperature and the maximum shear stress rate [2], [5], [14] as

$$\tau_{yp} = 23.17\exp\left(16.1 - 0.00\,916T\right)\left(\frac{d\tau}{dt}\right)^{0.4} \tag{19}$$

where the stress unit is in Pascal and the temperature unit is in degrees Celsius. The stress rate $d\tau/dt$ is taken to be the larger of 2.5×10^5 Pa/s or its calculated value. If the result calculated from (19) exceeds 3.1×10^8 Pa, it is taken to be 3.1×10^8 Pa which means that the wafer is at a low temperature. From (19), we know that the yield shear stress will be about 1.5 MPa when $T = 1200\ ^\circ$C at the beginning of the cooling process which is far less than 310 Mpa at the room temperature $T = 27\ ^\circ$C. This simply indicates that, according to the failure criterion stated in (17), a small temperature nonuniformity may induce material failure at a high temperature.

III. Results and Discussion

Numerical solutions of (3) and (14) and (15) were obtained using a fully implicit finite-difference method and a trapezoidal integration technique, respectively. We first consider the heat transfer effects of convection and radiation to the wafer. From Fig. 3, curve (a) represents the radiative-only cooling with the

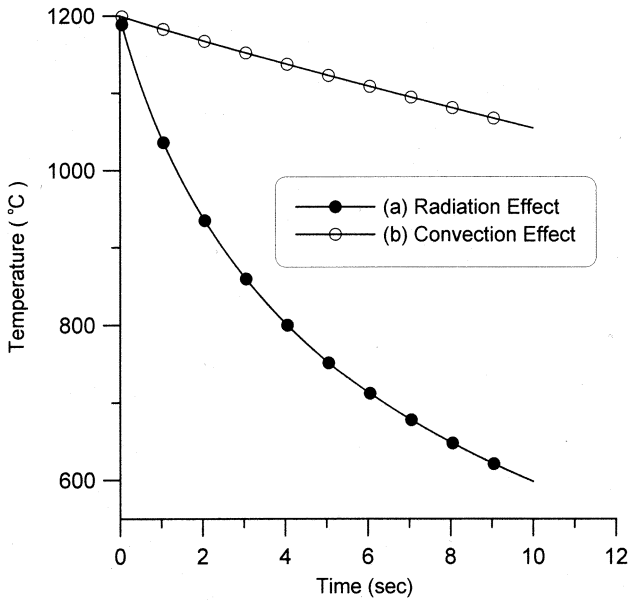

Fig. 3. Convective heat loss is small and negligible compared with radiative heat loss especially at a high temperature.

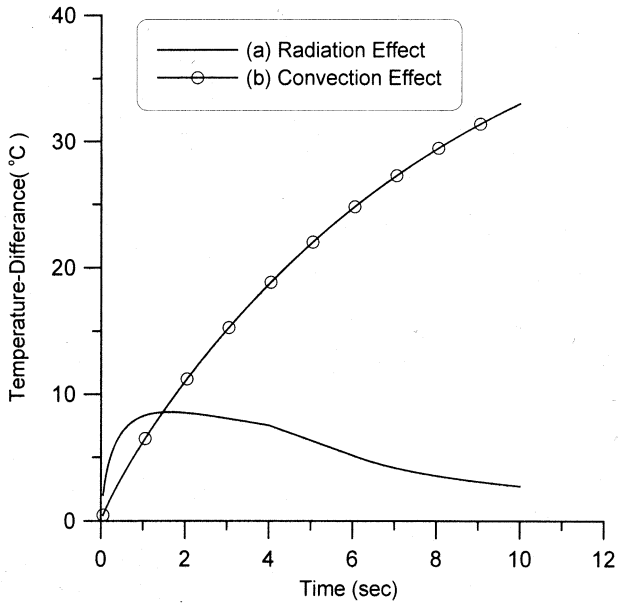

Fig. 4. Radiative heat loss is highly uniform compared with the convective heat loss.

top and bottom of the oven, which are maintained at room temperature (27 °C) while the oven is assumed to be vacuum. Curve (b) represents the convective-only cooling with reaction vapor, which is kept at 27 °C while the top and bottom of the oven are assumed to be adiabatic. At the beginning of cooling processes, we can estimate q^{conv} from (7) and (9), which is about the order of 2×10^4. That is much less than the value of order 2×10^5 for the radiation term q^{rad}. By that reason, the thermal energy of the radiation is proportional to absolute temperature to the fourth power, and the convective heat loss is believed to be small and negligible compared with the radiative heat loss especially at high temperature [2]. Furthermore, the radiative heat loss is found to be highly uniform over the time as compared to the convective heat loss as shown in Fig. 4. Based on the above findings, the convective heat loss may be a major factor in causing temperature variation across the wafer. The phenomenon further suggests that the convective cooling is not a good choice at the beginning of the cooling process, thus the following discussion will not consider the convective effect during the cooling process.

Fig. 5 shows the temperature profile during ramp-down for the radiative-only cooling process. Since the area of heat loss is larger at the edge of the wafer, the temperature drop is expected at the edge of the wafer. On the contrary, the temperature profile at the central region of the wafer is seen to be flatter.

Fig. 6 shows, for the radiative-only cooling process, the tangential stress at the wafer edge is positive due to thermal shrinkage induced by the edge effect. On the other hand, the compressive tangential stress prevails at the central region of wafer. From curve (a) in Fig. 4 and curve (c) in Fig. 6, it is interesting to see that the maximum temperature nonuniformity and the maximum tangential stress occur at the same time ($t = 1.4$ s).

In this work, we consider three different boundary conditions of the oven during the cooling process: 1) the top and bottom of the oven are kept at room temperature (27 °C); 2) the lamp power on the top of the oven decreases gradually and the bottom of the oven is a cold floor maintained at 27 °C; 3) the lamp power on the top and bottom of the oven decrease gradually under a constant cooling-rate control scheme (10 kW/m^2 · s). According to the maximum shear stress criterion stated in (17), material failure is found to take place in cases (a) and (b) at the beginning of cooling processes, whereas the normalized maximum resolved stress is always below one during the cooling process for the case (c) with the constant cooling-rate condition as indicated in Fig. 7. Note the time $t = 0.4$ s at which the maximum resolved stress S takes place, as shown in Fig. 7, which is different from that of $t = 1.4$ s where the maximum tangential stress occurs, as shown in Fig. 4, for the room temperature

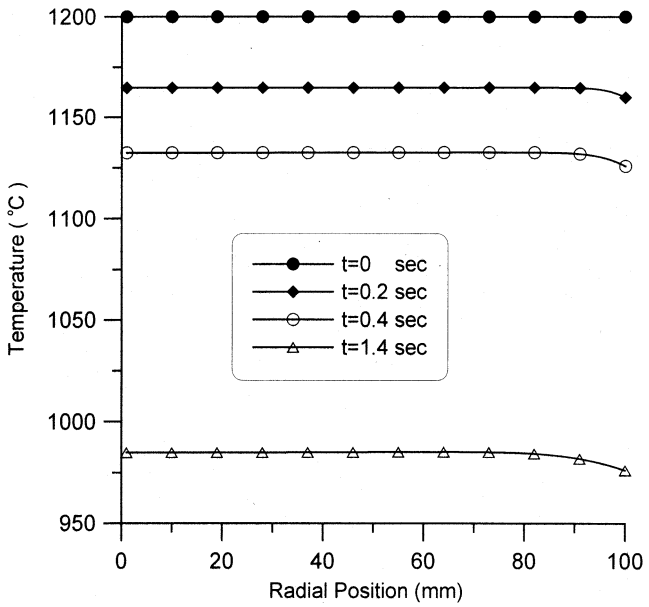

Fig. 5. Temperature profile on the wafer for the room temperature (top and bottom of the oven) cooling condition.

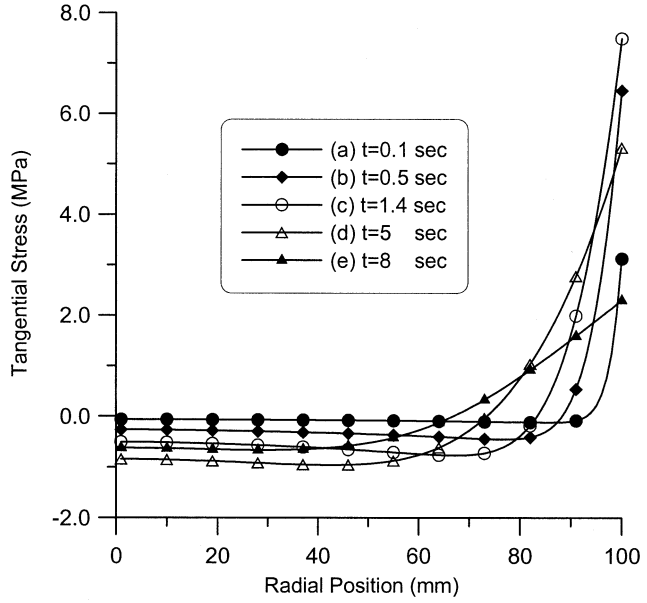

Fig. 6. Tangential stress distribution on wafer for the room temperature (top and bottom of the oven) cooling condition.

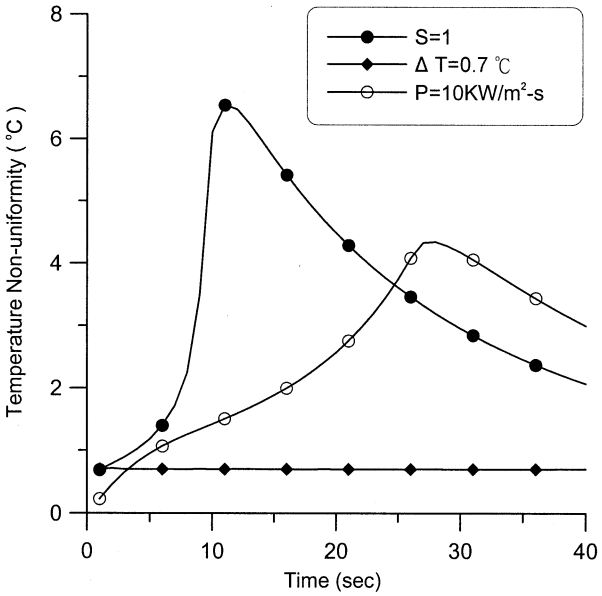

Fig. 8. Variation of the temperature difference during cooling process under three different control schemes.

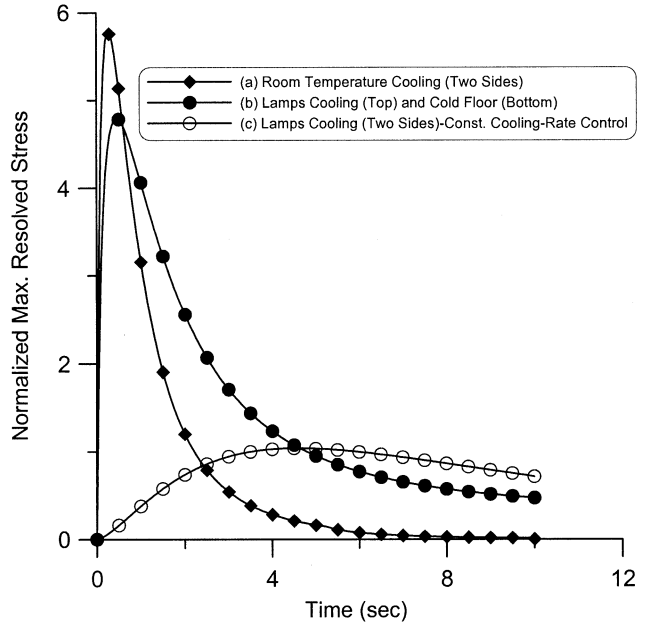

Fig. 7. Variation of the normalized maximum resolved stress at the wafer edge under three different boundary conditions.

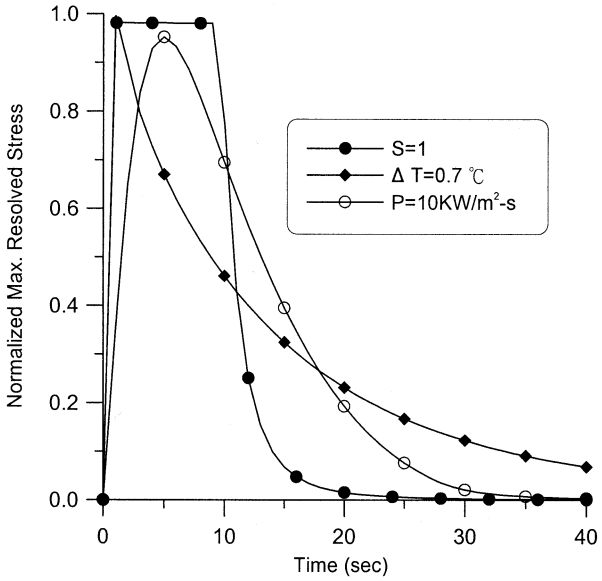

Fig. 9. Variation of the normalized maximum resolved stress at the wafer edge under three different control schemes.

cooling condition. The reason is the yield stress in shear τ_{yp} at $t = 1.4$ s is greater than τ_{yp} at $t = 0.4$ s as indicated in (19).

Next, we consider three different control schemes in the cooling process using the boundary condition that the lamps power on the top and bottom of the oven decrease with various cooling-rate conditions: 1) fixed temperature-difference control scheme—the maximum temperature difference within a wafer maintains constant which is determined to be 0.7°C by trial and error such that the normalized maximum resolved stress is less than one during the cooling process; 2) constant cooling-rate control scheme—the lamp's power decreases gradually at a constant rate which is determined to be 10 kW/m^2 · s by trial and error, which ensures that the normalized maximum resolved stress is less than one during the cooling process; and 3) maximum stress control scheme—the normalized maximum resolved stress is kept close to one until the lamp's power decreases to zero during the cooling process.

Fig. 8 shows the temperature nonuniformity under three different control schemes. It is seen that, initially, the allowable temperature difference is getting larger as time increases until the peaks $t = 10$ s and $t = 27$ s for the maximum stress control and constant cooling-rate control, respectively. This is because the lamp's power reaches zero at $t = 10$ s and $t = 27$ s for the maximum stress control and constant cooling rate control, respectively, as shown in Fig. 10.

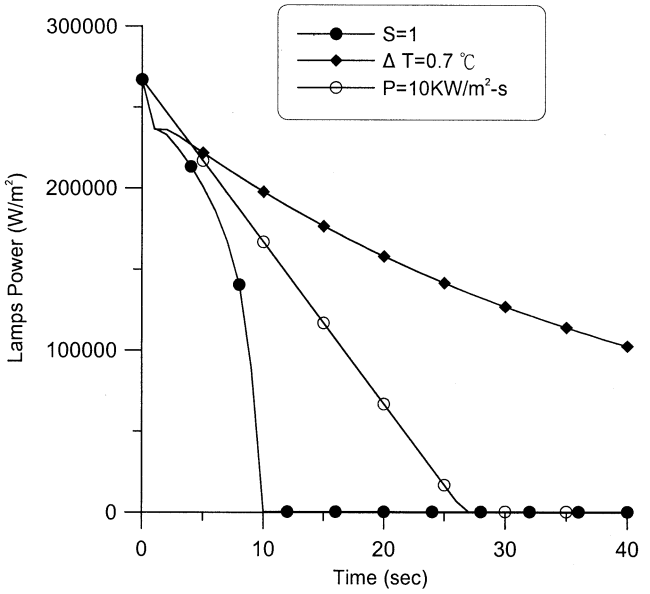

Fig. 10. Variation of the lamp's power under three different control schemes.

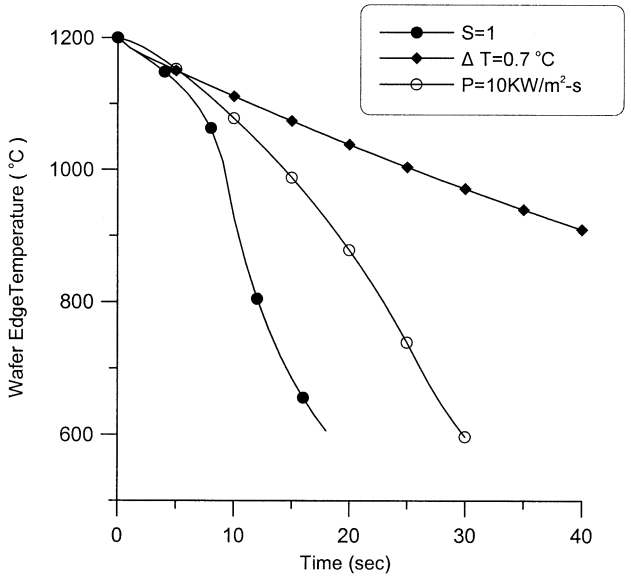

Fig. 11. The temperature variation at wafer edge under three different control schemes.

Fig. 9 shows the corresponding normalized maximum resolved stress for three different control schemes. The normalized maximum resolved stress remains at unity until $t = 10$ s for the maximum stress control scheme. After $t = 10$ s, the lamp's power is down to zero and thus the normalized resolved stress decreases accordingly (Fig. 10) as the result of decreases of the temperature at the wafer edge (e.g., from 900 °C to 600 °C as shown in Fig. 11). It is then suggested that after $t = 10$ s the wafer can be cooled by other more efficient ways, for example convective cooling. Under the constant cooling-rate and fixed temperature-difference control schemes, the normalized maximum resolved stresses reach their the maximum value at $t = 5$ s and $t = 1$ s, respectively, and then the normalized maximum resolved stresses decrease subsequently.

Fig. 10 shows the lamps power decreases dramatically during the first 2 s for both the maximum stress control scheme and the fixed temperature-difference control scheme. After 5 s elapsed, the lamp's power for the fixed temperature-difference control scheme decreases gradually with the rate even smaller than the constant cooling-rate control scheme. This is because the temperature nonuniformity $\Delta T = 0.7$ °C for the fixed temperature-difference control scheme is smallest among the three different control schemes as indicated in Fig. 8. The required cooling time for the maximum stress control scheme is only 18 s from 1200 °C to 600 °C, compared to 30 s for the constant cooling-rate control scheme, and, moreover, it is only one-fifth of the required time for the constant temperature-difference scheme as shown in Fig. 11. From the above discussion, we conclude that the maximum stress control scheme can significantly reduce the required cooling time and thermal budgets compared with other ways. Moreover, this can be achieved by programming the lamp power (e.g., Fig. 10) or setting the temperature according to Fig. 11 for closed-loop control. The results further indicate the inappropriateness of the current linear temperature ramp-down practice.

IV. Conclusion

The temperature and the induced thermal stresses during the cooling process are calculated by the finite-difference method and a trapezoidal integration technique, respectively. It is shown that material failure initiates in the peripheral region of the wafer and the convective effect is a major factor to cause temperature nonuniformity. Therefore, the convective cooling is not a good cooling mechanism in the initial stage during the cooling process. As for the radiative cooling, the temperature nonuniformity is caused by edge effect and geometric relation between the chamber and the wafer. Among the three different boundary conditions, the two sides' (top and bottom) room temperature radiative cooling condition is found to be the worst choice that the maximum S takes place at $t = 0.4$ s which would result in material failure. On the other hand, the two-side lamp's radiative cooling condition is found to be the best choice because the S value is always below one during the cooling process.

In this paper, we compare three control schemes using the lamp's radiative cooling condition. Both the maximum allowed temperature nonuniformity and the maximum stress are predicted. The maximum stress control scheme is found to reduce the required cooling time at most compared with other ways, which promotes reliability and practicability of the rapid thermal processing. This phenomenon is consistent with the result associated with a batch furnace [15]. In this control scheme, the cleaning gas is suggested to flow through the chamber as the lamp's power is down to zero (after 10 s). At this time, the wafer is strong enough to resist the thermal stress due to convection since the temperature is already down to about 900 °C at which the yield stress in shear τ_{yp} is increased accordingly, as indicated in (19).

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Ching-Kong Chao received the B.S. and M.S. degrees in mechanical engineering from National Cheng Kung University, Tainan, Taiwan, R.O.C., and National Taiwan University, Taipei, Taiwan, R.O.C., respectively, and the Ph.D. Degree in mechanical engineering from Lehigh University, Easton, PA, in 1987.

His current research interests include rapid thermal processing, thermoelastic behavior in composite materials, biomechanics, and the mechanics of nonequilibrium phenomena.

Shih-Yu Hung was born on December 17, 1966, in Nantou, Taiwan, R.O.C. He received the M.S. degree in engineering science from National Cheng Kung University, Tainan, Taiwan, R.O.C, in 1993, and is currently working toward the Ph.D. degree in mechanical engineering at National Taiwan University of Science and Technology, Taipei, Taiwan, R.O.C.

Since 1993, he has been an Instructor with Nan Kai College, Nantou, Taiwan, R.O.C. His current research interests include devices design and simulation for RTP equipment and the vertical Bridgman furnace.

Cheng-Ching Yu received the B.S. degree from Tunghai University, Taichung, Taiwan, R.O.C., in 1979, and the M.S. and Ph.D. degrees from Lehigh University, Easton, PA, in 1982 and 1986, respectively, all in chemical engineering.

Since 1986, he has been with the National Taiwan University of Science and Technology, Taipei, Taiwan, R.O.C., for 16 years. Currently, he is a Professor of chemical engineering at National Taiwan University, Taipei, Taiwan, R.O.C. His current research interests include multivariable control, plantwide control, control of microelectronic processes, and reactive distillation. He is the author of *Autotuning of PID Controllers* (New York: Springer-Verlag, 1999).

Dr. Yu received the Young Investigator Award from the Chinese Institute of Chemical Engineers, and the Outstanding Research Awards from the National Science Council of Taiwan. He is on the editorial board of the *J. Chinese Institute Chemical Engineering*.