Semicond. Sci. Technol. **22** (2007) 884–889 doi:10.1088/0268-1242/22/8/010

# Charge trapping characteristics of atomic-layer-deposited $HfO_2$ films with $Al_2O_3$ as a blocking oxide for high-density non-volatile memory device applications

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Received 10 January 2007, in final form 7 June 2007
Published 29 June 2007
Online at stacks.iop.org/SST/22/884

**Abstract**
Charge trapping characteristics of high-relative permittivity (high-$\kappa$) $HfO_2$ films with $Al_2O_3$ as a blocking oxide in p-Si/$SiO_2$/$HfO_2$/$Al_2O_3$/metal memory structures have been investigated. All high-$\kappa$ films have been grown by atomic layer deposition. A transmission electron microscope image shows that the $HfO_2$ film is polycrystalline, while the $Al_2O_3$ film is partially crystalline after a high temperature annealing treatment at 1000 °C for 10 s in $N_2$ ambient. A well-behaved counter-clockwise capacitance–voltage hysteresis has been observed for all memory capacitors. A large memory window of ~7.4 V and a high charge trapping density of $\sim 1.1 \times 10^{13}$ $cm^{-2}$ have been observed for high-$\kappa$ $HfO_2$ charge trapping memory capacitors. The memory window and charge trapping density can be increased with increasing thickness of the $HfO_2$ film. The charge loss can be decreased using a thick trapping layer or thick tunnelling oxide. A high work function metal gate electrode shows low charge loss and large memory window after 10 years of retention. High-$\kappa$ $HfO_2$ memory devices with high-$\kappa$ $Al_2O_3$ as a blocking oxide and a high work function metal gate can be used in future high-density non-volatile memory device applications.

(Some figures in this article are in colour only in the electronic version)

## 1. Introduction

High-relative permittivity (high-$\kappa$) charge trapping layers in poly-Si/$SiO_2$/high-$\kappa$/$SiO_2$/Si (SOHOS) memory structure are of increasing interest for charge storage non-volatile memory (NVM) device applications [1–8]. Memory devices with nano-crystals have been reported by several groups [9–17], but they have a uniformity problem. A single quantum well ($HfO_2$/$TiO_2$/$Al_2O_3$) memory capacitor with a small memory window (~1.6 V) has also been reported [18]. Silicon-nitride ($Si_3N_4$) charge trapping layers in a poly-Si/$SiO_2$/$Si_3N_4$/$SiO_2$/Si (SONOS) memory structure have been studied extensively with poor retention and scaling issue [19, 20]. The high-$\kappa$ film as a charge trapping layer should be used in the SONOS structure to improve the program/erase speed, vertical scaling and charge retention characteristics [21–23]. To further improve the vertical scaling and charge retention characteristics of non-volatile memory devices, the high-$\kappa$ materials with a large barrier height, such

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**Table 1.** The growth and capacitance–voltage (*C–V*) hysteresis window of all memory capacitors with an Al gate electrode.

| Memory capacitors | $SiO_2$ (nm) | $HfO_2$ (nm) | $Al_2O_3$ (nm) | Memory window $V_g - V_{FBN} = \pm 15$ V |
|---|---|---|---|---|
| S1 | 3 | 5 | 10 | ~7.0 V |
| S2 | 3 | 10 | 10 | ~7.4 V |
| S3 | 4 | 5 | 10 | ~6.0 V |

as $Al_2O_3$ films, are interesting alternatives as a blocking oxide [21–24]. To obtain high-performance non-volatile memory devices, a high work function metal gate electrode in a metal/$Al_2O_3$/$HfO_2$/$SiO_2$/Si (MAHOS) memory structure has been studied for a new generation of memory technology. In this paper, charge trapping characteristics of atomic-layer-deposited high-$\kappa$ $HfO_2$ films with high-$\kappa$ $Al_2O_3$ as a blocking oxide and a high work function metal gate (Pt) on $SiO_2$/p-Si substrates in the MAHOS memory structure have been investigated.

## 2. Experimental details

High-$\kappa$ $HfO_2$ and $Al_2O_3$ films were deposited on p-type silicon (1 0 0) substrates with a resistivity of 15–25 Ω cm by atomic layer deposition (ALD) using hafnium tetra-chloride ($HfCl_4$) and tri-methylaluminium ($Al(CH_3)_3$) precursors at a substrate temperature of 300 °C. The precursor temperatures were 185 °C for $HfCl_4$ and 23 °C for $Al(CH_3)_3$. Prior to deposition of high-$\kappa$ $HfO_2$ and $Al_2O_3$ films, the p-Si substrate was cleaned by dipping in dilute HF for 1 min using the Radio Corporation of America (RCA) process to remove native oxide from the surface. Then, tunnelling oxides ($SiO_2$) with thicknesses of 3 nm–4 nm were grown by a rapid thermal oxide (RTO) system with a temperature of 1000 °C for 20–60 s. High-$\kappa$ $Al_2O_3$ films as a blocking oxide were used for all memory capacitors. After deposition of high-$\kappa$ films, a post-deposition annealing (PDA) was carried out at 1000 °C for 10 s in $N_2$ ambient. Table 1 shows all high-$\kappa$ memory capacitor structures. After deposition of an aluminium (Al) or platinum (Pt) gate electrode (gate area: $3.14 \times 10^{-4}$ cm$^2$), post-metal annealing with a temperature of 400 °C for 5 min was done using forming gas [$N_2$(90%) + $H_2$(10%)]. To probe the thickness and microstructure of high-$\kappa$ $HfO_2$ memory capacitors, high-resolution transmission electron microscopy (HRTEM) was performed using a JEM 3000F field emission system with an operating voltage of 300 kV and a resolution of 0.17 nm. Electrical properties such as high-frequency (100 kHz) capacitance–voltage, current–voltage, charge loss and retention of all memory capacitors were carried out using HP 4284A LCR meter and HP4156B semiconductor analyser systems.

## 3. Results and discussion

Figure 1 shows the typical HRTEM image of a p-Si/$SiO_2$/$HfO_2$/$Al_2O_3$/Al memory structure (S3). Excellent interfaces of p-Si/$SiO_2$, $SiO_2$/$HfO_2$, $HfO_2$/$Al_2O_3$ and $Al_2O_3$/Al have been observed. Thicknesses of tunnelling oxide ($SiO_2$), high-$\kappa$ trapping layer ($HfO_2$) and high-$\kappa$ blocking oxide ($Al_2O_3$)

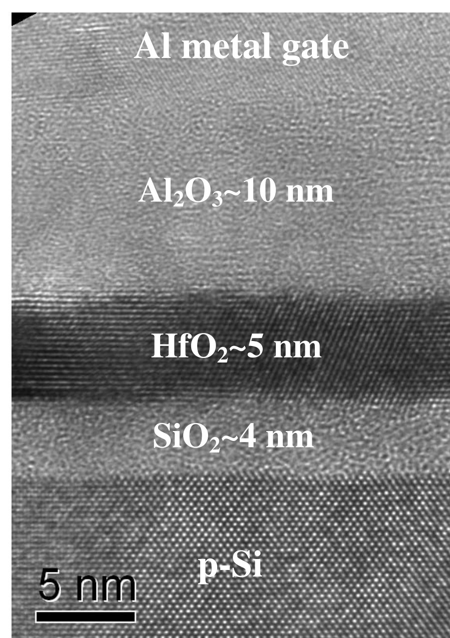


**Figure 1.** A typical high-resolution transmission electron microscope (HRTEM) image of a high-$\kappa$ $HfO_2$ charge trapping layer with high-$\kappa$ $Al_2O_3$ as a blocking oxide for the memory capacitor (S3).

are found to be ~4 nm, ~5 nm and ~10 nm, respectively. It is observed that the $HfO_2$ film shows polycrystalline, while the $Al_2O_3$ film as a blocking oxide shows almost amorphous after a high temperature annealing treatment (~1000 °C, 10 s) in $N_2$ ambient. It is also investigated that the high-$\kappa$ $Al_2O_3$ film as a blocking oxide has a great impact to enhance the electron injection from the Si substrate under the program condition and to enhance the hole injection under the erase condition of memory capacitors, and it has been explained by a schematic energy band diagram as shown in figure 2. The program and erase conditions are used positive and negative gate voltages, respectively. Under positive gate voltage, the electrons can be tunnelled from the Si substrate and captured by the traps in the $HfO_2$ films. The trapped electrons in the $HfO_2$ films will create an electric field distribution to inhibit electron injection. Under the programming condition, the flat-band voltage shift ($\Delta V_{FB}$) can be related to the charge transfer through the corresponding charge centroids [25] in the $HfO_2$ films by the following relation

$$\Delta V_{FB} = \frac{Q_{HfO_2}}{\varepsilon_o}\left[\frac{x_{BO}}{\varepsilon_{BO}} + \frac{x_{HfO_2}}{\varepsilon_{HfO_2}}\right], \quad (1)$$

where $Q_{HfO_2}$ is the amount of trapped charges per unit area in $HfO_2$ films. The $\varepsilon_{HfO_2}$ and $\varepsilon_{BO}$ are relative permittivities of the trapping oxide ($HfO_2$) and the blocking oxide ($Al_2O_3$), respectively. The $x_{HfO_2}$ and $x_{BO}$ are thicknesses of the trapping oxide ($HfO_2$) and the blocking oxide ($Al_2O_3$), respectively. The $\varepsilon_o$ is the permittivity of free space. The charge centroids can be measured from the tunnelling oxide ($SiO_2$)/high-$\kappa$ $HfO_2$ interface. Assuming a uniform trap distribution in the high-$\kappa$ $HfO_2$ films, the charge centroid will be approached half the $HfO_2$ film thickness and the flat band voltage shift can be

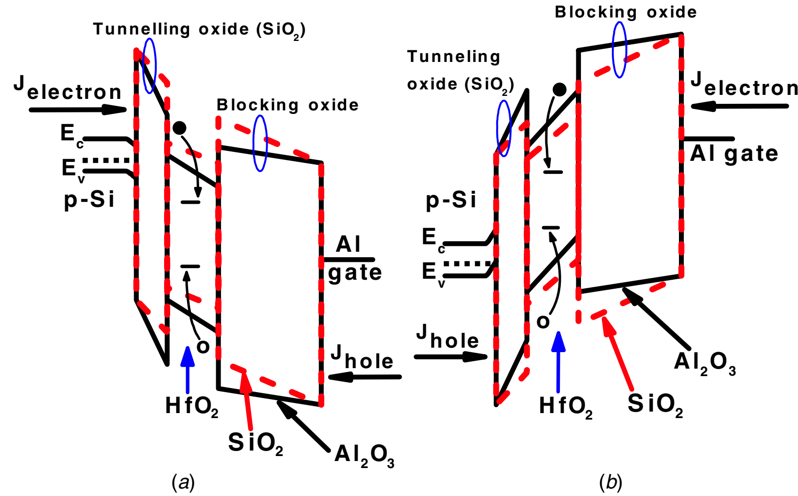


**Figure 2.** Schematic energy band diagrams of p-Si/$SiO_2$/$HfO_2$/$Al_2O_3$/Al (solid line) and p-Si/$SiO_2$/$HfO_2$/$SiO_2$/Al (dash line) memory structures under (*a*) program and (*b*) erase modes.

simplified as

$$\Delta V_{FB} = \frac{Q_{HfO_2}}{\varepsilon_o}\left[\frac{x_{BO}}{\varepsilon_{BO}} + \frac{x_{HfO_2}}{2\varepsilon_{HfO_2}}\right]. \tag{2}$$

The capacitance-equivalent thickness (CET) of $SiO_2$/$HfO_2$/$Al_2O_3$ stack dielectrics can be written as

$$x_{eff} = x_{TO} + \frac{\varepsilon_{TO}}{\varepsilon_{HfO_2}} x_{HfO_2} + \frac{\varepsilon_{TO}}{\varepsilon_{BO}} x_{BO}, \tag{3}$$

where $\varepsilon_{TO}$ is the relative permittivity and $x_{TO}$ is the thickness of tunnelling oxide ($SiO_2$). The electric fields across tunnelling oxide ($E_{TO}$) and blocking oxide ($E_{BO}$) under an erase mode [24] can be explained by the following equations:

$$E_{TO} = \frac{|V_g| - \phi_{ms} - \phi_s - \Delta V_{FB}}{x_{eff}}, \tag{4}$$

$$E_{BO} = \left[E_{TO} + \frac{Q_{HfO_2}}{\varepsilon_o \cdot \varepsilon_{TO}}\right] \cdot \frac{\varepsilon_{TO}}{\varepsilon_{BO}}, \tag{5}$$

where $V_g$ is the applied gate voltage, $\phi_{ms}$ is the work function difference between the gate electrode and p-Si substrate, and $\phi_s$ is the surface potential. Relative permittivities of $HfO_2$ and $Al_2O_3$ films are found to be ~17 and ~8, respectively, after a high temperature annealing treatment at ~1000 °C for 10 s in $N_2$ ambient. Assuming the permittivity of ~3.9 of $SiO_2$, relative permittivities of pure $HfO_2$ and $Al_2O_3$ films are calculated using p-Si/$SiO_2$(3 nm)/$HfO_2$(10 nm)/Al and p-Si/$SiO_2$(3 nm)/$Al_2O_3$(10 nm)/Al stack capacitor structures, respectively, with the series capacitance method [26]. The high-frequency (100 kHz) capacitance is used to calculate the relative permittivity. Using those relative permittivity values in the above equations and applying the $V_g = 15$ V, the electric field across tunnelling oxide ($E_{TO}$) is ~14 MV $cm^{-1}$ and the electric field across blocking oxide ($E_{BO}$) is ~7.7 MV $cm^{-1}$ for the high-$\kappa$ $Al_2O_3$ blocking oxide, while the $E_{TO}$ is ~8.3 MV $cm^{-1}$ and the $E_{BO}$ is ~10 MV $cm^{-1}$ for the $SiO_2$ blocking oxide. It is noted that the electric field across tunnelling oxide is very high and electric field across blocking oxide is very small if one can use the $Al_2O_3$ as a blocking oxide instead of $SiO_2$ as a blocking oxide. The larger relative permittivity of a trapping layer ($HfO_2$) and blocking oxide ($Al_2O_3$) leads to larger difference of $E_{TO}$ and $E_{BO}$. The calculated energy band diagram on p-Si/$SiO_2$/$HfO_2$/$Al_2O_3$/Al (solid line) and p-Si/$SiO_2$/$HfO_2$/$SiO_2$/Al (dash line) structures under the program/erase mode is shown in figure 2. Under the program mode, electron current ($J_{electron}$) from the Si conduction layer can be enhanced and hole current ($J_{hole}$) from the gate electrode can be suppressed using high-$\kappa$ $Al_2O_3$ as a blocking oxide. Under the erase mode, the $J_{hole}$ from the Si conduction layer can be enhanced and the electron current from the gate electrode can be suppressed using high-$\kappa$ $Al_2O_3$ as a blocking oxide. To get a high program/erase speed, the difference $J_{electron} - J_{hole}$ should be increased. It is important to note that the back tunnelling currents ($J_{hole}$ under program mode and $J_{electron}$ under erase mode) can be suppressed using a large barrier height and large relative permittivity of the high-$\kappa$ blocking oxide. It is also observed that the high-$\kappa$ $HfO_2$ layer can not only improve charge trapping properties but also can improve the program/erase speed and device scaling. Due to the advantage of the high-$\kappa$ $Al_2O_3$ as a blocking oxide, memory characteristics of the p-Si/$SiO_2$/$HfO_2$/$Al_2O_3$/Al (or Pt gate electrode) structures have been investigated in this study.

A well-behaved high-frequency (100 kHz) counter-clockwise capacitance–voltage (*C*–*V*) hysteresis of a memory capacitor (S2) has been observed with different sweeping gate voltages (figure 3). The counter-clockwise *C*–*V* hysteresis of p-Si/$SiO_2$/$HfO_2$/$Al_2O_3$/Al memory capacitors confirms that the electrons can be injected from the Si substrate to the $HfO_2$ trapping layer under positive gate voltage and the holes can be injected from the Si substrate to the $HfO_2$ trapping layer under negative gate voltage. A quasi-neutral capacitance–voltage (*C*–*V*) curve (i.e., no charging up or discharging the memory capacitor) has been obtained with the application of a small sweeping gate voltage ($V_g \sim \pm 3$ V). The sweeping gate voltage step was 0.1 V $s^{-1}$ during the *C*–*V* measurement for all memory capacitors. The quasi-neutral flat-band voltage ($V_{FBN}$) is shown in figure 3. A large memory window of $\Delta V \approx 7.4$ V has been observed under a sweeping gate voltage of $V_g \approx \pm 15$ V, and it can be used in multi-level charge

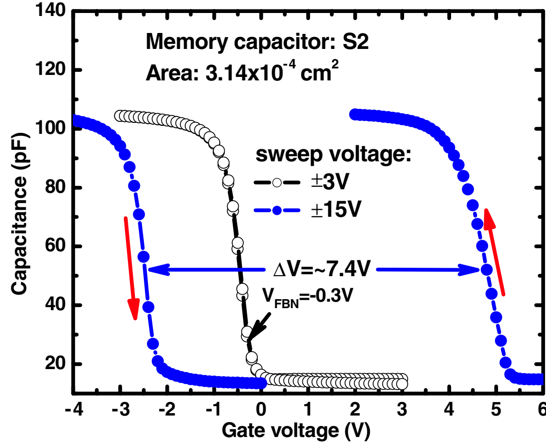


**Figure 3.** Capacitance versus gate voltage characteristic of the high-$\kappa$ $HfO_2$ memory capacitor (S2).

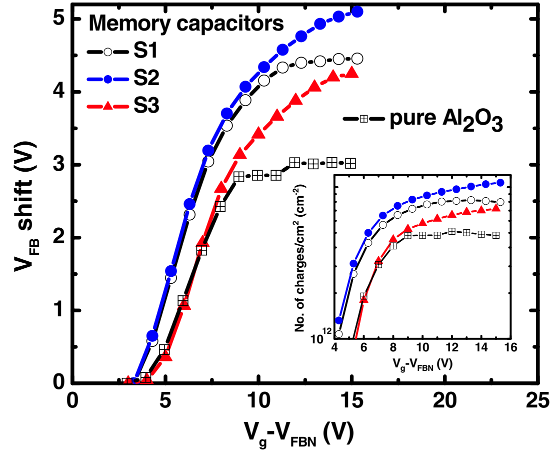


**Figure 4.** Flat-band voltage ($V_{FB}$) shift versus gate drive voltage ($V_g - V_{FBN}$) for all high-$\kappa$ $HfO_2$ charge trapping memory capacitors. The charge trapping density of all memory capacitors has been shown in the inset. The $V_{FB}$ shift and charge trapping density of an $Al_2O_3$ charge trapping memory capacitor have been plotted for comparison.

(MLC) storage memory device applications. The capacitance-equivalent thicknesses are found to be ~9.2 nm for S1, ~10.3 nm for S2 and ~11.2 nm for S3 memory capacitors. The capacitance density of >3.0 fF $\mu m^{-2}$ is high enough to scaling the device. According to industrial technology roadmap on semiconductor (ITRS), the thicknesses are needed to be 3 nm for tunnelling oxide ($SiO_2$), 4 nm for the silicon-nitride ($Si_3N_4$) trapping layer and 4 nm for blocking oxide ($SiO_2$) for 45 nm technology node in the SONOS flash memory device. So, the total thickness of the SONOS flash memory is 11 nm. Furthermore, the SONOS memory device cannot be scaled below the 45 nm technology node, and one of the reasons is the high leakage current. Our memory device shows the small CET of 9.2 nm with a low leakage current because of thick high-$\kappa$ $HfO_2$ as a trapping layer and the high-$\kappa$ $Al_2O_3$ as a blocking oxide. It is believed that our memory device can be used below the 45 nm technology node.

Figure 4 shows the flat-band voltage shift ($V_{FB}$) versus drive gate voltage ($V_g - V_{FBN}$). The $V_{FB}$ shift has been measured with respect to the $V_{FB}$ of quasi-neutral *C–V* curve ($V_{FBN}$). The $V_{FB}$ shift increases with increasing the drive gate voltage. The $V_{FB}$ shifts at $V_g - V_{FBN} \approx +15$ V are found to be ~4.4 V for S1, ~5.1 V for S2, ~4.2 V for S3 and ~3.0 V for pure $Al_2O_3$ charge trapping layers. A pure $Al_2O_3$ charge trapping layer in the p-Si/$SiO_2$ (3 nm thick)/$Al_2O_3$ (15 nm thick)/Al structure has been used for comparison (figure 4). The $V_{FB}$ shift of all $HfO_2$ charge trapping layers is higher than that of the pure $Al_2O_3$ charge trapping layer and it can be explained as follows. Conduction band offset $[\Delta E_c \approx (E_c)_{HfO_2} - (E_c)_{Si}]$ and valence band offset $[\Delta E_v \approx (E_v)_{Si} - (E_v)_{HfO_2}]$ of the $HfO_2$ films with respect to the Si substrate are found to be ~1.7 eV and ~3.1 eV, respectively, and those values of the pure $Al_2O_3$ films are found to be ~2.8 eV and ~4.9 eV, respectively. It indicates that more electrons or holes from the Si substrate can be injected into the $HfO_2$ films rather than the $Al_2O_3$ films because Fowler–Nordheim (FN) tunnelling current has been dominated at the same gate voltage. The $V_{FB}$ shifts are found to be ~1.2 V for the $HfO_2$ film (S1) and ~0.5 V for the pure $Al_2O_3$ films under the same drive gate voltage (+5 V), suggesting that the FN tunnelling current from the Si substrate to the $HfO_2$ trapping layer is higher than that of the pure $Al_2O_3$ films. The valence band offset and conduction band offset of all memory structures have been measured by ultra-violet photoelectron spectroscopy (not shown here). The memory window and the $V_{FB}$ shift of all $HfO_2$ memory capacitors are higher than that of the pure $Al_2O_3$ film, due to higher charge trapping sites and higher charge trapping density in the $HfO_2$ film [21]. A thicker $HfO_2$ film (~10 nm) has a larger memory window than that of a thin (~5 nm) $HfO_2$ film (table 1), due to high charge trapping density of the thicker $HfO_2$ film (inset of figure 4). The charge trapping density for all memory capacitors is calculated using this equation,

$$N_{charge} = \Delta V_{FB} \cdot C_{ox}, \tag{6}$$

where $C_{ox}$ is the total oxide capacitance per unit area. A high charge trapping density of $\sim 1.1 \times 10^{13}$ cm$^{-2}$ has been observed for a high-$\kappa$ memory capacitor, indicating that the high-$\kappa$ $HfO_2$ charge rapping layer shows promise for application.

Erasing characteristics for all memory capacitors are shown in figure 5. Erasing drive voltages ($V_g - V_{FBN}$) with an Al gate electrode are found to be −10.0 V for S1, −10.5 V for S2 and −11.7 V for S3 memory capacitors. A large erasing voltage is necessary for all memory capacitors, due to large valance band offset (~3.1 eV) and small amount of hole injection from the Si substrate. The memory capacitor (S3) has a large erase voltage (−11.7 V), due to the thicker tunnelling oxide (~4 nm) and lower tunnelling probability of holes from the Si substrate into the high-$\kappa$ charge trapping layers. The erasing voltage of the S1 memory capacitor with a Pt gate is −8.3 V. It is observed that the work function is ~4.1 eV for the Al gate and ~5.2 eV for the Pt gate. The erasing voltage can be drastically decreased with a high work function metal gate (Pt), due to lower leakage current from the gate electrode. Figure 6 shows the leakage current of the high-$\kappa$ $HfO_2$ memory capacitor (S1). The gate leakage current is lower for a high work function metal gate and the memory capacitor can be operated up to the gate voltage of

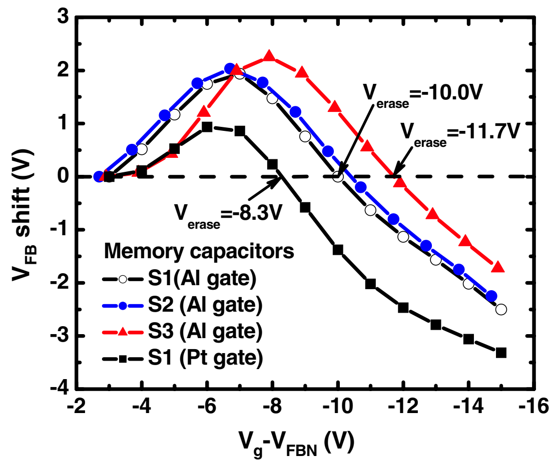


**Figure 5.** Erasing characteristics of all high-$\kappa$ $HfO_2$ memory capacitors with Al and Pt metal gates.

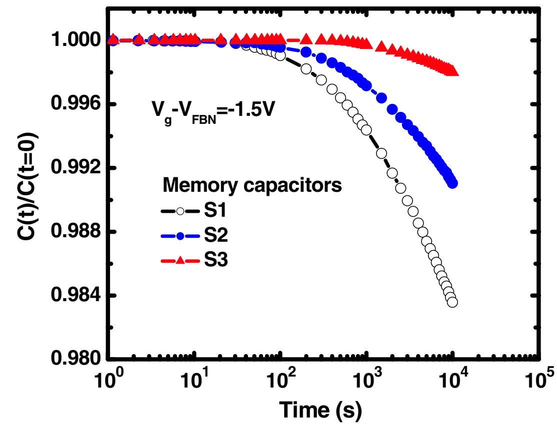


**Figure 7.** Capacitance versus elapsed time of all high-$\kappa$ $HfO_2$ charge trapping memory capacitors.

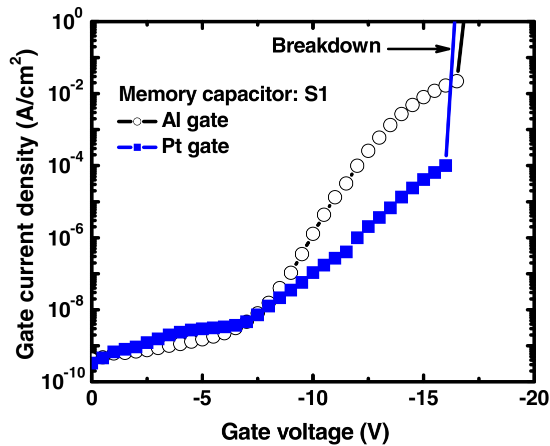


**Figure 6.** Leakage current characteristics of the memory capacitor (S1) with Al and Pt gate electrodes.

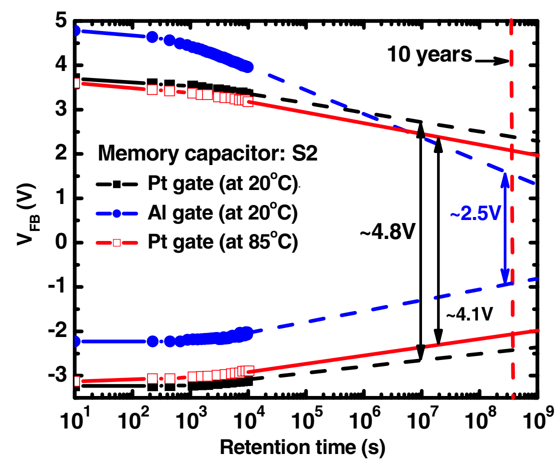


**Figure 8.** Retention characteristics of the high-$\kappa$ $HfO_2$ memory capacitor (S2) with Al and Pt gate electrodes.

$\sim$16 V because of the high breakdown voltage of $<-16$ V. It is noted that a low backward tunnelling current, thin tunnelling oxide and small valence band offset between the trapping layer and Si substrate are necessary for easy erasing of memory devices.

Normalized capacitances versus time have been shown in figure 7. To investigate the charge loss, all memory devices are programmed using $V_g - V_{FBN} = +6$ V for 60 s. Then, the capacitance has been measured at a gate voltage of $V_g - V_{FBN} = -1.5$ V. A constant gate voltage of $V_g - V_{FBN} = -1.5$ V has been applied to the gate electrode at all times during the capacitance measurement. The memory capacitor (S1) with a thin ($\sim$5 nm) $HfO_2$ charge trapping layer shows a large charge loss as compared with a thick ($\sim$10 nm) charge trapping layer (S2). The memory capacitor (S3) shows a negligible charge loss as compared with those of other memory capacitors, due to low probability of charge loss through thick tunnelling oxide ($\sim$4 nm). The impact of the metal gate electrode on the memory window after 10 years of retention has been shown in figure 8. At first, the memory capacitors (S2) are programmed under a drive gate voltage of +15 V for 10 s. Then, the $V_{FB}$ has been measured with time. The memory capacitor has been grounded during $V_{FB}$ measurement. Similarly, the memory capacitors (S2) are erased under a drive gate voltage of $-15$ V for 10 s and the $V_{FB}$ is measured with time. Assuming the logarithmic behaviour for retention, the extrapolation of $V_{FB}$ shift for all memory capacitors has been performed up to 10 years. Memory windows of the Al and Pt gate electrodes are estimated to be $\sim$2.5 V and $\sim$4.8 V at 20 °C after 10 years of retention. The memory window of the Pt gate is $\sim$4.1 V at 85 °C after 10 years of retention. An excellent retention has been observed by the Pt gate electrode, due to the low leakage current of the memory capacitors (figure 6). Charge losses of the Al and Pt gate electrodes are estimated to be $\sim$60% and $\sim$31%, respectively, after 10 years of retention. The charge loss of the memory capacitor (S2) with a Pt gate electrode increases (slightly) $\sim$39% at 85 °C after 10 years of retention. She *et al* [27] reported that the charge loss of $HfO_2$ charge trapping memory devices is higher $\sim$56% at 85 °C after 10 years of retention. Due to the large memory window and low charge loss of the high-$\kappa$ $HfO_2$ charge trapping memory device with high-$\kappa$ $Al_2O_3$ as a blocking oxide and a high work function metal gate, it can be used in future high-density and scaled flash memory device applications.

## 4. Conclusion

Charge trapping characteristics of the high-$\kappa$ $HfO_2$ charge trapping memory capacitors with high-$\kappa$ $Al_2O_3$ as a blocking oxide have been investigated. They show a high charge trapping density, large memory window, low charge loss and small equivalent oxide thickness. The high-$\kappa$ memory devices with a high work function metal gate show promise for future scaled high-density flash memory device applications.

## References


[1] Choi S, Cho M, Hwang H and Kim J W 2003 *Appl. Phys. Lett.* **94** 5408

[2] Sugizaki T, Kobayashi M, Ishidao M, Minakata H, Yamaguchi M, Tamura Y, Sugiyama Y, Nakanishi T and Tanaka H 2003 *Symp. on VLSI Tech. Dig.* p 27

[3] Tan T N, Chim W K, Choi W K, Joo M S, Ng T H and Cho B J 2004 *IEDM Tech. Dig.* p 889

[4] Specht S, Reisinger H, Hofmann F, Schulz T, Landgraf E, Luyken R J, Rosner W, Grieb M and Risch L 2005 *Solid-State Electron.* **49** 716

[5] Lee C H, Hur S H, Shin Y C, Choi J H, Park D G and Kim K 2005 *Appl. Phys. Lett.* **86** 152908

[6] Lin Y H, Yang T Y, Chien C H and Lei T F 2006 *SSDM: Ext. Abstr. Solid State Devices and Materials* p 558

[7] Joo M S *et al* 2006 *SSDM: Ext. Abstr. Solid State Devices and Materials* p 982

[8] Lai C H *et al* 2006 *Symp. on VLSI Tech. Dig.* p 54

[9] Tiwari *et al* 1996 *Appl. Phys. Lett.* **68** 1377

[10] Das K *et al* 2004 *Appl. Phys. Lett.* **84** 1386

[11] Wang S *et al* 2005 *Appl. Phys. Lett.* **86** 113105

[12] Samanta S K *et al* 2005 *IEDM Tech. Dig.* p 177

[13] Lee J J *et al* 2005 *IEEE Trans. Electron. Devices* **52** 507

[14] Wang Y Q *et al* 2005 *IEDM Tech. Dig.* p 169

[15] Choi S *et al* 2005 *IEDM Tech. Dig.* p 173

[16] Ahn Y J *et al* 2006 *Symp. on VLSI Tech. Dig.* p 109

[17] Yin C K *et al* 2006 *SSDM: Ext. Abstr. Solid State Devices and Materials* p 994

[18] Maikap S *et al* 2006 *Ext. Abstr. Solid State Devices and Materials* p 582

[19] Hwang J R *et al* 2005 *IEDM Tech. Dig.* p 161

[20] Du P Y and Guo J C 2006 *SSDM: Ext. Abstr. Solid State Devices and Materials* p 986

[21] Maikap S *et al* 2006 *VLSI-TSA : Proc. Int. Symp. VLSI Tech., Sys., and Appl.* p 36

[22] Maikap S *et al* 2006 *SNDT : Symp. on Nano Device Technology (Taiwan)* p 16

[23] Maikap S *et al* 2006 *SSDM: Ext. Abstr. Solid State Devices and Materials* p 984

[24] Lee C H, Hur S H, Shin Y C, Choi J H, Park D G and Kim K 2005 *Appl. Phys. Lett.* **86** 152908

[25] Bu J and White M H 2001 *Solid-State Electron.* **45** 47

[26] Mahapatra R, Maikap S, Lee J H and Ray S K 2006 *J. Appl. Phys.* **100** 034105

[27] She M, Takeuchi H and King T J 2003 *19th Non-Volatile Semiconductor Memory Workshop* p 53