Single-electron transistors and memory cells with Au colloidal islands

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In this study, single-electron transistors and memory cells with Au colloidal islands linked by C_{60} derivatives have been fabricated by hybridization of top–down advanced electron-beam lithography and bottom–up nanophased-material synthesis techniques. Low-temperature transport measurements exhibit clear Coulomb-blockade-type current–voltage characteristics and hysteretic-type gate-modulated current. The hysteresis is attributed to the presence of electrically isolated charge–storage islands. With the guidance provided by Monte Carlo simulation, we propose a circuit model and give an estimate of the sample parameters. © *2002 American Institute of Physics.* [DOI: 10.1063/1.1527236]

The single-electron transistor (SET) is a potential candidate for the next generation of electronic devices because of its great advantages in low power consumption and high packing density. Since the operating temperature of a SET is determined solely by the geometrical size of the island that should be as small as only a few nanometers, it presents a challenge to the modern nanofabrication technology. Even with the present day state-of-the-art electron-beam lithography technology, this is still a very demanding requirement. On the contrary, nanostructured materials with a critical dimension smaller than a few nanometers can be created through the control of matter at the level of atoms and molecules, but electrical contact to these materials is not at all trivial. Combining advanced electron-beam lithography and nanophased-material synthesis techniques, we have prepared and measured a single-electron device with a Au-colloidal/fullerene island. The low-temperature current–voltage ($I-V_b$) characteristics display clear Coulomb-blockade structure and the gate-voltage modulations of the current ($I-V_g$ characteristics) show hysteretic behavior. The measured transport characteristics were analyzed within the context of single-electron tunneling and were compared with simulation results. SETs containing nanoparticles were reported previously,[1] but what we investigate here is the additional memory effect.

Figure 1 shows a scanning electron microscope (SEM) image of a fabricated sample. The electrodes were made following the scheme of Bezyadin *et al.*[2] Two oppositely pointed Au electrodes are made by standard electron-beam lithography and lift-off techniques. These electrodes, acting as a source and a drain, are to be bridged by Au-colloidal islands. The electrodes consist of a 10 nm thick Cr bottom layer, which is used as an adhesion layer, and a 25 nm thick Au top layer. The width of the electrodes is about 160 nm, and the gap between the two tips is about 15 nm. The substrate is a standard Si wafer covered by a 100 nm thick low-pressure chemical vapor deposition-grown Si_3N_4 and a 300 nm thick thermally grown SiO_2 layer. A window on the Si_3N_4/SiO_2 layer beneath the gap is etched away prior to the attachment of Au-colloidal islands. This window is defined by electron-beam lithography and is accomplished by CF_4/O_2 plasma reactive ion etching of Si_3N_4 layer and HF wet etching of SiO_2 layer. This process eliminates the capacitance between the colloidal islands (which are not yet present at this stage of the fabrication procedure) and the ground, and helps to increase the operating temperature. The two Au leads are made wider so as to sustain themselves without a substrate. In addition, a gate electrode (not shown in the SEM image) is placed about 400 nm away from the Au-colloidal particle. This gate electrode is used to tune the potential of the islands. After preparation of electrodes, the chips are ready for the assembling of Au-colloidal islands.

To assemble nanoparticles between the electrodes, two solutions, the first solution containing C_{60} derivatives (synthesized by C_{60} reacting with 2-aminoethl propyl disulfide) and the second solution containing Au nanoparticles (synthesized by reducing tetrachloroauric acid with trisodium citrate in distilled water), are employed alternatively.[3] In this process, C_{60} particles first attach to the Au electrodes, and by subsequent application of the second solution, the C_{60} particles can link Au-colloidal particles to the Au electrodes. Alternative application of the two solutions allows formation of one-dimensional chains of Au-colloidal particles linked by C_{60} with the desired number of Au particles between the two electrodes. The diameter of the Au-colloidal particles is about 14 nm, and the separation between the Au particles and the leads, including a linking C_{60} particle, is about 2 nm. In this work, the chip was alternatively subjected three times to the C_{60} derivatives containing solution and Au particle containing solution. The number of Au-colloidal particles be-

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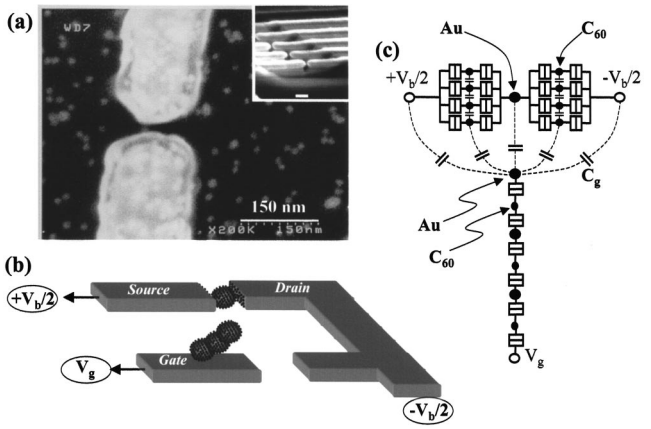

FIG. 1. (a) An SEM image of the measured device; the gate electrode is not shown. The inset shows the suspended Au leads before attachment of Au particles; the scale bar is 150 nm. (b) Schematic of the device: The source and drain electrodes are bridged by $C_{60}-Au-C_{60}$ nanoparticles, acting as an electrometer, and the gate electrode is also attached by a chain of $C_{60}-Au$ nanoparticles, acting as a charge storage cell. (c) The circuit model used for simulation. The electrometer is symmetrically biased.

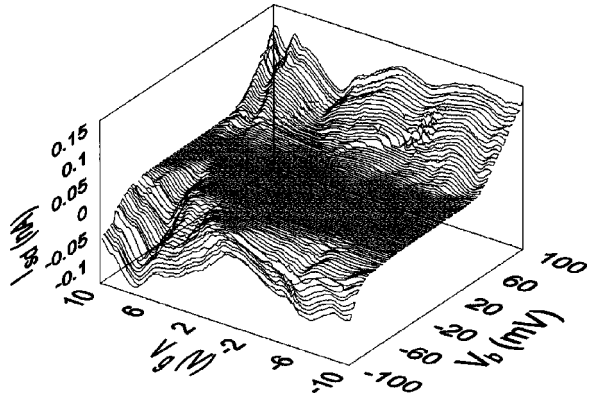

FIG. 3. A three-dimensional plot of I_{sd} vs V_g and V_b. The curves are measured at $T=4.2$ K. Note that the modulation is irregular, but the curves are reproducible, and a Coulomb-blockade region is clearly seen.

tween the two electrodes was limited by the gap separation to only one single particle. Details of synthesis and assembly of the Au and C_{60} nanoparticles will be reported elsewhere.[4] Several attempts along this line have been made: Similar structure but with aminosilane as an adhesion agent was studied previously by Sato *et al.*;[5] M. Persson *et al.*[6] also used a similar approach, where Au particles were connected to Au electrodes via dithiol. Other approaches for preparation of small particles such as thermal evaporation of AuPd islands[7] have also been pursued, but the number of particles was not controlled. In these works, the electrodes were prepared in a single standard lift-off process.

Figure 2 shows $I-V_b$ characteristics taken at three temperatures. The curves are nonlinear with a current smaller than the linear ones. The nonlinear behavior is more pronounced at lower temperatures, which is a sign of the Coulomb blockade of electron tunneling. However, this behavior alone cannot prove the existence of a charging effect. The single-electron tunneling should manifest itself in an oscillatory modulation of the source–drain current I_{sd} as a function of applied gate voltage V_g. Figure 3 shows this modulation, i.e., $I-V_g$ characteristics, measured at various bias voltages. Notice that the $I-V_g$ characteristic is not a simple periodic oscillation curve (as for a single-island SET) but is an irregular modulation curve. Despite this, these curves are reproducible and have a clear dependence on the bias voltage; as the bias voltage decreases, the current dips shift with gate voltage and fine structures appear. This irregular modulation implies that the device consists of multiple islands connected in series. The shift in the dip position indicates that the threshold potential required for tunneling through one of the junctions changes with bias voltage. Furthermore, at high bias voltages, more tunnel channels are activated at the same time and the fine dip structures seen at low bias voltages thus diminishes. To justify this multi-island model, we built a Monte Carlo simulation code[8] based on the orthodox theory[9] to calculate $I-V_b$ characteristics of such a device at $T=4.2$, 77, and 300 K. Notice that one Au particle can actually be surrounded by about 70 C_{60} particles, and, as schematically depicted in Fig. 1(b), there are approximately four C_{60} particles between the Au-colloidal particles and each Au lead. Each C_{60} couples to the leads and Au-colloidal particle via two tunnel junctions with capacitance C_J and resistance R_J, and couples to the gate electrode via gate capacitors C_g. This $4C_{60}-Au-4C_{60}$ circuit is illustrated in Fig. 1(c). Inter-C_{60} coupling is taken into account by coupling capacitors C_C, but no electron tunneling between C_{60} particles is allowed. Due to this intercoupling, the electron tunneling in the four-parallel C_{60} SETs are correlated. Figure 2 shows a comparison of the measured and calculated $I-V_b$ characteristics. In the calculation, static offset charges in Au and C_{60} particles are randomly assigned. All sample parameters including C_J, R_J, C_C, and C_g are randomly assigned with a spread within an assigned distribution range. These parameters are listed in Table 1.

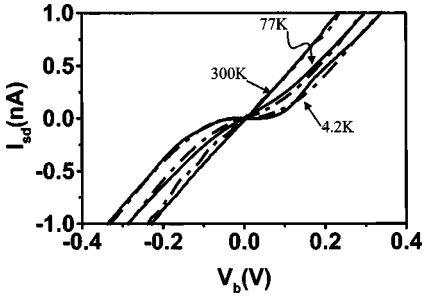

FIG. 2. $I-V_b$ characteristics (solid curves) measured at 4.2 K, 77 K, and 300 K. The dashed curves are calculated $I-V_b$ characteristics at the corresponding temperatures using the electrometer parameters listed in Table I.

Figure 4(a) shows measured current at a fixed bias voltage as a function of gate voltage for a second sample. Note that the $I-V_g$ characteristic is hysteretic, and this hysteresis is, again, reproducible for various bias voltages. This is attributed to charges stored in nearby, additional nanoparticles attached on the gate electrode. It has been shown both theoretically[10] and experimentally[11] that such a structure has,

TABLE I. The sample parameters used for simulations. The junction parameters are the same for both the electrometer and the storage cell.

C_J	R_J	$C_{g\to C60}$	$C_{g\to Au}$	$C_{g\to gnd}$	C_C
350±70 zF	100±10 MΩ	15±3 zF	110 zF	870 zF	40±8 zF

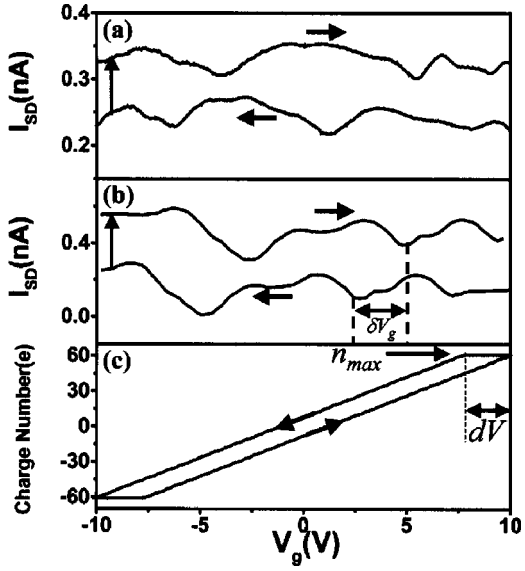

FIG. 4. A comparison of (a) measured and (b) calculated I_{sd} vs V_g curves at $V_b=160$ mV and at $T=4.2$ K. The upper curves in each panel are for $V_g=-10\ \mathrm{V}\rightarrow 10\ \mathrm{V}$, and the lower curves are for $V_g=10\ \mathrm{V}\rightarrow -10\ \mathrm{V}$. The upper curves are shifted up by 0.2 nA for clarity. The parameters for the storage cell used for calculation are listed in Table I. (c) Number of electrons in the storage cell as a function of ramping gate voltage.

as a function of the gate voltage, multiple value in the number of excess charges and is a basic building block of storage cells. To check the simulation in our circuit model as illustrated in Fig. 1(c), we incorporate the original $4C_{60}-Au-4C_{60}$ single electron device with additional 3 $\times(4C_{60}-Au)$ particles on the gate electrode. As shown in Fig. 4(b), the calculated $I-V_g$ curve is in reasonable agreement with the measured one, which strongly suggests that the system indeed consists of multiple islands in series, and the hysteresis arises from charge storage in unconnected islands. A memory cell is characterized by the presence of two distinct states,[12] which, as depicted in Fig. 4(c), manifests itself in the number of electrons in the storage island. The maximum number of electrons $n_{\max}$ that may be involved in this operation can be estimated as

$$n_{\max}=(V_{g\,\max}-dV/2)/(e/C_{g\Sigma}), \tag{1}$$

with $V_{g\,\max}$ as the maximum applied gate voltage and $C_{g\Sigma}$ as the total capacitances between the storage island and the multi-island electrometer. The value $(V_{g\,\max}-dV)$ is the threshold voltage for the first electron to enter the storage island (which originally contains $-n_{\max}$ electrons) when ramping down from $V_{g\,\max}$. Assuming an array of N tunneling junctions with identical C_J values, one can calculate dV by zeroing the energy required for the transferring of one electron from the gate electrode to the storage island via all tunnel junctions. In this way, dV is found to be related to the sample capacitances as

$$dV=(N-1)e/C_J+e/2C_{g\Sigma}. \tag{2}$$

In our circuit, $N=6$, $C_J\approx 350$ zF, and $C_{g\Sigma}=C_{g\rightarrow gnd}+C_{g\rightarrow \mathrm{particles}}\approx 1.1$ aF, giving a $n_{\max}$ of 60. This is consistent with the maximum number of involving electrons shown in Fig. 4(c). The key feature of the hysteretic characteristics is the double value of storage electrons n at any gate voltage. The difference in these two numbers then gives a voltage difference δV_g in the hysteretic $I-V_g$ characteristic. This δV_g is experimentally observable and is related to dV as

$$\delta V_g=dVNC_g/(C+NC_g). \tag{3}$$

Accordingly, we obtained a δV_g value of 2.58 V, which agrees reasonably well with the measured hysteresis shown in Fig. 4(a). We have measured several samples, which all showed similar behavior. Although the detailed structures in the measured characteristics cannot be fully accounted for, we believe that these devices can be described well by this circuit model.

In conclusion, we have bridged a pair of source–drain leads with $Au-C_{60}$ nanoparticles. The device exhibited pronounced Coulomb-blockade-type $I-V_b$ characteristics and complex $I-V_g$ oscillations, which can be described by a multi-island model. The hysteretic $I-V_g$ characteristics are attributed to the presence of a charge storage cell. This is confirmed by a Monte Carlo simulation.

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