*Electrochemical and Solid-State Letters*, **9** (3) C51-C53 (2006)
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# Fabrication of Nanoscale $PtO_x$/PZT/$PtO_x$ Capacitors by E-beam Lithography and Plasma Etching with Photoresist Mask

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Nanoscaling of $PtO_x$/$Pb(Zr_xTi_{1-x})O_3$ (PZT)/$PtO_x$ capacitors in well-ordered arrays down to a cell size of 90 × 90 nm was sucessfully achieved by electron-beam lithography and plasma etching with photoresist mask. Fast etch of $PtO_x$ and PZT layers was obtained with a rate of 165 nm/min in plasma of $Ar/Cl_2/10\%O_2$ and 240 nm/min in $Ar/CF_4/30\%O_2$, respectively. The selectivity of $PtO_x$ to NEB resist was 5.8 and that for PZT was 4.3. Crystallization of PZT film and reduction of $PtO_x$ layer were also observed after post-annealing of the etched specimens. Direct electrical measurement reveals that a good polarization switching characteristic can be retained in the nanoscaled PZT capacitors.
 [DOI: 10.1149/1.2162339] 

Manuscript submitted June 15, 2005; revised manuscript received November 16, 2005. Available electronically January 9, 2006.

The fabrication of a large array of ferroelectric thin-film capacitors, such as $Pb(Zr_xTi_{1-x})O_3$ (PZT) and $(Ba_{1-x}Sr_x)TiO_3$ (BST), is important for the development of high-density nonvolatile ferroelectric random access memories (FeRAM) and dynamic random access memories.[1,2] Especially for system-on-chip application, the FeRAM has the potential to replace other standard embedded semiconductor memories due to its high-performance and low-cost advantages.[3,4] To reach full compatibility of integration with nano-scaled complementary metal oxide semiconductor (CMOS) logic and interconnect circuits for high-density embedded memories beyond G-bit, the ferroelectric capacitor must have a lateral dimension below 100 nm and must retain a high polarization value for large array sensing. Fine patterning ferroelectric cell arrays with lateral size of 100 nm were performed using transformed metalorganic mesa by electron beam (EB) direct writing.[5,6] Nevertheless, to directly measure the electrical properties and realize the interconnect characteristic, patterning and etching of full capacitor stack consisting of a top electrode is necessary.[7,8] Ganpule et al. have measured the piezoresponse of PZT capacitors by atomic force microscope (AFM) in a scale down to 100 × 100 nm with Pt/$(La,Sr)CoO_3$ top electrode, which was patterned by focus ion beam (FIB).[7] However, the high ion energy may lead to a high density of surface defects and cause properties degradation.[9] Comparing to FIB patterning, the technique of dry etching with high-density plasma provides a high etch rate and low etch damage with large-area process control capability,[10] which is more appropriate to adopt in fabrication of the array of nanoscale capacitors for mass production of the memories.

Noble metal electrode, such as Pt, is usually used in the ferroelectric capacitors for its good electrical property and high oxidation resistance.[11] However, the use of Pt electrodes in high-density memory cells is still not practical due to the difficulty of etching. To solve this problem, the use of $PtO_x$ thin film as a transient template of Pt electrode is considered. The $PtO_x$ films show benefits of high etch rate, selectivity, and etch slope, along with a suppression of sidewall redeposition, as described elsewhere.[12] Improvement in polarization switching characteristic of the PZT capacitors has been also reported due to the release of oxygen from the $PtO_x$ electrode to compensate for the oxygen vacancies in PZT.[13,14] In this work, the successful fabrication of array of nanoscale PZT capacitors with $PtO_x$ electrode by EB patterning and high-density plasma etching with photoresist mask is demonstrated.

## Experimental

A double-layered bottom electrode of $PtO_x$ (50 nm) on top of Pt (100 nm) (abbreviated as $PtO_x$/Pt, hereafter) was deposited at 150°C on 6 in. TiN/Ti/$SiO_2$/Si substrate by RF magnetron sputtering of a 4 in. Pt target in pure Ar and, subsequently, in a gas mixture of $Ar/O_2$ with a ratio of 70/30. The 100 nm thick PZT film was then deposited at room temperature on the $PtO_x$/Pt electrodized substrates. To minimize the etching damage, post annealing to crystallize PZT films was not performed before the capacitor fabrication, which is different to the traditional process.[6] This is because the grain boundaries at the sidewall may be roughed by ion bombardment, causing the degradation of ferroelectric properties.[15]

The multilayered structure was then capped with a 50 nm thick $PtO_x$ film. The films were masked with hexamethyldisilazane (HMDS) primer and then coated with Sumitomo NEB-22 negative photoresist. The EB exposure was carried out using a Leica Weprint 200 stepper. The EB energy was 40 kV with a beam size of 20 nm and the exposure dose was varied from 9 to 16 $\mu C/cm^2$. After developing, the patternized wafers with NEB-resist mask were etched by high-density plasma in a helicon wave etcher with a single step sequence using the gas mixture of $Ar/Cl_2/O_2$ for $PtO_x$[12] and $Ar/CF_4/O_2$ for PZT. After ashing, a two-step annealing process was conducted. First, a rapid thermal annealing (RTA) at 600°C for 5 min under $O_2$ flow was employed for the crystallization of PZT films. Then, the specimens were annealed in a vacuum chamber with pressure of $5 \times 10^{-5}$ Torr at 400°C for 30 min to enhance the oxygen releasing from $PtO_x$ electrode for interfacial defect compensation[14] and the reduction of $PtO_x$ back to Pt for improving the contact resistance for electrical measurements. The crystallization of PZT layer was analyzed by X-ray diffraction (XRD). A stoichiometric composition of $Pb(Zr_{0.4}Ti_{0.6})O_3$ was also measured for the PZT films on Si substrate from Ruthford backscattering spectrometry (RBS) analysis with 2 MeV $He^{2+}$ ions, as shown in Fig. 1. In addition, the sidewall angle of the fully etched features and the etch morphology of the capacitors were observed by field-emission scanning electron microscopy (FESEM). The electrical property of the individual capacitor stack was measured with TF-2000 analyzer linking to ultrahigh vacuum atomic force microscope (UHV-AFM).

## Results and Discussion

The dependence of the critical dimension of dot size of NEB resist on the exposure electron-beam dosage is shown in Fig. 2. The process window of dot size can be observed from the dosage-fitting curve. The process window decreases from 3 to 1 $\mu C/cm^2$ as the designed cell size shrinks down from 300 to 90 nm, which reveals the process complexity.

Figure 3a shows the etch rates of $PtO_x$ and NEB resist, as well as their etch selectivity, as a function of $O_2$ content in the $Ar/Cl_2/O_2$ gas mixture at a flow rate of 40 sccm. The etching parameters of the source power, bias power, and gas pressure were kept constant at 2100 W, 250 W, and 5 mTorr, respectively. Additional $O_2$ is used in

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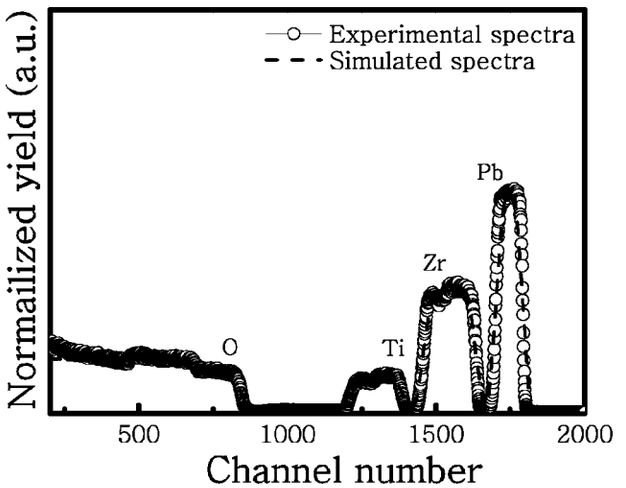


**Figure 1.** RBS spectra for scattering 2 MeV $He^{2+}$ ions of stoichiometric $Pb(Zr_{0.4}Ti_{0.6})O_3$ films on Si substrate.

the plasma to suppress the sidewall redeposition,[5-12] although it also increases the etch rate of NEB resists and decreases the selectivity. The maximum etching rate of $PtO_x$ films is around 165 nm/min at the addition of 10% $O_2$, and the etching selectivity can reach to an optimum value of 5.8. The etch rates of PZT and NEB resist, and their selectivity are also shown in Fig. 3b. The etching parameters of the source power, bias power and gas pressure were kept constant at 2500 W, 150 W, and 5 mTorr, respectively. The maximum etching rate of PZT is 240 nm/min at the addition of 30% $O_2$ into the gas of Ar(50%) /(50%) $CF_4$, and the selectivity is around a value of 4.3. The addition of $O_2$ leads to an increase of F radicals, and thus enhances the etch ability. However, the etch rate decreases when too much $O_2$ is added into the mixed gas, obviously due to the reduction of Ar-ion concentration causing the loss of physical bombardment effect, and leading to a poor selectivity between PZT and NEB.

The micrographs of the etched PZT capacitors with lateral size decreasing from 300 to 90 nm were observed via FESEM, as shown in Fig. 4. A well-ordered array of PZT capacitors was obtained without sidewall residue and fences redeposition. Each cell still has a taper sidewall angle over 75°. The thickness of PZT film for 90 × 90 nm capacitor was 90 nm and the thickness of PZT film for 300 × 300 nm capacitor was 100 nm. Rounded cells were found

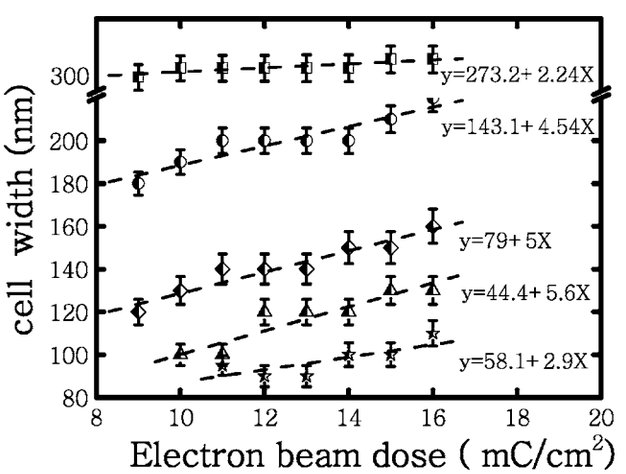


**Figure 2.** Dependence of the critical dimension of dot size of NEB resist as a function of exposure electron-beam dosages.

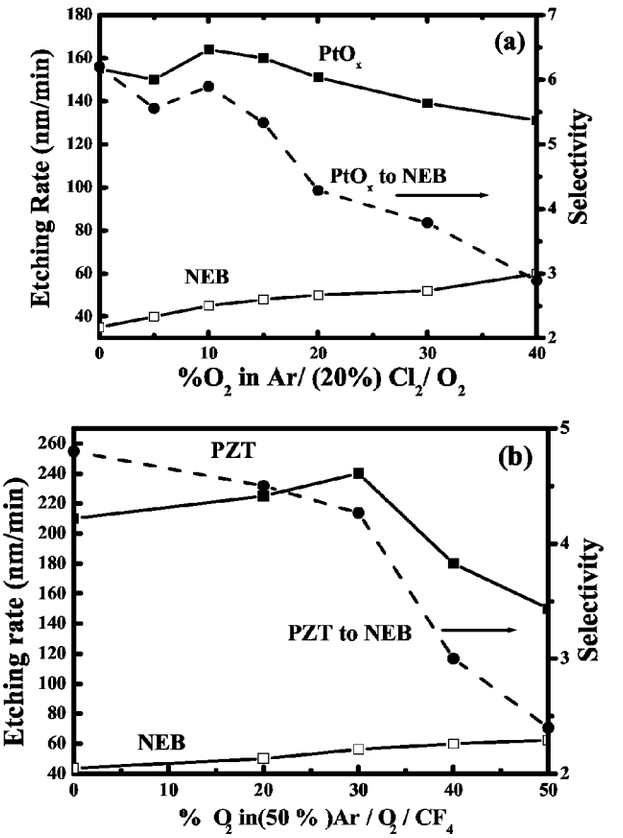


**Figure 3.** Etch rate of (a) $PtO_x$ and NEB and their etching selectivity as a function of $O_2$ content in the Ar/(20%) $Cl_2/O_2$ plasma, and (b) PZT and NEB and their etching selectivity as a function of $O_2$ content in the Ar/(50%) $CF_4/O_2$ plasma.

when the dimension was scaled down to less than 300 nm, which is because the corners of NEB-resist mask are more rapidly etched off

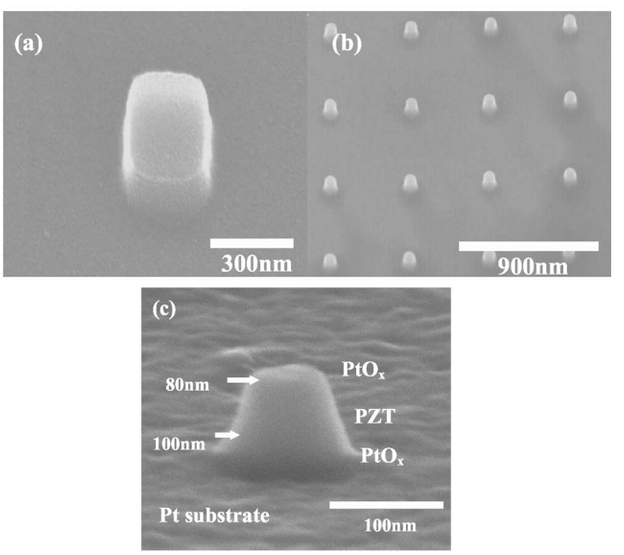


**Figure 4.** SEM showing (a) single cell capacitor (300 nm lateral size), (b) a cell array (90 nm lateral size), and (c) the cross-sectional view of $PtO_x$/PZT capacitor (90 nm feature size).

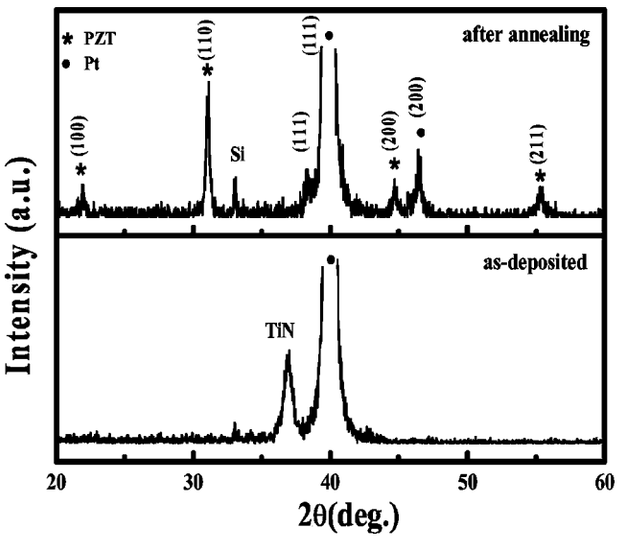


**Figure 5.** XRD patterns of as-deposited and postannealed $PtO_x$/PZT/$PtO_x$/Pt thin films.

by the $O_2$-additive plasma. Figure 5 shows the XRD patterns of the PZT capacitors on the Si substrate before and after the two-step annealing process. The PZT layers are well crystallized into perovskite phase. The reduction of $PtO_x$ layers into crystalline Pt is also observed, which can be confirmed from the appearance of Pt(200) peak.[14]

The hysteresis loops of polarization vs applied electrical field (P-E) were directly measured from the nanoscaled capacitors. In the measurement, a conductive Pt-coated cantilever was used, and an enhanced compensation procedure was adopted to eliminate the parasitic capacitance of setup, which was obtained from an open measurement by lifting the cantilever due to its linear character.[16] Figure 6a shows the measured P-E hysteresis loops after elimination of parasitic value, which exhibits the satisfactory result after compensation. The results of the capacitors with different feature size are also shown in Fig. 6b. All of them have a high $P_r$ value and no size effects were observed down to 90 nm. However, the shape of hysteresis loops for feature size below 150 nm were distorted, which is most likely due to the worse signal to noise ratio influencing the accuracy of measured polarization value.[16]

In summary, fabrication of nanoscale PZT capacitor array down to 90 × 90 nm using $PtO_x$ top electrode was successfully achieved by EB lithography and plasma etching with photoresist mask. Direct electrical measurements reveal that a good polarization switching characteristic is retained in the nanoscale ferroelectric capacitors. The result indicates that the integration of PZT capacitor array in nanoscale is feasible for fabricating high-density ferroelectric memory with the use of $PtO_x$/PZT/$PtO_x$ capacitor configuration.

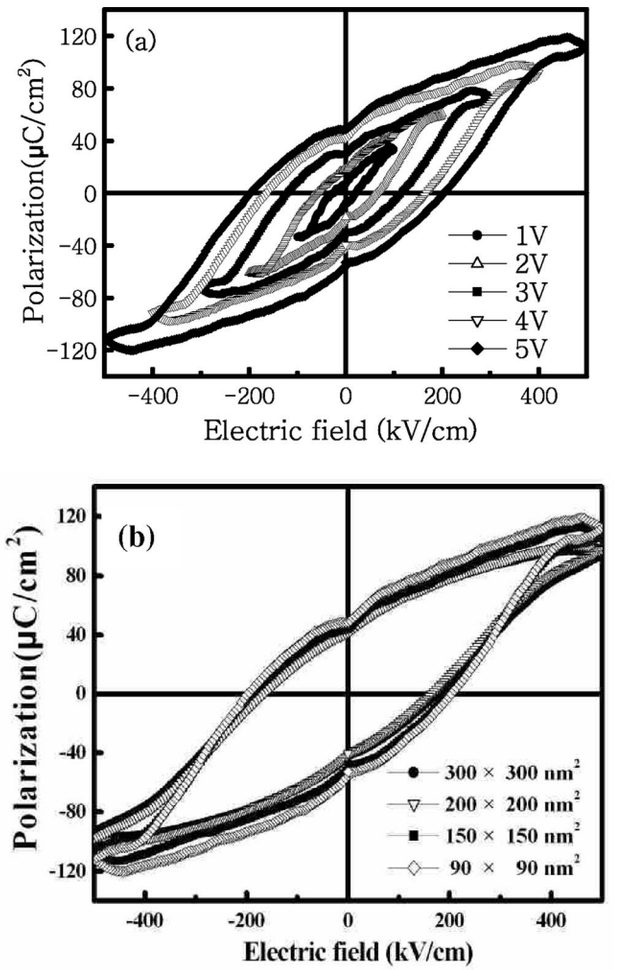


**Figure 6.** (a) P-E hysteresis loops obtained from capacitor stack of 90 × 90 nm feature size after compensation and (b) compensated P-E hystersis loops measured from capacitors with different feature size.


## Acknowledgments

The authors thank Dr. Stephan Tiedke and Thorsen Schmitz of aixACCT System for the measurement and discussion of the electric properties. The work was supported by Taiwan Semiconductor Manufactory Company under project no. 92A0174J4.

*National Tsing Hua University assisted in meeting the publications costs of this article.*


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