# Influence of Grinding Process on Semiconductor Chip Strength

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**Abstract:**

The objective of this paper is to study the strength distribution of semiconductor chips on a wafer, and the influence of the back-side grinding process on the chip strength.. The three-point bending test, complying with the ASTM standard E855, was adopted to measure the chip strength. The first set of test vehicles is from three 8-inch wafers. One is of 28 mils thick without backside grinding, and the other two are backside ground to 18 mils and 11 mils thick. Then, four 6-inch wafers were used as the second set of test vehicles. The first two were 22 mils thick which were backside ground and the other two wafers were 27 mils in thickness without grinding. The third set of test vehicles was formed by three 8-inch wafers of identical thickness (11-mil) and size, but they were backside ground by different factories.

It is found that, whereas the chip strength distributed randomly on a wafer which did not experience any backside grinding, any wafers that were subjected to backside grinding always resulted in weak regions. The averaged strength for the chips in the weak region was approximately 30% lower than the averaged strength calculated from the whole wafer, regardless of the chip dimension. This phenomenon is independent of wafer thickness to be ground, wafer diameter, backside grinding equipment and process, existence of metal and passivation layers, etc. Meanwhile, this weak region, in the shape of a pair of sectors, is axisymmetric to the wafer center.

## 1. Introduction:

The drive to use portable electronic devices, smart cards, multi-chip modulus, 3-D package, etc., forces the industry to develop thinner packages with thinner chips. At the same time, the drive to employ larger chips with lower cost per function also forces the industry to use wafers of larger diameters (300mm). As a result, wafers become thicker and the need to do backside grinding increases significantly. This process is generally done before the wafer is dicing. Thus, the damage due to backside grinding, which is one of the major causes of die cracking after packaging, becomes inevitable. Although this annoying problem can also be solved by, for example, a better material and structural design to lower the stress on die surface after it is packaged, a fundamental solution is still relied on the improvement of chip strength. Before an optimal solution could be found out to solve this problem, the first step is to study the cause of the damage of the wafer. This is the motivation of the current study.

There are only limited data available in the literature for this topic. In 1994, Blech and Dang studied the effect of backside grinding on wafer deformation [1]. In this paper, the wafer, after backside grinding using different types of machine, showed different distribution of residual stress concentration. Based on this phenomenon, what we are interested is if a chip, after dicing from a wafer, also exists excessive stresses or damage. And whether this excessive stresses or damage is the potential root cause of die cracking after the chip is packaged.

In 1987, Hawkins, et al., conducted a series of biaxial loading tests on chips to study the influence of flaws on chip strength. Unfortunately, the prediction did not consistent with the experimental data [2]. And as the experimental results scattered so much, it is difficult to extract physical phenomenon. Scott and Popelar [3] used the four-point bending method to test nine groups of chips. They measured the total chip strength and studied the influence of the chip dicing process. This included the effect of flaws and chipping. Three parameters, i.e., bare die, etching process and backside grinding speed, were employed in their study. However, the dimensions of the chips used in their study are much larger than the dimensions people normally used for a real die in industry. As a result, the experimental phenomenon they observed might be very different from what will happen in semiconductor industry. In 1996, Ward used the three-point bending method to test three different types of chip, and interpreted the results by statistics [4].

In all the previously published data, the sample sizes were small and the chips used were randomly picked up from a wafer. As the semiconductor chips are made of brittle materials and it is difficult to learn before actually conducting the test how the chip strength depends on the location on the wafer, we decided to test all the specimens on wafers and map the chip strength on the wafer. Thus, in this study thousands of samples from wafers of different diameter, metalization process, backside grinding process, and chip dimensions were tested.

## 2. Experimental Method and Set Up:

For the experimental set-up, a force gauge mounted on an XYZ-table was employed as the loading and recording component, and an LDM (Laser Displacement Meter) was used as the displacement detector component. The testing method conforms to the ASTM standard E855 [5], as shown in Fig. 1. Note that in all the tests conducted and shown in Sections 3.1 to 3.3, the line loading was applied on the front side of the chip, i.e., the active side. Thus, the backside of the chip was subjected to tensile loading. The setup is calibrated using an LLORD material tester.

In this study, three sets of wafers were used. In the first set, three 8-inch wafers, designated as T1, T2 and T3, were used to study the effect of backside grinding on the measured chip strength, and the corresponding wafer thickness are 11-mils, 18-mils, and 28-mils, respectively. Wafer T3 was without backside grinding and T1 and T2 were ground from the original thickness, i.e., 28-mils, to 11 and 18-mils, respectively. The

in-plane dimensions of the tested chips are 13.6 mm by 6.3 mm and are all flash memory chips. Table 1 lists the geometry of the chips and wafers. In each wafer, more than 300 samples were tested.

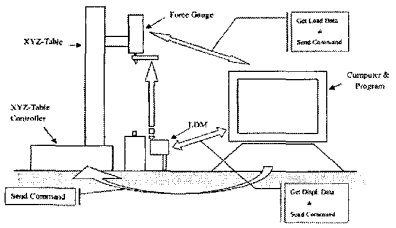


**Fig. 1 Experimental set up**

Test results from four 6-inch wafers were grouped as set two. These are all bare wafers. That is, no metal layers on the silicon surface. In this set, wafer B3 and B4 were not subjected to backside grinding, and are 27-mils in thickness, whereas wafers B1 and B2 were grounded down to 22-mils thick. This experiment was aimed at getting rid of the effect of metal layers on chip strength. The total number of chips, each of them is 11 mm by 11 mm, on a wafer is 121 and all these chips were tested in this study. Table 2 also depicts the relevant information of the tested chips.

In the last set, three 8-inch wafers, F1, F2 and F3, were used to evaluate the effect of using different grinding machines and process on the measured chip strength. These wafers were grounded to 11mils, The in-plane dimensions are 10.2 mm by 9.1 mm and are MROM chips.

| Object | Length (mm) | Width (mm) | Thickness (mil) | Diameter |
|---|---|---|---|---|
| T1, T2, T3 | 13.6 | 6.3 | 11,18,28 | 8" |
| B1 to B4 | 11.0 | 11.0 | 22,27 | 6" |
| F1, F2, F3 | 10.2 | 9.1 | 11 | 8" |

**Table 1. Geometries of the specimens tested**

When a chip is subjected to loading to failure, the peak load, $P_p$, is obtained from the record of the force gauge. Equation (1) is then used to calculate the corresponding chip strength:

$$\sigma_p = {1.5 \cdot P_p \cdot L}/{bh^2} \qquad (1)$$

where L, b and h, are the span, width and thickness of the chips tested. In the above equation, both the loading and the two simply supported boundaries were assumed to be of line type and were parallel to one another. In order to verify the validity of Eq. (1), which is based on the Euler beam theory, the finite element method was employed and the effect of the deviation in testing arrangement was studied. This included the span deviation, existence of non-parallel boundaries, concentrated loading/boundary-contact rather than of line-type [6]. The numerical results show that all the above-mentioned effect contributed insignificantly to the tested results and Eq. (1) is suitable within the scope in this study.

**Results and Discussion:**

3.1 Effect of Backside Grinding

The averaged chips strength on the three wafers, T1 to T3, is 235.7 MPa. Shown in Table 2 are the averaged chip strengths from the three wafers tested. The deviation is less than 5%. Thus, one can conclude that backside grinding, in general, will not affect the overall chip strength.

However, when the measured chip strength is mapped on the wafer, as shown in Figures 3, 4, and 5, which are for wafers T1, T2 and T3, it is found that weak regions do exist in the two wafers, i.e., T1 and T2, experienced back-side grinding. Note that the flat portion of the wafer is always oriented at the bottom of the figure. On the other hand, the chip strength is randomly distributed on wafer T3, the one not subjected to backside grinding. Further, the weak regions spread as a pair of sectors of around 30 degree, and are inclined also to approximately 30 degree. These sectors are opposite with respect to the wafer center, as shown in Figures 3 and 4.

| | T1 | T2 | T3 |
|---|---|---|---|
| Thickness (mil) | 11 | 18 | 28 |
| Sample Number | 302 | 308 | 304 |
| Avg. Strength (MPa) | 224.4 | 239.2 | 243.6 |

**Table 2. Averaged Chip Strength Results**

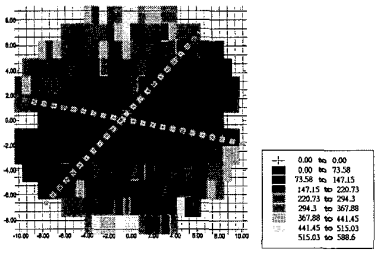

**Fig. 2 Chip Strength Map on Wafer T1**

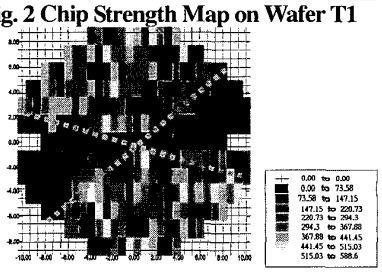

**Fig. 3 Chip Strength Map on Wafer T2**

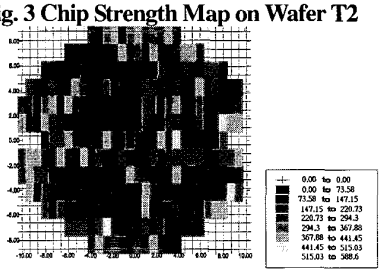

**Fig. 4 Chip Strength Map on Wafer T3**

When we calculated the chip strength from the weak region on wafers T1 and T2, these values are 30% lower than that of the strength averaged from the whole wafer, as depicted in Figure 5. In this figure, the averaged chip strength in the strong region, i.e., the wafer area substracted by the weak region, was also calculated. These values are approximately 40% higher than the averaged chip strength in the weak region.

**3.2 Effect of Metalization and Wafer Diameter**

To manufacture a semiconductor chip, several metal layers need to be put on top of a silicon wafer. During this process, a

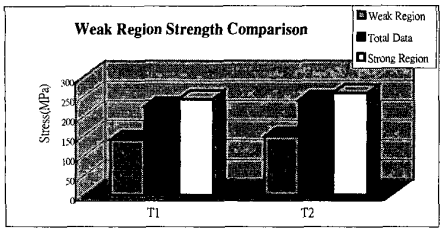


**Fig. 5 Chip Strength Comparison in Wafers T1 and T2**

wafer is subjected several runs of metal deposition and etching, and the temperature rises also to several hundreds degrees Celsius. In addition, when the passivation layer made by either Silicon Oxide/Nitride or polyimide is deposited, the stress on the backside of the chip will be different as the coefficient of thermal expansion (CTE) is much different for these two passivation materials. As a result, stresses accumulate and contribute also to die cracking when the chip is later on packaged.

To study this effect, four bare wafers, B1 to B4, were employed. As no metal layer was deposited, they should have much less residual stress on these wafers as compared to the chips having metal layers. For these four wafers, B1 and B2 were ground down to 22 mils from the original thickness of 27 mils. These four wafers were all of 6-inch in diameter. Thus, we also can study whether change of wafer diameter will result in any new phenomenon. A total of 121 samples were tested in each of the four wafers. Detailed geometry of these wafers is listed in Table 1.

Table 3 lists the averaged chip strength recorded from the test results. The averaged chip strength from all four wafers is 223.9 MPa. Although small deviation was observed, the averaged chip strength for each wafer is essentially the same regardless of whether the wafer experienced backside grinding or not.

| | B1 | B2 | B3 | B4 |
|---|---|---|---|---|
| Sample Number | 121 | 121 | 121 | 121 |
| Avg. Strength (MPa) | 218.8 | 222.8 | 214.5 | 239.6 |

Table 3 Chip Strength in four Bare Wafers

The chip strength map on wafers B1 to B4 are shown in Figures 6 to 9, respectively. For all these four 6-inch wafers, the flat portion was oriented to the bottom and each of the chips was tested in the same orientation, too. As expected, there exist weak regions in the two wafers by backside grinding, i.e., wafers B1 and B2, as shown in Figures 6 and 7. Although the orientation is more toward the vertical direction, the general trend is the same as that observed in the flash memory chip tested previously in Section 3.1, as shown in Figures 3 and 4. On the other hand, the chip strength distribution on wafer B3 and B4 are more uniform. No weak region was observed.

Thus, a brief summary can be made that backside grinding does produce a weak region for the chip strength regardless of whether it is a 6-inch or 8-inch wafer, existence of metal layer, and chip size. When the chip strength in the weak region is calculated, it is found that the value is approximately 30% and 40% lower than the averaged strength calculated from the whole wafer and the strong region, respectively. This phenomenon is exactly the same as that observed in Section 3.1.

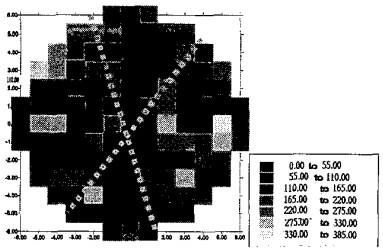


**Fig. 6 Chip Strength Map for Wafer B1**

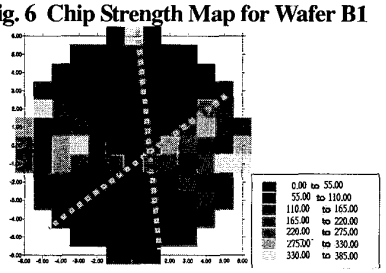


**Fig. 7 Chip Strength Map for Wafer B2**

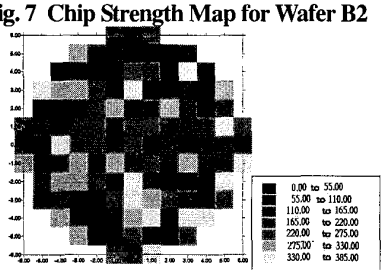


**Fig. 8 Chip Strength Map for Wafer B3**

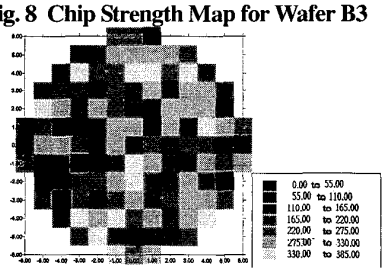


**Fig. 9 Chip Strength Map for Wafer B4**

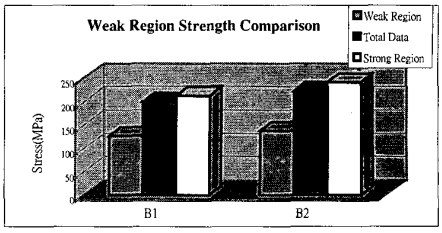


**Fig. 10 Chip Strength Comparison in Wafers B1 and B2**

### 3.3 Effect of Grinding Machine

For all the above-mentioned results, the backside grinding was done in one factory. In order to verify whether this weak region phenomenon occurs generally in industry, three wafers were sent to two contract manufacturing companies in Taiwan. It was hoped that this could verify whether different grinding machines and grinding processes would result in different distribution of chip strength. In this specific study, these three wafers were of 8-inch in diameter and were all ground to 11-mils.

The chips, all were for MROM applications, were 10.2 mm in length and 9.1 mm in width, as listed in Table 1. A total of 291 chips in each wafer were tested. The results are listed in Table 4. The averaged strength for all the chips tested from three wafers is 89.7 MPa, and the deviation among three wafers is considered to be small as it is less than 5%. It means that the averaged chip strength on a wafer does not affected significantly by using different grinding process by different machines.

| | F1 | F2 | F3 |
|---|---|---|---|
| Sample Number | 291 | 291 | 291 |
| Avg. Strength (MPa) | 89.3 | 86.0 | 94.0 |

**Table 4. Averaged Chip Strength for Wafers via Different Grinding Processes**

On the other hand, the weak regions for all three wafers still exist, as shown in Figures 11 to 13, although the orientation of the weak regions shown in Figure 12 is different from the ones in Figures 11 and 13. This is probably due to the effect of using different grinding machines. In addition, the chip strength in weak region is also 30% to 40% lower when comparing it to the averaged strength of the whole wafer and the stronger region, respectively. As a result, it is concluded that the existing of the weak region for chip strength in a wafer is a general problem.

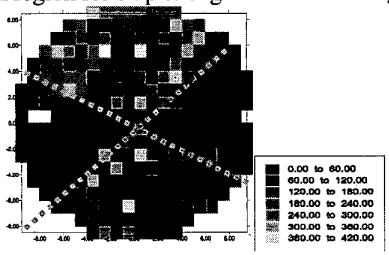


**Fig. 11 Chip Strength Map for Wafer F1**

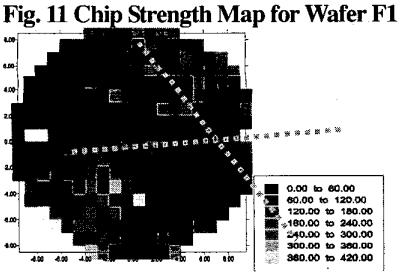


**Fig. 12 Chip Strength Map for Wafer F2**

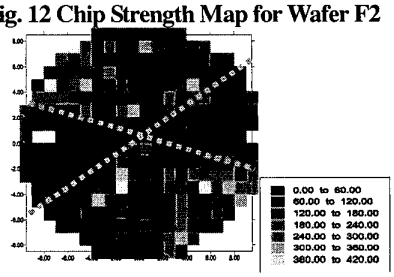


**Fig. 13 Chip Strength Map for Wafer F3**

3.4 Further Study on Effect of Metalization

In Section 3.2, an experiment was designed using the bare wafer to eliminate the effect of metalization and passivation. And in all the above tests, the line loading measured by the force gauge was exerted on the front face, i.e., the active side in which the metalization and passivation was applied. As a result, the backside of the chip was always in tension when subjected to the

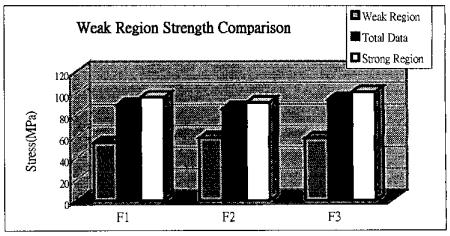


**Fig. 14 Chip Strength Comparison in Wafers F1, F2 and F3**

three-point bending load. Note that the CTE is approximately 6 ppm/C for silicon, 20 ppm/C for metals, and 100 ppm/C for polyimide. When the chip is cool down from its processing temperature of several hundred degrees, the backside of the chip is always in tension due to smaller contraction magnitude of the silicon. As a result, it is expected that the chip strength obtained by the three-point bending test must be different for the two sets specimens tested in this section. Table 5 shows the result in which the number of chips used in each set of test is 10. It is found that the averaged strength for the chips loaded on the backside is almost two folds to the strength for the chips loaded on the active side.

| | Act. Side | Backside |
|---|---|---|
| Sample Number | 10 | 10 |
| Avg. Strength (MPa) | 200.0 | 395.0 |
| STD | 80.1 | 53.1 |

**Table. 5 Strength for Chips Loaded on Active and Backside**

The causes of the much higher strength for chips loaded on the backside, in the authors' opinion, are three: (a) the backside of the chip has residual stresses in tension. This is because the CTE for silicon is much smaller than those for metal and passivation layers. Because the silicon is brittle, any additional tensile loading, in this case it is from the applied line loading on the active side in the three-point bending test, will tend to reach the value of the fracture toughness of the silicon material. However, when the chip is loaded from the backside, it is the active side of the chip, i.e., the metal layers, that is subjected to larger tension; (b) due to the backside grinding on the brittle silicon, micro-cracks occur and penetrate from the silicon surface. The additional tensile loading in the three-point bending test triggers propagation of some of these cracks; (c) the metal and the polyimide, if used, are ductile materials. They have much higher fracture toughness values and require much higher applied tensile loading to extend the stable cracks.

Further, the standard deviation for the strength of the chips loaded on the backside is much smaller than the standard deviation obtained from the chips loaded on the active side, although the strength from the former is almost two folds higher. This also helps demonstrate the fact that the active side of the chip has more uniform strength, a phenomenon usually observed for stable crack growth.

## 3. Conclusion:

Weak region in a wafer has been identified after testing thousands of chips using the three-point bending loading method. This weak region did not exist if the chips on a wafer did not go through the backside grinding process. It is evenly distributed within a pair of sectors 30 degree wide and is symmetric with respect to the wafer center. The averaged strength calculated

from the weak region has been found to be 30% lower than the chip strength averaged from the whole wafer. Further, this weak region and the corresponding reduction of the chip strength has been found to be independent of the wafer diameter, grinding thickness of the wafer, metallization layers and passivation type, grinding factory and equipment, and the dimensions of the chip. It is believed that the residual stresses existed on the damaged silicon surface, which, in turn, is due to backside grinding, is the major cause of this reduction of chip strength. As a result, there should be ways to improve during a packaging design and assembly process to prevent a packaged chip from cracking.

**4. Acknowledgment**

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**References**

1. Blech, I. and Dang, D., "Silicon Wafer Deformation After Backside Grinding," Solid State Tech., 1994, p.p.74-76
2. Hawkins, G., Berg, H., Mahalinggam, M., Lewis, G., and Lofgran, L., "Measurement of Silicon Strength as Affected by Wafer Back Processing," Physical Electronics & Packaging Laboratory, SRDL, Technical Report No, PEPL-37-8
3. Scott, F. and Popelar, "An Investigation Into the Fracture of Silicon Die Used in Flip Chip Applications," International Symposium on Advanced Packaging Materials, March 15-18, 1998
4. Ward, A. III, "Residual Stress Effects on Power Slump and Wafer Breakage in GaAs MESFETs," Ph D Dissertation, Materials Engineering Science Department, Virginia Polytechnic Institute and State University, USA.
5. ASTM Industrial Standard , E 855
5. Chen, S.L., "On Strength Analysis of Chip Strength and Optimal Design of Large-die Flip Chip Packages," Ms Thesis, Institute of Applied Mechanics, National Taiwan University, Taiwan, ROC, 2001.