HOW TO IMPROVE CHIP STRENGTH TO AVOID DIE CRACKING IN A PACKAGE

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ABSTRACT

Die cracking is an annoying problem in the packaging industry. In our previous study, we have identified the weak region of the chip strength distribution in a wafer using the three-point bending test. It was found that the strength of the chips within the weak region was 30% to 50% lower than the averaged chip strength of the whole wafer, and the cause of the weak region was due to backside mechanical grinding. In this paper, additional thousands of chips on different wafers were tested to find the solution to enhance the chip strength in these weak regions, which included the effects of grinding speed, fine grinding depth, post processing using plasma etching or polishing, and search of optimal polishing depth.

It was found from the experimental results that (a) slow down the grinding speed can increase chip strength in both the weak region and the whole wafer by approximately 50%, (b) although use of polishing after mechanical grinding increased the chip strength in the weak region, only 1 to 2 umthick polishing is considered adequate. On the other hand, use of coarse mechanical grinding only reduced the chip strength drastically to about 20% of the original value.

KEY WORDS: chip strength, mechanical backside grinding, plasma etching, polishing, die sawing

1. INTRODUCTION

As electronic devices become more complicated and the increasing need for use of semiconductor chips in portable products, the requirement for chips and packages to be smaller and lighter becomes more stringent. As a result, a wafer needs to be ground thinner before dicing. In the current packaging industry, wafers are first processed by coarse mechanical grinding using particles of #320 mesh size followed by fine mechanical grinding of #2000 mesh size. Grinding marks of spiral shape are easily observed on the backside of the wafer, which was a kind of structurally defect and inevitably induced micro-cracks. In order to remove these micro-cracks, additional process using either wet polishing or plasma etching is frequently induced [1]. On the other hand, dicing wafer always induces chipping and rough edges on a chip. This damage also becomes the source of crack propagation when the chip is stressed. Further, when a diced chip is packaged, due to mismatch of the coefficient of thermal expansion in different materials that composed of the package, the chip is frequently subjected to large tension on its backside. As a result, die cracking initiated from either the grinding mark or the rough edge is sometimes found and becomes an annoying issue, especially when the chip becomes thinner and larger. Thus, the need for investigating the chip strength due to backside grinding becomes obvious.

Currently, literature study about the effect of grinding on chip strength is still very limited. In 1994, Blech and Dang studied the effect of backside grinding on wafer deformation [2]. In this paper, the whole wafer after backside grinding using different types of machine, showed different distribution of residual stress concentration. In 1987, Hawkins, et al, conducted series biaxial loading tests on chips to study the influence of flaws on chip strength. Unfortunately, the prediction was not consistent with the experimental data [3]. In addition, as the experimental results scattered drastically, it was difficult to extract physical phenomenon. In 1998, Popelar used the four-point bending method to test nine groups of chips [4]. They measured the total chip strength and studied the influence of the chip dicing process, and included the effect of flaws and chipping. Three parameters, i.e., bare die, etching process and backside grinding speed, were employed in their study. However, the dimensions of the chips used in their study were much larger than the dimensions normally used for a real die in industry. As a result, the experimental phenomenon they observed might be very different from what happens in the semiconductor industry.

In our previous study [5,6], we used the three-point bending method to measure the strength of thousands of chips and observed weak region of approximately 45 degree in two sectorial regions axisymmetrically to the wafer center. The chip strength in these weak regions was found to be 30% to 50% lower than the chip strength averaged from the whole wafer. The orientation of the weak regions coincides with the spiral grinding marks and the chip orientation within the wafer. In this study, a more detailed study is performed to correlate the failure pattern of the chip with the measured strength, and

investigate from the probabilistic point of view. Extensive parametric study on the mechanical grinding speed, coarse versus fine mechanical grinding, search of optimal polishing depth, etc, will also be presented in this paper.

2. EXPERIMENTAL SETUP

The experimental setup for three point bending test is identical to that used in [5,6]. In this setup, a force gauge was mounted on a XYZ-table as the loading and data recording component. An LDM (Laser Displacement Meter) was used as the displacement measurement device. The testing method conforms to the ASTM standard E855 [7], as shown in Figure 1. Note that in all the tests conducted the line loading was applied on the front side, i.e., the active side, of the chip. Thus, the backside of the chip was subjected to tensile loading.

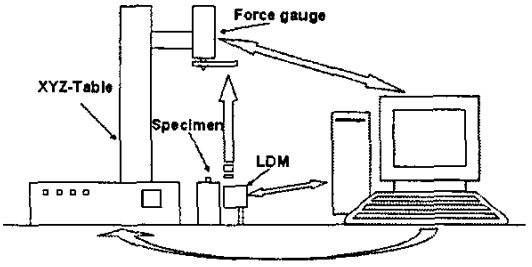


Fig. 1 Schematic of the experimental setup for three-point bending test

In this study, the backside mechanical grinding process employed is an industry standard one, which includes two steps: the coarse grinding as the first step, and the fine grinding as the second step [8]. The grinding tool is a wheel containing diamond particles of very fine dimension bonded with epoxy or wax. When the wafer is placed on the rotating chuck, the grinding wheel presses on the wafer backside and rotates with different directions. By the shear force exerted from rotating chuck, the hard diamond particles remove silicon from the wafer backside. More than 90% wafer thickness is eroded in the coarse grinding process normally. The subsequent fine grinding process, using even finer diamond particles, removes the remaining thickness and the majority of the micro-cracks caused from coarse grinding.

Table 1 lists the design of the experimental plan. In the first group, the effect of grinding speed and the depth of the fine grinding is studied. For the wafers tested in the second group, additional post grinding process was employed by using either polishing or plasma etching, and the effect of polishing depth was also studied lastly.

In this paper, the grinding speed in the mechanical grinding process was 5500 rpm unless otherwise mentioned. Further, when samples were picked from a wafer, there were picked randomly from all eight regions of the wafer, as shown in Figure 2. In this figure, 24 samples were selected for most of tested wafers. For the tests using different sample number, the criterion is similar. This aims to obtain the averaged chip strength from the wafer.

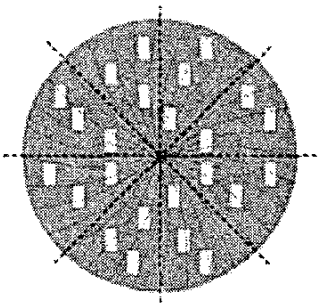


Fig. 2 The sketch of samples picked in eight regions of a wafer. The grinding mark of spiral shape is also plotted

Table 1 Experimental Grouping

Object	Grouping	Device Type	Geometry(mm)	Sample Size	Corresponding Section
Mechanical Grinding	i. Grinding speed	NOR Flash	9.4x3.9x0.432	788pcs x 2 wafer	3.1
	ii. Fine grinding depth	Mask ROM	9.4x4.6x0.483	24pcs x 4 wafers	3.2
Post Grinding	i. Polish vs. Plasma Etching	NOR Flash	11.2x5.45x0.283	40pcs x 3 wafers	4.1
	ii. Polish Depth	NOR Flash	11.2x5.45x0.283	10-24pcs x 5 wafers	4.2

When a chip is subjected to three-point loading to failure, the peak load, Pp, is recorded by the force gauge. The chip strength is then calculated as

$$\sigma_p = {1.5 \cdot P_p \cdot L}/{bh^2} \qquad (1)$$

where L, b and h, are the span, width and thickness of the chips tested. In the above equation, both the loading and the two simply supported boundaries were assumed to be of line type and were parallel to one another. In order to verify the validity of Equation (1) when the experimental arrangement was not perfect, the finite element method was employed and the effect of the deviation in testing arrangement was calculated. The parameters studied including the span deviation, existence of non-parallel boundaries, and concentrated load/boundary rather than line-type. The numerical results showed that all the above-mentioned effects contributed insignificantly to the tested results and Equation (1) was suitable within the test scope in this study.

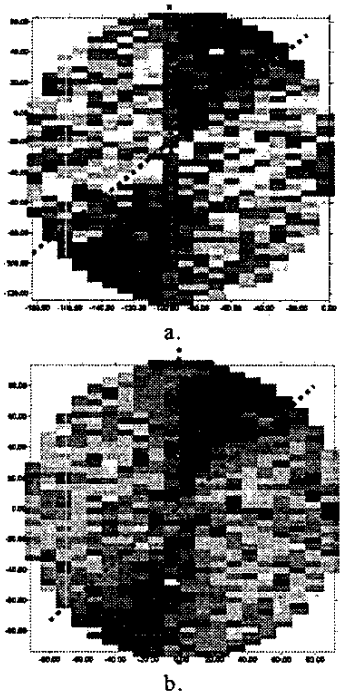
3. MECHANICAL GRINDING PROCESS

3.1 Effect of Grinding Speed

Two 8-inch wafers, each one has 788 NOR flash chips 9.4mm by 3.9 mm were employed for the study of the effect of grinding speed on the chip strength. The grinding speed of the first wafer, S1, is 5500rpm, which is the standard spindle speed used in the industry. The grinding speed for the second wafer, S2, is 2750rpm. The grinding speed for coarse grinding

is always 5500 rpm. Thus, the only difference in the grinding speed is in the fine grinding process. The mesh sizes used in the coarse and fine mechanical grinding processes were #320 and #2000, respectively.

Figure 3 shows the mapping of the chip strength tested on each wafer. The flat of each wafer is always located at the bottom of the figure. The chips with darker color in each wafer have lower strength. The averaged chip strengths of the whole wafer for S1 and S2 are 315MPa and 202MPa, respectively. In this figure, the weak region in each wafer, which are the two sectors 45 degree wide and symmetric to each other are clearly observed. It is noticed that the color in S2 wafer is lighter than that in S1 wafer, indicating that slower grinding speed resulted in a higher chip strength. In our previous study, we have identified that the existence of the weak region in each wafer is due to the grinding marks [9]. These grinding marks, and the corresponding micro-cracks at their tips, are the weakest portions of the chips. The chips in the weak region always have the grinding marks in parallel to the chip width edges. When these chips are subjected to line-loading during the three-point bending test, cracks tend to propagate because the positive bending stress at the backside of the chip was applied. It is a typical Mode I fracture, as depicted in Figure 4. As a result, the chip strength in the weak region always has lower strength compared to the chip strength in the remaining portion of the wafer. On the other hand, use half of the grinding speed enhanced the chip strength due mainly to the fact that the grinding marks are less significant and the damage to the wafer backside is lighter.



a.

b.

Fig. 3 Chip strength map on (a) wafer S1; and (b) wafer S2

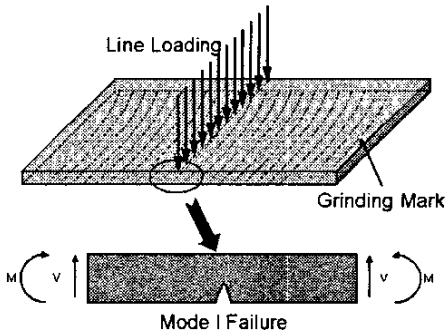


Fig. 4 Schematic of the grinding marks on backside of a chip and fracture of the chip by three-point bending load

Because the chip was broken after the three-point bending test, the fragmentary body can be a useful clue to get more information or the linkage between different physical phenomena. Figure 5 shows the result of grouping of the fracture pattern. When chips were broken in only two pieces under three-point bending loads, they belonged to Type A. When chips were fractured in three to five pieces, they were categorized as Type B chips. When the number of the broken pieces for a chip was from six to ten, it is categorized in Type C. When a chip was shattered under the loading, it was classified as Type D. Row two of Figure 5 shows typical fracture patterns for chips in Types A, B, C and D. During the test, we could always re-assembly the fragmented pieces back to the original chip shape for chips in Types A, B, and C. On the other hand, the fragments in Type D were so small that we were not able to put the back to the original chip shape. By close investigation of these tested chips, we found that the grinding marks in Type A were in parallel to the width of the chips, and those in Type D were in parallel to the length of the chips. On the other hand, the orientation of the grinding marks for chips in Types B and C was inclined to the chip edges, as also portrayed in Row there of Figure 5.

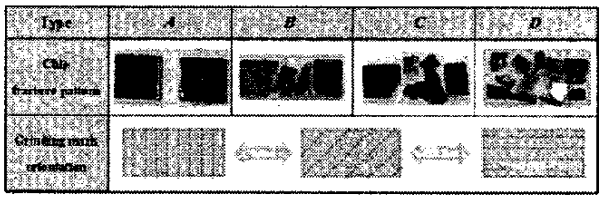


Fig. 5 Grouping of chip fracture pattern

In Wafer S1, the total number of chips in types A, B, C, and D was 287, 165, 289, and 47, which represents a percentage distribution of 36.4%, 20.9%, 36.7% and 6.0%, respectively. For S2 Wafer, the total number of chips in types A, B, C, and D was 184, 86, 308, and 210, and the percentage distribution is 23.4%, 10.9%, 39.1% and 26.6%, respectively. From these numbers, we found that S2 wafer has significantly less number of chips fall into type A whereas it has much larger number of chips in type D. The averaged chip strength of these four types of chips is depicted in Figure 6. In this figure, the chip strength increases as the number of fractured pieces increases. This trend is logically reasonable as more fresh surfaces are

created as a chip is broken into more pieces. As a result, more energy, which comes from the larger magnitude of the applied load, is needed. From these data, it is concluded that the strength of a chip tested under three-pointed bending loading is strongly affected by the grinding marks on the backside of the wafer, and this strength can be much enhanced by reducing the backside grinding speed.

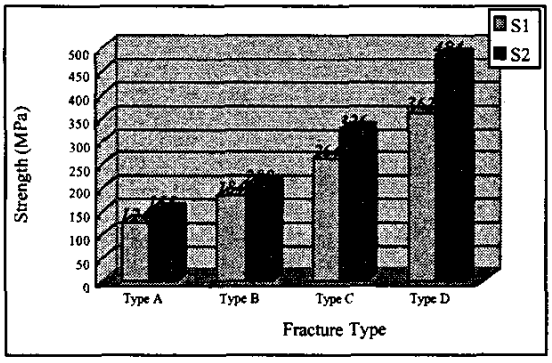


Fig. 6 Comparison of the averaged strength in Types A, B, C, and D in wafers S1 and S2

The strength distribution of the chips can also be observed from the probability aspect. Figure 7 shows the result. Both S1 and S2 results have two peaks in the probability distribution, the first peak corresponds to the strength in the we ak region. Further, by comparing the result from wafers S1 to S2, we noticed that the probability distribution in wafer S2 is smoother, and the peaks were shifted to the higher strength side. This demonstrates that by reducing the grinding speed, the damage due to backside grinding marks is less significant. Thus, it results in a higher chip strength, as already shown in Figures 3, 5, and 6. Finally, the weaker 25% tested results were calculated and the calculating result is called as lower fourth in statistics. The lower fourth results of S1 and S2 were 89.0MPa and 131MPa respectively, and S2's was increased about 47.2%. The increasing ratio was very similar to the total averaged strength difference between S1 and S2. Slower grinding speed does improve the chip strength and the effect is total to whole wafer.

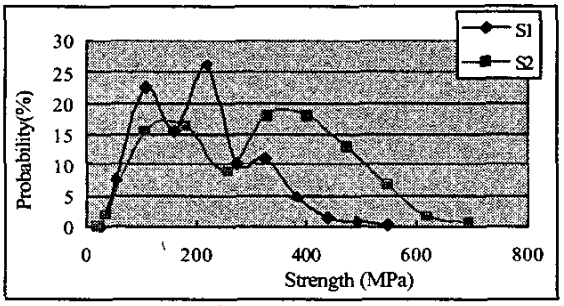


Fig. 7 Probability distribution of chip strength in wafers S1 and S2

3.2 Effect of fine grinding depth

In this section, four groups of tests were conducted to investigate the effect of fine grinding depth on the chip strength. In the first group, the wafer was thinned only by coarse grinding with #320 mesh size. In the rest three groups, the wafers were thinned additional 10, 20, and 30 um more by fine grinding of #2000 mesh after the coarse grinding. In each group, 24 chips of 9.4mm by 4.6 mm in size were picked from a wafer. Figure 2 shows the scheme for selection of these chips from a wafer. The design for the test was such that the final wafer thickness was all 483 um (19-mils).

Figure 8 shows the experimental result, in which there is no direct correlation between the fine grinding depth and the chip strength. This might be an indication that 10 um fine grinding is deep enough to remove the damage induced during the coarse grinding process. On the other hand, the strength obtained from the chip experienced coarse grinding only on its backside only has 20% the strength for chips experienced additional fine grinding. Although the fine grinding process after coarse grinding is a standard procedure in the industry, it is meaningful from these data to show the drastic reduction of the chip strength due to lack of fine grinding. This is because eccentric rotating between grinding wheel and chuck, or uneven uniformity of diamond particles on wheel or the adhesion between the wafer and tape, might result in insufficient fine grinding depth of in a portion of a wafer. As a result, the chip strength in this portion might be much reduced.

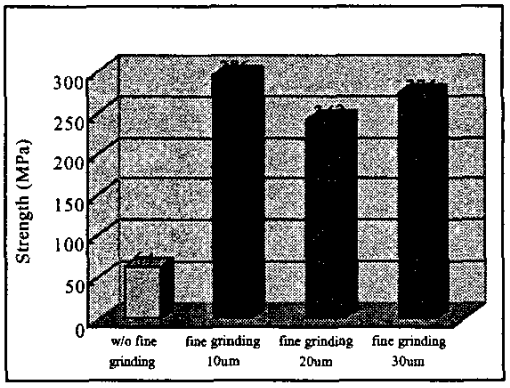


Fig. 8 The effect of fine grinding depth on chip strength

4. POST GRINDING PROCESS

4.1 Polishing vs. plasma etching

In order to eliminate the adverse effect due to grinding mark from mechanical grinding, the polishing process and plasma etching were chosen. Results of three wafers that went through mechanical grinding only, mechanical grinding and additional polishing, and mechanical grinding and plasma etching were presented. The chip dimensions were 11.2mm by 5.45mm. The final thickness for all three wafers was 283um.

The averaged chip strength ,data recorded were 329MPa, 406MPa and 439MPa. Imposing additional polishing process resulted in an improvement of about 24% in the averaged strength, and adding the plasma etching process after

mechanical grinding improved the chip strength by 34%. Although not only the additional polishing but also plasma etching treatments enhanced the chip strength, the result by plasma etching was still higher than that by polishing. This might be due to the fact that plasma etching is near a chemical reaction, whereas polishing is still a mechanical reaction. Although in the polishing process, the severity due to the induced micro-cracks by polishing should be more server than in the situation of plasma etching.

On the other hand, the chip strengths in the weak regions were 144MPa, 371MPa, and 418MPa. These values were 44%, 91%, and 95% of the chip strength averaged from the whole wafer. Thus, introducing of either polishing or plasma etching after the regular mechanical grinding process did not only enhance the average chip strength from the whole wafer but almost completely eliminated the weak region effect. The even better performance in chip strength improvement from the additional plasma etching process is also because of the more complete elimination of the micro-cracks induced in the mechanical polishing process. Consequently, we can expect that chips processed by polishing or plasma etching have better chance to avoid cracking problems after they are packaged.

Although both polishing and plasma etching processes can enhance the chip strength, there are other factors to consider before employing these processes. The advantage of the polishing process is its consistency with the current packaging infrastructure. Thus, it is easier for a packaging manufacturer to adopt this process. However, because heavier pressure than that in the mechanical grinding process is applied on the wafer during the polishing process, this loading to wafer might cause damage in the interfaces between metal and dielectric layers. On the other hand, in the plasma etching process, both chemical etching and ion bombardment are involved to remove the silicon. During chemical etching, gases such as SF_6 or CF_4 are corrosive and they have to be used in a very high level industrial security environment. Such an infrastructure is not yet available in the current packaging industry.

4.2 Polishing depth

Five wafers were used to study the effect of polishing depth on the chip strength of the chips. After the mechanical grinding, they were subjected to no polishing, and polishing of 1um, 2um, 4um and 8um in depth. The samples size for the chips without polishing was 24. The sample size in each wafer experiencing polishing was 10 and was randomly picked from each wafer. The chip size was 11.2mm by 5.45mm, and the final thickness was 283 um (11mils). The averaged chip strengths of polish 1um and 2um were 350MPa and 344MPa, and both were stronger than the strength of the chip without polishing, 315MPa. On the other hand, it is surprisingly to find that when the polishing depth is 4 um and beyond, the strength of the chip recorded was even lower than the strength of the chips without polishing. Although the exact reason for decrease of the chip strength when the polishing depth was larger than 2um was not unknown, it is believe that the excessive pressure impose on the wafer during the long polishing period might induce additional damage to the chip, and the sample size might be too small.

5. CONCLUSION

A detailed strength study on the strength of flash and mask ROM chips has been presented in this paper. Good correlation between the weak region of the chips in 8-inch wafers and the fracture pattern of the chips under three-point bending load were found, which, in turn, was demonstrated in the dual peak pattern in the chip strength probability distribution. The chip strength in the weak region was found to be approximately 60% of the averaged strength of the chip in the whole wafer. Extensive parametric study has been performed in this study. It was found that:

1) Use of a slower backside mechanical grinding speed enhanced the chip strength substantially. In our study, reducing the grinding speed by 50% increased the averaged chip strength by 36%. Both the chip fragment and the strength probabilistic distributions confirmed this chip enhancement trend.
2) In the mechanical grinding process, fine grinding after the coarse grinding increased the chip strength by approximately 5 folds. On the other hand, the results also showed that the chip strength is irrelevant to the fine grinding depth when it was larger than 10 um.
3) In the post grinding process, use of polishing or plasma etching after the mechanical grinding process on wafer enhanced the strength of the chip in the wafer weak region by approximately 3 folds. In addition, although more data are still needed, 2-um thick polishing seemed to be the optimal depth to impose. Excessive polishing induced an adverse effect on the chip strength.

6. ACKNOWLEDGEMENT

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