

行政院國家科學委員會補助專題研究計畫成果報告

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※晶圓廠總體設備效能提升與管理系統子計畫二 ※

※ 工作單元內整體設備效能導向之作業排程 ※

※ Intra-Bay Operation Scheduling for Enhancing Overall ※

※ Equipment Effectiveness (2/2) ※

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計畫類別： 整合型計畫

計畫編號： NSC 89-2212-E002-040

執行期間： 88年8月1日至89年7月31日

總計畫主持人：周雍強 教授

計畫主持人：張時中 教授

本成果報告包括以下應繳交之附件：

- 赴國外出差或研習心得報告一份
- 赴大陸地區出差或研習心得報告一份
- 出席國際學術會議心得報告及發表之論文各一份
- 國際合作研究計畫國外研究報告書一份

執行單位：國立台灣大學工業工程學研究所

中華民國八十九年十月三十一日

晶圓廠總體設備效能提升與管理系統子計劃二： 工作單元內整體設備效能導向之作業排程 Intra-Bay Operation Scheduling for Enhancing Overall Equipment Effectiveness (2/2)

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賴益璋、胡明德。

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一、摘要

本計劃在88年8月1日至89年7月31日的執行期間，針對晶圓廠機臺工作順序及工作單元內晶圓派工的排程問題，進行生產控制方法研究。其中包含排程晶片的設計與實作、單站隨機產流控制之研究、序列式最佳化方法的應用開發、等比例分配機台產能生產控制的分析方法，以及半導體專製廠交單承諾服務建立之研究。具體成果如下：

- I. 設計與實作完成一款少量多樣生產環境的排程VLSI晶片。
- II. 完成以統計製程管制為基準的方法作為產流監看機制的可行性探討。設計出生產速率控制策略，並以馬可夫模型加以分析。
- III. 完成以排序佳化模擬來動態選擇派工法則的初步方法設計與可行性探討。
- IV. 研究出分析方法來對有迴流之生產線上等比例機台產能分配方法加以分析。
- V. 以交單承諾服務為例，展現了所設計的動態製造服務提供機制。

關鍵詞：排程晶片、隨機產流控制、排序佳化模擬、派工法則、動態製造服務提供機制、等比例產能分配

Abstract

During the execution period of this project from August 01, 1999 to July 31, 2000, we conducted research on operation sequencing of cluster tools and wafer scheduling for enhancing OEE of future semiconductor wafer fabs. Subjects of study and development included the design of a VLSI scheduling chip, design and analysis of stochastic production flow control for single station, dynamic scheduling rule selection, analysis method of proportional machine allocation scheme for reentrant line and the creation of available-to-promise service for wafer fabrication. Results are as follows.

- I. Designed, implemented and tested a VLSI chip for Job Shop Scheduling.
- II. Designed and analyzed (1) statistical-process-control (SPC)-based schemes for production flow monitoring and (2) production rate control policies for a single-machine and failure prone system.
- III. Designed and assessed an ordinal optimization (OO)-based simulation approach for dynamic selection of scheduling rules.
- IV. Developed an analysis for analyzing the properties of an iterative and proportional machine allocation scheme over a reentrant line.
- V. Demonstrated the ideas and feasibility of dynamic manufacturing service provisioning mechanism that we designed previously via the creation of an order delivery commitment service.

Keywords: VLSI chip for scheduling, stochastic production control, ordinal optimization-based simulation, dispatching, dynamic manufacturing service provisioning mechanism, analysis of proportional capacity allocation

二、Research Results

I. VLSI Chip for Job Shop Scheduling [P1][P2]

Job shop is a typical environment for manufacturing low-volume and high-variety discrete parts. Good scheduling of when to do what using which resource is critical and challenging to the competitiveness of job shops. The Lagrangian relaxation neural network (LRNN) developed by Luh et al. provides an approach of quantifiable quality and successful industrial applications. To further speed up scheduling for large-scale problems, in this paper, the parallelism of the LRNN approach is exploited for hardware implementation.

We first determine modifications of LRNN

algorithm needed for VLSI implementation by using software simulations (Fig. 1). A baseline hardware architecture (Fig. 2) is then designed, which includes functional modules of state cells, a forward sweep circuit, an instruction decoder, a global memory, and two buses. State cells form a parallel processing architecture for arithmetic operations of LRNN. The forward sweep circuit performs the forward sweep procedure in neuron-based dynamic programming (NBDP), which sequentially interacts with individual state cells. Global data such as due date and problem dimension parameters can be read from and written into the global memory via the global bus. To implement the proposed architecture, designed detailed circuitry and a corresponding instruction set, which allows the algorithm to be implemented in minimum number of instructions and therefore minimizes the required clock cycle time needed. The instruction decoder decodes instruction code to control the operations of modules in the architecture via the control bus.

Correctness of the circuit design is verified via simulations of problem solving and then translated into the physical layout by the standard-cell design procedures. After extensive verification of the functional and timing correctness of the layout, it is fabricated into a chip (Fig. 3). Preliminary test results of the resultant chip show that it is functionally correct under the 3.3V supply voltage at 100MHz operating frequency with a power dissipation of 742.5 mW. The speed performance analysis of the chip indicates a potential of two orders of magnitude in speedup for the job shop scheduling problem solving than using software implementation.

II. Stochastic Production Flow Control: Single Station Case [P3][P4]

Statistical process control scheme

In this task, we first investigate whether statistical process control (SPC) concepts can be applied to production flow control (PFC). We study the simplest but representative M/M/1 queueing system and investigate the detection of the shift in mean arrival and service rate by monitoring the sequence of transformed conditioned cycle times (TCCTs). Monitoring statistics, TCCTs, are derived according to the following innovative ideas. The cycle time changes among individual jobs are independent because of the Markovian property of M/M/1 queue. A transformation is taken to transform CCTs into independent and identically normal distributions. Two SPC-based control schemes, Shewhart and EWMA (Table 1) [4], are applied to monitoring such statistics for shift detection. Performance evaluation by simulation demonstrates that the rate shifts in a M/M/1 system are hardly detected by the Shewhart control scheme. Although they can be detected by EWMA control scheme under a good choice of parameters, the detection by the scheme is not fast enough when applied to a high-variety and low-volume manufacturing system (Fig. 4; Fig. 5). The effect of

applying SPC-based schemes to PFC is therefore skeptical.

Capacity allocation of a single machine

We then study machine capacity allocation of a single machine system for meeting the local performance requirements. In the system, the machine is failure-prone and service rate adjustable. A service rate policy is proposed and analyzed, where different service rates imply the different machine capacity allocated to job processing. The policy assigns a slower service rate to the machine when the number of jobs waiting in the queue is no more than k and a faster mean rate otherwise [1]. The relationship between performance metrics such as system size and the queue length and the control parameters are derived. We also contribute to the derivation of inter-departure time distribution. As a result of the analysis, we derive the statistics of local performance requirements, including mean, variance, and squared coefficient of variation (SCV). The aspect of variability, i.e. second order statistics, as well as mean value is taken into consideration. Numerical experimentation shows that the service rate control policy has good effects of control in both mean and variance of queue length and system size. However, the variance of the inter-departure time is insensitive to service rate control policy.

III. Dynamic Dispatching Rule Selection [P5][P6][P7][P8]

In this task, we exploit the speed of an ordinal optimization (OO)-based simulation tool designed in year one to investigate dynamic selection of scheduling rules for semiconductor wafer fabrication. Although a scheduling rule is a combination of loading wafer release and dispatching rules, this research specifically focuses on dispatching when significant amount of wafers-in-process (WIPs) are held due to engineering causes and when major machine failures occur. Four prominent dispatching rules combined with the wafer release policy of workload regulation constitute a basic set of rule options. The dispatching rule may be weekly selected based on fab states over a four-week horizon. A total of 256 rule options are then evaluated and ranked by the OO-based simulation tool under the performance index of mean cycle time (Table 2) and throughput rate (Table 3). Results demonstrate the value of dynamic rule selection for uncertainty handling, the insightful selection of good rules and the needs for further research.

IV. Analysis of Proportional Machine Allocation Scheme

In the past few years, Chang et al. have developed a fixed-point iteration and proportional resource allocation approach for re-entrant line production. Motivated by its successful field application results, in this task, the properties of the approach for a reentrant line of multiple machine groups and one product type are analyzed. By translating the fixed-point iteration

problem into a polynomial root solving problem, it is proved that there exists a unique machine allocation in this scheme under an arbitrary initial WIP distribution and a constant work release rate at the capacity of the line. Furthermore, by defining a Lyapunov function as a balance measure of the reentrant line WIP distribution and by applying the theory of majorization, it is shown that the reentrant line reaches the status of line balance when the scheme is repetitively applied over time. Although the analysis is under a deterministic model, it provides some insights of the long-term average performance and steady state of a stable stochastic re-entrant line.

V. Design of Available-to-Promise Service Creation Mechanism [P11][P12]

In this task, a dynamic manufacturing service provisioning mechanism (DMSPM) is designed to flexibly create and execute manufacturing services under a virtual fab (VF) enabling framework (Fig. 6). The DMSPM exploits object-oriented (OO) technology to flexibly bind fab objects into services. It consists of four skeleton steps: name mapping, business process binding, resource reservation binding, and service management binding. To assess the feasibility and potential of DMSPM, the order commitment service (OCS) provided by a foundry serves as a study case. A prototype system is designed and implemented to realize DMSPM in the OCS application.

The implementation exploits object-oriented (O.O.) abstraction of a fab and is service process driven. Input data and/or information are mostly available. In this research, both the ATP binding service creation process and the ATP model are implemented using a Computer-Aided Software Engineering tool -- Rational Rose 98. The tool generates the object oriented C++ code of a model expressed in UML (Unified Modeling Language) format. The resource reservation algorithm is coded in visual C++ program and tested. Numerical experimentation results (Table 4) demonstrate the ideas and the practicability of DMSPM for ATP service creation and that DMSPM has a good potential for application to virtual fab and e-business developments.

三、計劃成果自評

本計劃之研究內容包含排程晶片的設計與實作、單站隨機產流控制之研究、序列式最佳化方法的應用開發、等比例分配機台產能生產控制的分析方法，以及半導體專製廠交單承諾服務建立之研究。研究成果雖不全然針對原計劃目標之工作單元內整體設備效能，然作業排程、機臺工作順序、晶圓派工以及生產控制方法之改善對於整體設備效能之提昇有相當的應用價值。研究成果除有部分已發表在國際之研討會外(請參閱：Publication List)，其中有關排程晶片的設計與實作、以排序佳化模擬來動態選擇派工法則的初步方法設計與可行性探討、以及以分析方法來對有迴流之生產線上等比例機台產能

分配的分析成果，亦已分別投稿至國際學術期刊。排程晶片成果正在尋求推廣技轉中。

四、Publication List

- [P1] K.-H. Chen, S.-C. Chang, T.-D. Chiueh, P. B. Luh², X. Zhao, "SIMD Architecture for Job Shop Scheduling Problem Solving," submitted to *ISCAS-2001*, Sydney, May, 2001.
- [P2] K.-H. Chen, "Job Shop Scheduling IC Design and Implementation," MS Thesis, EE Dept., NTU, Taipei, July 2000.
- [P3] I-Chun Chen and S.-C. Chang, "Detecting Production Rate Shift by Using Cycle Time Data: a M/M/1 case," *The 6th International Conference on Automation Technology*, Taipei, Taiwan, ROC, May 2000.
- [P4] I-Chun Chen, "Stochastic Production Flow Control: Single Station Case," MS Thesis, EE Dept., NTU, Taipei, July 2000.
- [P5] B.-W. Hsieh, C.-H. Chen, S.-C. Chang, "Fast Fab Scheduling Rule Selection by Ordinal Comparison-based Simulation," *Proceedings of International Symposium of Semiconductor Manufacturing 1999*, Santa Clara, Oct. 1999, pp.53~56.
- [P6] B.-W. Hsieh, S.-C. Chang and C.-H. Chen, "Dynamic Scheduling Rule Selection for Fab Operations," *Proceedings of 2000 Semiconductor manufacturing Technology Workshop*, June 14-15, Hsin-Chu, pp.202-210.
- [P7] B.-W. Hsieh, S.-C. Chang, and C.-H. Chen, "Dynamic Scheduling Rule Selection for Semiconductor Wafer Fabrication," Submitted to *2001 IEEE International Conference on Robotics and Automation*, Soul, May.
- [P8] B.-W. Hsieh, C.-H. Chen, S.-C. Chang, "Scheduling Semiconductor Wafer Fabrication by Using Ordinal Optimization-based Simulation," submitted to *IEEE Transactions on Robotics and Automation*, July 2000.
- [P9] T.-K. Hwang and S.-C. Chang, "An Optimization-Based Short-term Scheduler for Target Tracking in IC Fabs," *Proceedings of the 6th International Conference on Automation Technology*, Taipei, Taiwan, ROC, May 2000, pp. 903-910.
- [P10] T.-K. Hwang, "Design An Integrated Fab Production Scheduling and Planning Environment for Semiconductor Wafer Fabrication", submitted to *IEEE Transaction on Robotics and Automation*, April 2000.
- [P11] Y.-C. Lai, "Research of Available to Promise Service Creation for Wafer Fabrication," MS Thesis, EE Dept., NTU, Taipei, July 2000.
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- [P13] C.-M. Fan, S.-C. Chang, R.-S. Guo, H.-H. Kung, J.-C. You, H.-P. Chen, Steven Lin and C.-S. Wei, "SHEWMAC: an End-of-line SPC Scheme via Exponentially Weighted Moving Statistics," *Proceedings of 2000 Semiconductor manufacturing Technology Workshop*, June 14-15, Hsin-Chu, pp.268-278.
- [P14] M.-D. Hu and S.-C. Chang, "Translating Fab Cycle Time and Output Targets into Production Control Requirements for Tool Groups," *Proceedings of 2000 Semiconductor manufacturing Technology Workshop*, June 14-15, Hsin-Chu, pp.73-83.

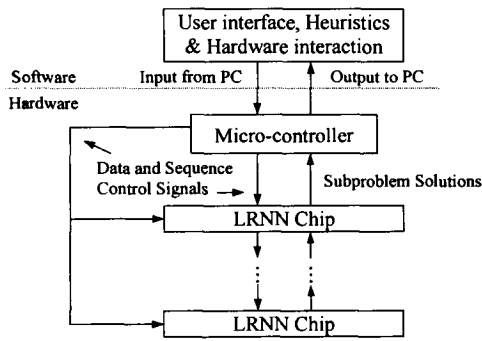


Fig. 1. Overall system architecture

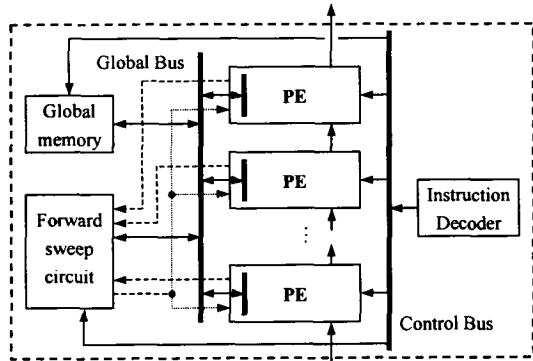


Fig. 2 SIMD architecture of a LRNN Chip

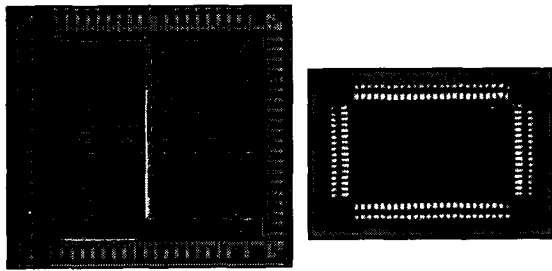


Fig. 3 Chip Layout and the packaged IC

EWMA control chart	
Monitor statistic	$Y_i = \alpha \cdot Z_i + (1 - \alpha) \cdot Y_{i-1}$, where $0 < \alpha \leq 1$
Upper/Lower Control limit	$LCL = \text{Mean} - L\sigma_Y^2$, $UCL = \text{Mean} + L\sigma_Y^2$, where $\sigma_Y^2 = [\alpha / (2 - \alpha)]^{1/2} \sigma_Z^2$

Table 1: EWMA control chart equations

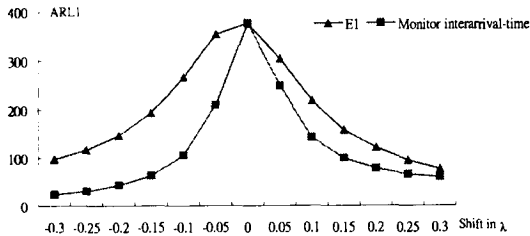


Fig. 4 Comparison of detection speed between monitoring cycle time and inter-arrival time

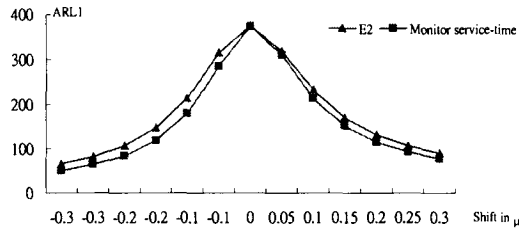


Fig. 5 Comparison of detection speed between monitoring cycle time and service time

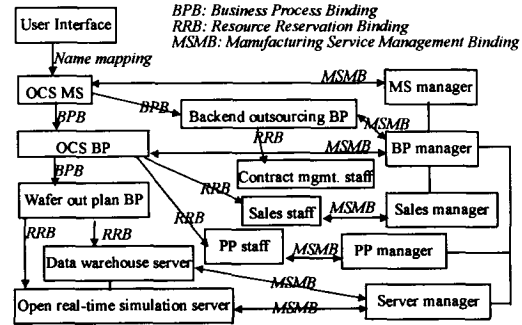


Fig. 6 Order commitment service flow by applying DMSPM

Rank	Rule +	LMCT	%	Throughput
1	C-C-C-C	12.388	-	0.618
2	C-C-C-B	12.395	0.06%	0.616
3	C-C-C-D	12.492	0.84%	0.617
4	B-C-C-B	12.644	2.07%	0.602
5	B-C-C-D	12.653	2.14%	0.607
6	B-C-C-C	12.705	2.56%	0.600
7	A-C-C-C	12.733	2.78%	0.608
8	A-C-C-B	12.740	2.84%	0.607
9	D-C-C-B	12.759	2.99%	0.601
10	C-D-C-C	12.781	3.17%	0.608
131	D-D-D-D	13.628	10.01%	0.610
145	A-A-A-A	13.690	10.51%	0.612

Table 2: Dynamic Rule Selection under Engineering Holds (ranked by LMCT)

+ Rule-A, Rule-B, Rule-C, and Rule-D represent WR-FSVCT, WR-FIFO, WR-LDF, and WR-OSA respectively.

Rank	Rule	Throughput	%	LMCT
1	A-C-D-D	0.621	-	13.514
2	A-A-B-A	0.621	0.00%	13.970
3	A-A-D-A	0.620	0.16%	13.995
4	A-C-C-A	0.619	0.32%	13.279
5	A-B-C-B	0.619	0.32%	14.043
6	A-B-B-D	0.619	0.32%	14.170
7	C-C-C-C	0.618	0.48%	12.388
8	D-D-C-C	0.618	0.48%	13.106
9	D-D-C-A	0.618	0.48%	13.605
10	D-B-A-D	0.618	0.48%	13.642
46	A-A-A-A	0.612	1.45%	13.690

Table 3: Dynamic Rule Selection under Engineering Holds (ranked by throughput)

◆ Case I

■ Binding Service Creation

Tech.	0.25 μm	0.28 μm	0.35 μm	0.25 μm	0.28 μm	0.35 μm
Request Due	20	20	20	10	10	10
Forecasted Due	20	20	20	10	10	10
W/S Date	8	10	13	1	1	3

◆ Case III

■ Bottleneck: Station 5, 6, 7

Lots	20	35	50	100	120
Capacity Allocation	PULL	PUSH	PUSH	PUSH	PUSH
Forecasted Due	15	16	18	22	24
W/S Date	2	1	1	1	1

Table 4: Two Experimentations with Prototype System
