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## Low voltage BiCMOS dynamic logic gates

H.P. Chen and Y.P. Wu

*Indexing terms: BiCMOS integrated circuits, Logic gates*

A low-supply-voltage BiCMOS logic gate is presented which can be used to form a pipelined system using the two-phase non-overlapping clocks. The new BiCMOS dynamic logic gates have no DC power dissipations and they have full voltage swings. It has been shown that the use of the described feedback technique provides a lower gate delay than previously reported low-voltage designs.

**Introduction:** Performance degradation at low voltage is verified to be a major limiting factor for BiCMOS circuits. The reduced swing degrades the speed of the driven gates, especially when the supply voltage is scaled down. Another disadvantage of the reduced swing is the noise margin reduction. To overcome the drawback, full-swing complementary designs using complementary bipolar device have been recently reported [1]. However, the advantages of the C-BiCMOS are considerably offset by the additional process complexity and cost for the *pnp* bipolar fabrication. In this Letter, a circuit technique using a feedback inverter to improve the BiCMOS logic swing and allow low voltage operation is proposed. This design offers an effective speed improvement over other existing designs, such as merged BiCMOS (M-BiCMOS) [2] and quasi-complementary BiCMOS (QC-BiCMOS) [3], without using extra processing steps in an *npm*-only BiCMOS process.

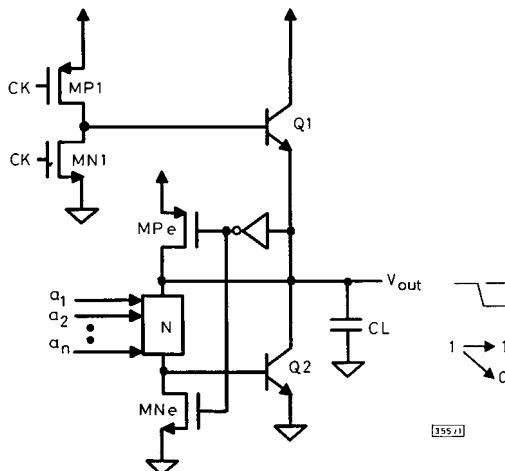


Fig. 1 Proposed BiCMOS dynamic N-cell

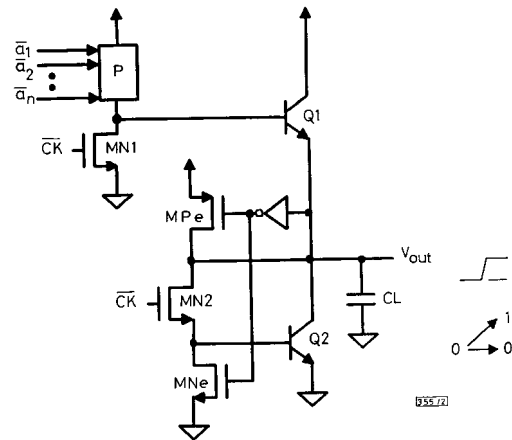


Fig. 2 Proposed BiCMOS dynamic P-cell

**Circuit:** The full-swing operation can be realised by using a feedback inverter as shown in Figs. 1 and 2. To organise to form a dynamic pipelined system [4], the logic gates can be divided into two types, the *N*-cell and *P*-cell. The operation of these two gates is as follows. As shown in Fig. 1, the *N*-cell has two operation phases, that is, precharge phase and evaluation phase. During the precharge period when the *CK* signal is low, *MN1* is turned off, and the current supplied by *MP1* is fully used to drive *Q1*. The output node is charged quickly to a value higher than  $V_{dd} - V_{BE}$ . Using the feedback inverter, the output node is pulled up to  $V_{dd}$  through *MPe*. After the precharge period when the *CK* signal goes high, *MNe* is turned off and the base of *Q1* is discharged through *MN1*. Hence, short circuit current in *Q1* and *Q2* can be avoided during the next pull-down thereby reducing unnecessary power dissipation. The output logic value is determined by the logic circuit block *N*, which is composed of *n*MOS transistors. Assuming a high-to-low transition at the output node due to the logic value, the output voltage decreases until it reaches  $V_{BE}$ . *MNe* is turned on in this time. This could lead to the saturation of *Q2* causing the output voltage to fall to  $V_{CEs}$  close to 0V. As shown in Fig. 2, the operation of the *P*-cell can be similarly explained as follows. During the precharge phase when  $\overline{CK}$  is high, *Q1* is turned off due to the turned on *MN1* and the output node is discharged to set up to low level, close to 0V. During the evaluation phase when  $\overline{CK}$  is low, *MN1* is turned off and the base of *Q2* is discharged by *MNe*. The output logic value is determined by the logic circuit block *P*, which is composed of *p*MOS transistors.

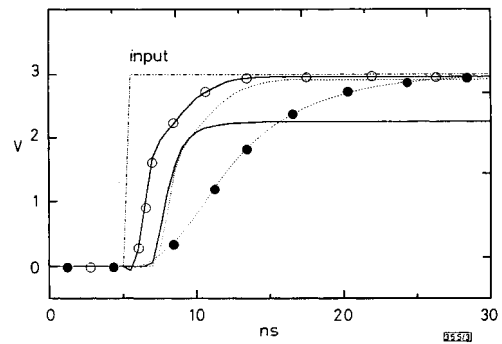
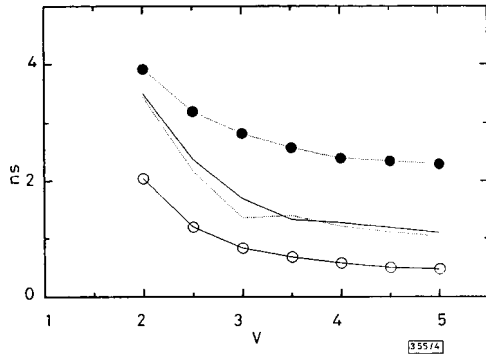


Fig. 3 Transient waveforms of the four inverters

---●--- CMOS  
 - - -○- - M-BiCMOS [1]  
 ····□···· QC-BiCMOS [2]  
 - · - · -◇- · - proposed BiCMOS (N-cell + P-cell)

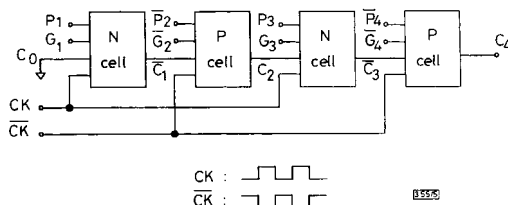
**Comparisons:** To compare the performance of the proposed BiCMOS circuit with those of CMOS, M-BiCMOS, and QC-BiCMOS circuits, the series of two inverters of each BiCMOS circuit is sim-

ulated. The MOS device threshold voltages are  $\sim\pm 0.7V$ . Fig. 3 shows the simulated transient waveforms of those logic gates (with 0.5pF load). As indicated in the Figure, the gate delay time of the proposed BiCMOS circuit is 2.21ns, which means the response speed of the proposed circuit is more than three times that of a CMOS inverter (7.1 ns). The proposed BiCMOS circuit can also be seen to provide a faster response speed than the other two BiCMOS designs. Fig. 4 shows the simulated dependence of the gate delay on  $V_{dd}$  for those four equal area inverters (with 0.5pF load). The proposed BiCMOS circuit is almost 160% faster than a CMOS circuit at 3V and also considerably faster than other *npn*-only BiCMOS logic gates.



**Fig. 4** Gate delay against supply voltage for different designs (load = 0.5pF)  
 - - ● - - CMOS  
 - - - - M-BiCMOS [1]  
 - - - - QC-BiCMOS [2]  
 - - ○ - - proposed BiCMOS

**Application:** As shown in Fig. 5, the *N*-cell and *P*-cell are replaced alternatively in the BiCMOS dynamic CLA circuit.  $P_i$  and  $G_i$  are the carry propagation and carry generation, respectively. After the precharge/predischarge phase, each output node is set high and low in the dynamic circuit alternatively, such that the output node of the *N*-cell/*P*-cell turns off the *p*MOS/*n*MOS in the next stage and the output node of each stage is not affected by the previous carry signal. During the evaluation phase, the output node of each stage is determined by the logic circuit. Thus, it is realised that the new dynamic BiCMOS circuit is fully racefree. The two types of cells should be connected alternatively in a system, thus forming an extensively pipelined structure. In fact, the arrangement of *N*-cell/*P*-cell can be used in any large-scale pipelined dynamic system to shorten the propagation delay time associated with complex irregular routing [5].



**Fig. 5** Example application of proposed dynamic logic gate

**Conclusion:** A novel BiCMOS dynamic logic gate is presented, which is suitable for organisation in a pipelined system. Without special IC processing, the new BiCMOS dynamic logic gates enhance the speed performance over other types of low voltage *npn*-only BiCMOS designs. Even at 2V, it is 100% faster than a CMOS design (with 0.5pF load). The proposed BiCMOS logic gates provide an absolute speed advantage, which is very helpful for low-supply-voltage operation.

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## Deep high-dose erbium implantation of low-loss silicon oxynitride waveguides

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*Indexing terms:* Optical waveguides, Ion implantation, Photoluminescence

Photoluminescence studies of low-loss SiON waveguides deeply (2.8MeV) implanted with erbium at concentrations up to 1atm.% are reported. Rapid thermal annealing at 900°C is found to repair most of the implantation damage and results in a 5.3ms  $^4I_{13/2}$  lifetime for 0.25atm.% Er concentration. Measurements in 1atm.% doped samples show significant erbium ion-ion interactions.

**Introduction:** A strong demand exists for active silicon-based optoelectronic devices, such as amplifiers, zero-loss splitters and so on, due to their technological compatibility with available silicon electronics. Silicon oxynitride (SiON) could be among the promising materials for such devices. Recently, very low-loss optical SiON waveguides have been made by plasma-enhanced chemical vapour deposition (PECVD) on 4 inch wafers [1]. The optical index of SiON can be varied from that of SiO<sub>2</sub> (i.e.  $n \approx 1.46$ ) to almost that of Si<sub>3</sub>N<sub>4</sub> ( $n \approx 2.2$ ) by changing the portion of nitrogen in the compound during growth. Thus, optical waveguide mode size can be controlled without changing the waveguide geometry. Unfortunately, no results on rare-earth doping of SiON in order to obtain optical amplification have been published to date. From this viewpoint, ion implantation appears to be a useful investigation technique because it allows the incorporation of erbium ions, among others, in virtually any solid host material [2, 3]. Moreover, the Er concentration profile can be easily controlled while the maximum concentration can exceed the limit of solubility.

In this Letter, we report for the first time on the photoluminescent characteristics of low-loss SiON waveguides heavily doped with Er by using deep ion implantation.

**Experimental setup:** A standard 100 mm diameter silicon wafer with a 3μm layer of thermally grown SiO<sub>2</sub> was used as a substrate. A 1.18μm thick SiO<sub>1.5</sub>N<sub>0.6</sub> guiding layer was deposited using PECVD. Losses as low as 0.05dB/cm were measured at 633nm for 7cm long waveguides. One optical mode was supported at both 0.98μm and 1.5μm wavelengths. No transverse optical confinement structure was realised on the samples.

The waveguides were implanted with 2.8MeV Er ions at room temperature. The implantation energy was chosen to provide maximum erbium concentration at a depth of 0.6-0.7μm, the latter corresponding to the position of the maximum of the 0.98μm pump mode spatial distribution. Two implantation doses were used:  $5 \times 10^{15}$ cm<sup>-2</sup> and  $2 \times 10^{16}$ cm<sup>-2</sup>, which resulted in ~0.25atm.% and ~1.0atm.% peak Er ions concentrations, respectively.

Thereafter, the implanted waveguides were repeatedly annealed