Design and Implementation of a Low-Voltage Fast-Switching Mixed-Signal-Controlled Frequency Synthesizer

Tzi-Dar Chiueh, Jin-Bin Yang, and Jen-Shi Wu

***Abstract*—A new frequency synthesizer based on combining the analog phase-locked loop (PLL) and the all digital PLL (ADPLL) is presented. The frequency synthesizer achieves high frequency resolution, broad frequency range, high switching speed, and low supply voltage. The oscillator is controlled by both the digital control word and the control voltage of the analog PLL. It is an array oscillator implemented by symmetric load differential inverting buffers which provide better rejection to supply noise and fabrication variance. Fractional-N divider and delay interpolation technique are employed to enhance the divider resolution without inducing jitter. A binary search algorithm is used to find the proper digital frequency control word, which can be saved for later use and greatly speed up the frequency switching process. Fabricated using a 0.6-μm SPTM CMOS process, the synthesizer achieves a frequency range of 54–154 MHz with a frequency error less than 1 ppm and a frequency switching time less than 10 μs. The chip consumes very little power and draws 47 mW from a 2-V supply voltage.**

***Index Terms*—Frequency synthesizer, mixed-signal control, phase-locked loop (PLL).**

I. Introduction

WIRELESS transmission almost always suffers severe interferences from various sources. Spread spectrum techniques have been applied successfully to combat the impairments in all sorts of wireless channels. Specifically, frequency hopping spread spectrum (FHSS) approach has been adopted by several commercial wireless communication standards, such as IEEE 802.11 wireless LAN, Bluetooth (http://www.bluetooth.com), and HomeRF (http://www.homerf.org). Fig. 1 shows the block diagrams of the transmitter and the receiver in a frequency hopping spread spectrum system. In a frequency hopping spread spectrum system, the available channel bandwidth is subdivided into frequency slots. Selection of these slots in each time interval is controlled by a PN code generator. The receiver must know and synchronize itself with this PN code to correctly demodulate the incoming signal. Since the PN code generator in a FHSS system switches carrier frequency frequently (as fast as once every 1 ms), a fast-switching and stable (low-jitter) frequency synthesizer for generating the hopping carrier frequency is essential to FHSS transmitters and receivers.

Conventionally, frequency synthesizers are designed using analog phase-locked loop (PLL) [1] or direct-digital synthesizer (DDS) [2]. The analog approach provides higher frequency resolution, but suffers slow acquisition. On the contrary, the digital approach has low frequency range and poor frequency resolution, but can achieve very fast switching.

An analog PLL usually includes a voltage control oscillator (VCO) to generate a periodic signal synchronized to a particular reference signal. The frequency of the periodic signal is controlled by an analog voltage, which is adjusted through a feedback loop. Generally, the feedback loop includes a phase frequency detector (PFD) and a loop filter. The PFD is used for generating a phase error signal which represents the phase difference between the periodic signal and the reference signal. The loop filter and a charge pump circuit are used for integrating the phase error generated from the PFD to output a control voltage. This control voltage generated from the loop filter is fed back to control the frequency of the periodic signal from the VCO. The control of this voltage over the frequency of the periodic signal is continuous and, therefore, the analog PLL can provide a good frequency resolution. However, the loop bandwidth of the analog PLL has to be carefully designed to ensure that the oscillation signal from the PLL have a proper phase noise level and a fast settling process.

In addition to the traditional analog PLLs, there is another approach called all-digital (ADPLL) [3]. The ADPLL employs a digital-controlled oscillator (DCO) to replace the voltage-controlled oscillator (VCO) in traditional PLLs. Because a special algorithm is used to search for the digital control word in the digital controlled oscillator, the digital PLL can capture the frequency in only 50 clock cycles, much faster then if analog PLLs are used. Although the ADPLL is very agile, it still has some problems, namely, poor frequency resolution and nonuniform frequency step size.

In this paper, a frequency synthesizer architecture that possesses both the advantages of high frequency resolution of analog PLLs and fast frequency acquisition of digital PLLs is proposed. The kernel of the synthesizer is a mixed-signal-controlled PLL which employs two types of control: analog and digital. With the flexibility and programmability of a

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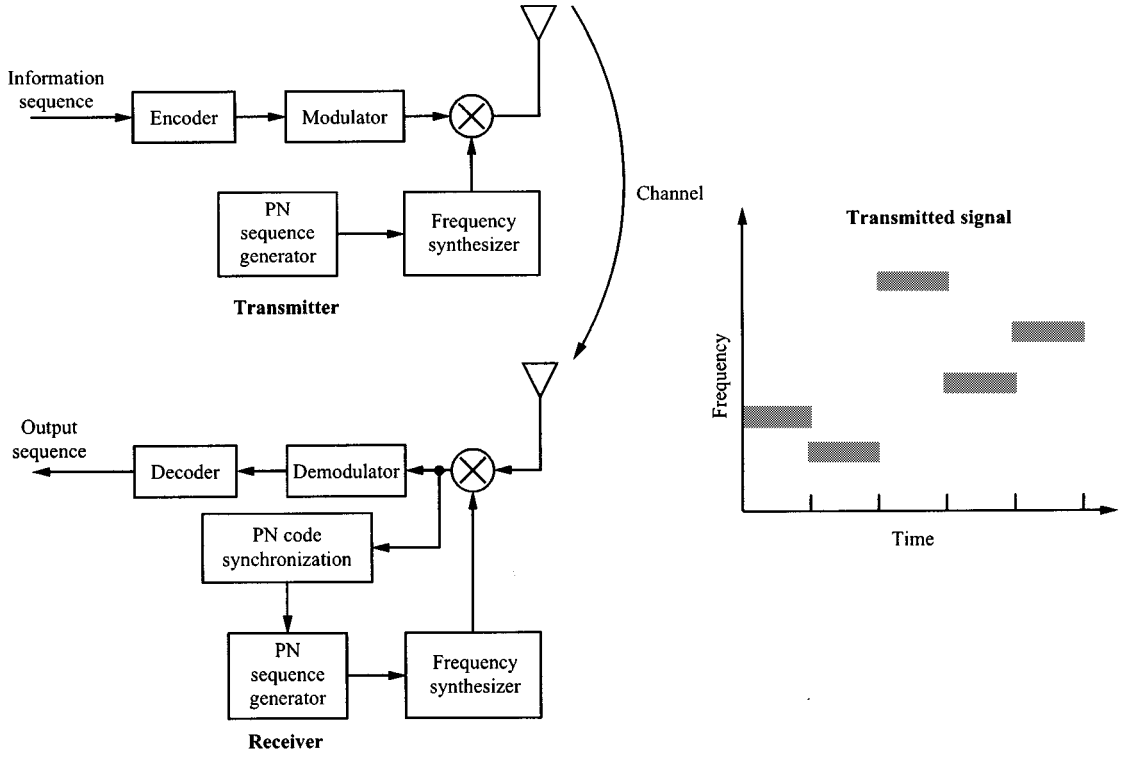


Fig. 1. Block diagram of a FHSS system.

digital controller, the new frequency synthesizer can acquire a frequency control word for coarse frequency acquisition. With the high resolution property of the accompanying analog PLL, the new frequency synthesizer can also provide high frequency resolution. With this new mixed-signal control concept, frequency synthesizers with better performance can be designed. Moreover, this concept can be applied to various other existing PLLs.

The rest of the paper is organized as follows. Section II presents the architecture of the proposed mixed-signal-controlled frequency synthesizer. Then the new mixed-signal PLL, mixed-signal-controlled oscillator (MSCO), and a digital frequency acquisition algorithm are discussed. In Section III, detail circuit design and simulation results of the proposed frequency synthesizer are given. The fabricated frequency synthesizer chip and its measurement results are described in Section IV. Section V then concludes this paper.

II. Architecture of the Mixed-Signal-Controlled PLL Frequency Synthesizer

For the aforementioned FHSS applications, the frequency range is between 2400–2500 MHz. To include a VCO with such a high frequency on chip is quite difficult, so an offset VCO approach [4] is adopted. In this approach two oscillation signals, one from a fixed oscillator and the other from a VCO, are mixed to generate a final oscillation signal whose frequency is the sum of the frequencies of these two signals. With this, the frequency range of the desired frequency synthesizer can be made attainable by an on-chip VCO. In this paper, the proposed frequency synthesizer can generate oscillation signal from 54 to 154 MHz with a frequency step of one MHz.

The block diagram of the proposed mixed-signal controlled frequency synthesizer is shown in Fig. 2. It consists of a MSCO using an array structure, nine fractional-N frequency dividers, multiplexers controlled by the delay-interpolation circuit, a phase frequency detector, a charge-pump PLL for analog offset control, and a digital controller for digital frequency control.

The MSCO consists a control current generator and an array current-controlled oscillator. Nine signals which are equally spaced in phase will be generated by the array oscillator. These signals are frequency divided individually by nine identical fractional-N frequency dividers whose divisors are controlled by the delay-interpolation circuit. Therefore, nine signals are divided by a fractional number N and are still equally spaced. Then, the nine frequency-divided signals are multiplexed by the delay-interpolation circuit, thus generating a low-jitter frequency-divided signal. The phase frequency detector will compare this signal with the reference signal. According to the phase difference between these two signals, *UP/DN* pulses are generated.

For the analog feedback loop, these pulses control the charge-pump to charge or discharge the loop filter. Then the voltage output of the loop filter is transformed into an offset current I_{OFFSET} by a voltage-to-current converter. For the other digital feedback loop, the *UP/DN* pulses are translated into *SUB* and *BYPASS* signals first. The *SUB* signal tells the digital controller to increase or decrease the control word, while the *BYPASS* signal represents leaving the control word unchanged. With these two signals, a binary search algorithm can locate the correct control word (the one that generates a

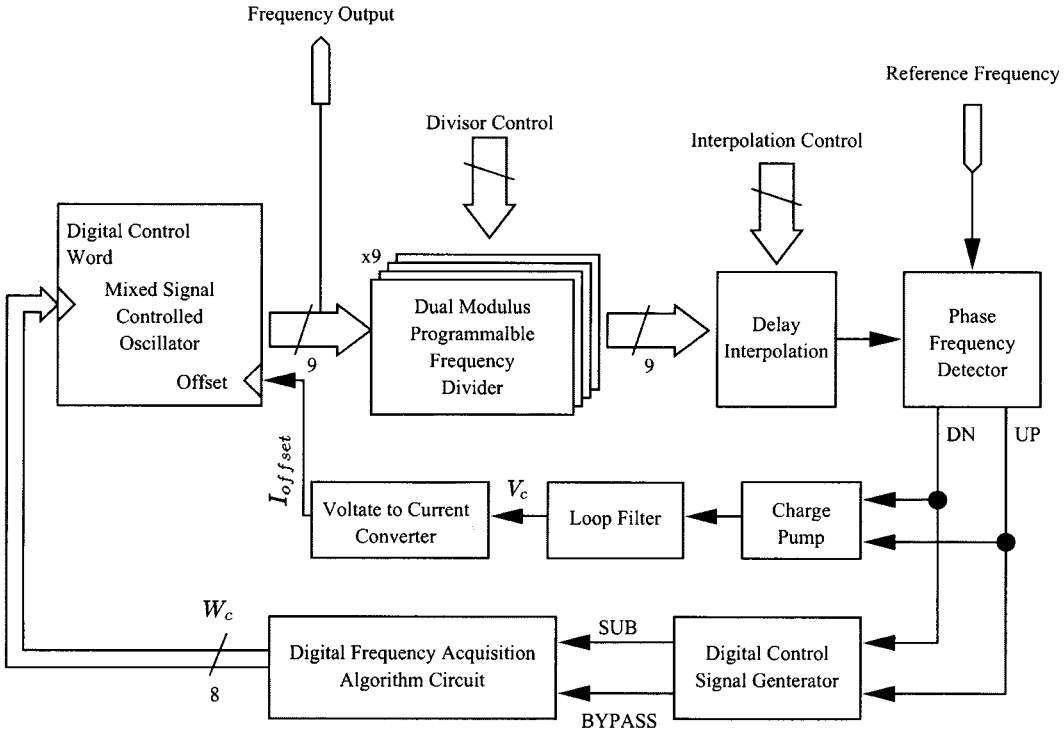


Fig. 2. Block diagram of the proposed mixed-signal-controlled frequency synthesizer.

frequency nearest the desired frequency) very quickly. The two control signals (one analog and one digital) are then combined to control the MSCO. However, note that the two control loops do not operate simultaneously. The digital loop is allowed to operate first, then its control signal is frozen and the analog loop starts to work. Therefore, the stability of the proposed frequency synthesizer is similar to that of the traditional analog PLL.

A. MSCO

The core of the new mixed-signal-controlled frequency synthesizer is an oscillator controlled by both digital and analog signals. This design combines both the advantages of digital-controlled oscillators and voltage-controlled oscillators. In a digital-controlled oscillator, the output frequency is determined by the delay of each DCO cell. The control word turns on or off the MOS devices, thus changing their drain currents and controlling the time to charge or discharge their load capacitance. Therefore, the output frequency is controlled by the control word. Unfortunately, the frequency resolution of a DCO is limited by the word length of its control word, especially at low frequency. To overcome this drawback, another analog offset current is added to increase the frequency resolution, as shown in Fig. 3. This newly designed oscillator is called the MSCO. The MSCO is composed of the following three components: a digital-to-current converter, a voltage-to-current converter, and a current-controlled oscillator.

Digital control of the MSCO can be viewed as a current-output digital-to-analog converter (DAC) that converts the digital control word into an analog current. With such a DAC, changes in the control word directly reflect on the control current, thus switching the output frequency quickly. Analog control of the MSCO provides an offset current to the current-controlled oscillator, enhancing its frequency resolution and at the same time canceling the nonideal factors, such as process variation, device mismatch, etc. Since the oscillator control signal from the loop filter in the analog PLL is a voltage signal, a voltage-to-current converter is needed.

The current-controlled oscillator generates a wide-frequency-range clock signal controlled by the currents supplied from the digital-to-current and the voltage-to-current converters. To achieve the goal of low phase noise and high frequency switching speed, we use an array oscillator [5] as the current-controlled oscillator in the proposed MSCO. The structure of an array oscillator is a two-dimensional array of *dual-input* inverting buffers. Rings of delay buffers that extend horizontally are also coupled vertically though the coupling inputs. By connecting the top array nodes and the bottom array nodes in a particular manner, an array oscillator is formed. The coupling connections force the rings to oscillate at the same frequency and maintain a precise delay between each coupled rings. The cyclic connections make the total delay from top to bottom equals to some multiples of the buffer delay.

In our design, we choose a 3×3 array oscillator using differential-input buffers. Therefore, 18 phases can be generated and we choose the noninverting nine phases as the outputs. The structure of our array oscillator is shown in Fig. 4, where nodes *Ti* are connected to nodes $B(i+2)$, respectively.

B. Delay Interpolation

To provide higher frequency switching speed, we need a high-frequency reference clock signal, which entails that fractional-N frequency divider is preferred. However, the major drawback of the fractional-N frequency divider, spurious

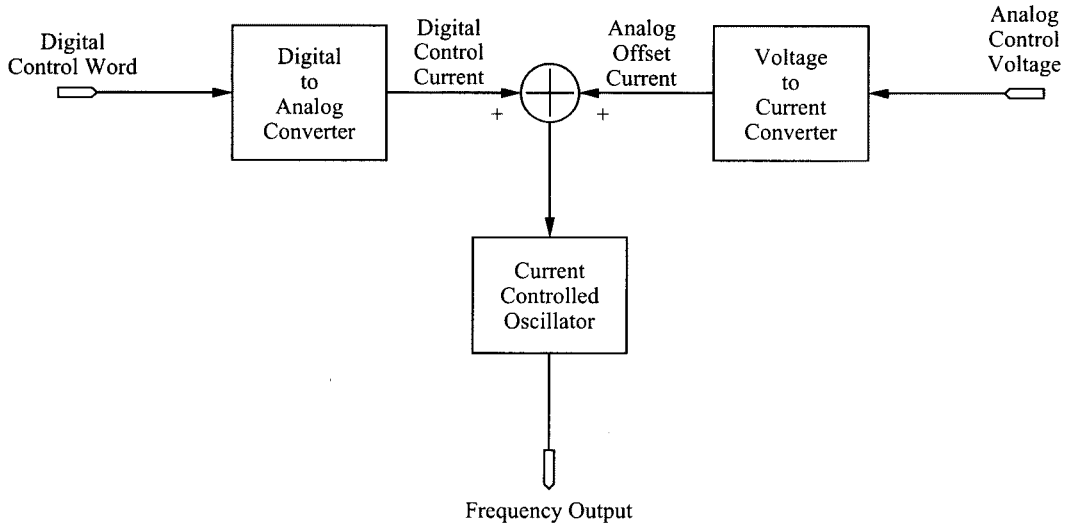


Fig. 3. Block diagram of the proposed MSCO.

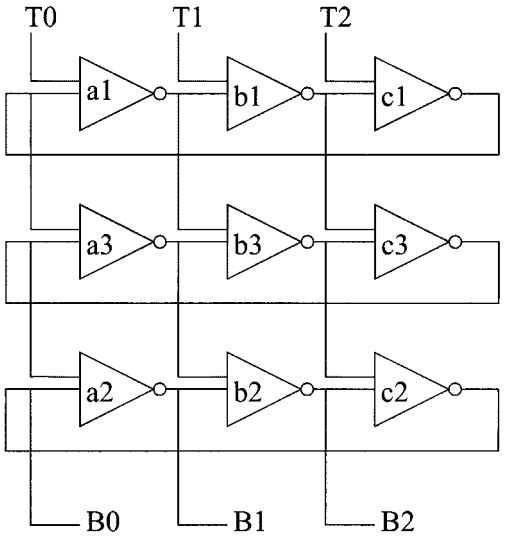


Fig. 4. Circuit diagram of the array oscillator.

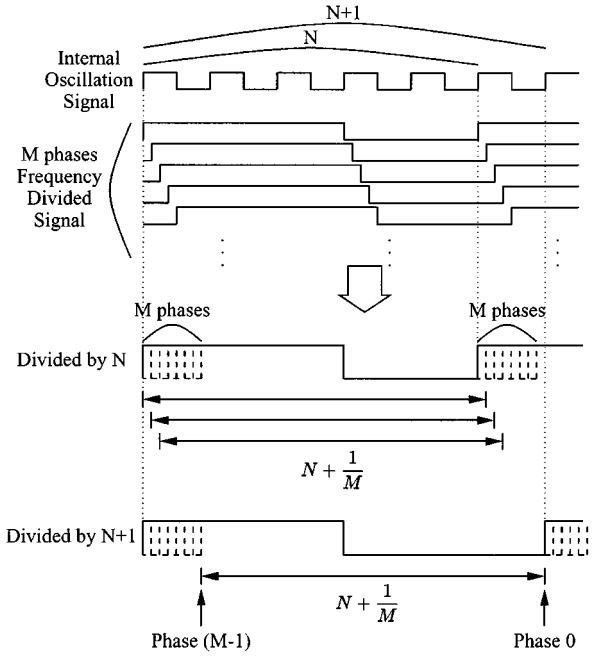


Fig. 5. Waveforms in the delay interpolation block.

frequency components, makes it inadequate for low-jitter frequency synthesizers [6], [7]. Delay-interpolation is an approach that can eliminate spurious frequency components [8].

In a fractional-N divider, the frequency of the input oscillation signal is divided by N or $N+1$. Therefore, its output may have several periods of N input clock cycles followed by several period of $N+1$ input clock cycles so that on average the output signal has a period of N plus a fractional number of input clock cycles. The concept of delay interpolation is to select among a group of evenly spaced nonperiodic oscillation signals and reconstruct (interpolate in time domain) a periodic oscillation signal (see Fig. 5).

The MSCO in the proposed frequency synthesizer produces nine same-frequency oscillation signals whose phases are evenly spaced in a period. Passing these nine oscillation signals through nine identical fractional-N frequency dividers will generate nine frequency-divided signals, each delayed from another by one-ninth of the input clock cycle. The interval between a rising edge of the earliest signal and the next rising edge of the second-earliest signal is $N+1/9$ input clock cycles. So if the output of the delay interpolater switches from the earliest signal to the second earliest signal during this interval, and then to the third-earliest signal at a later time, and so on, a periodic signal with period $N+1/9$ clock cycles can be obtained. In the same vein, one can generate periodic signals with period $N+i/9$ clock cycles, $i=0, 1, \ldots, 8$.

In our design, we choose $6 \leq N \leq 18$. Therefore, with a 9-MHz reference frequency, the synthesized frequency range runs from 54 to 154 MHz and the frequency spacing is 1 MHz.

C. Digital Frequency Acquisition Algorithm

The digital frequency acquisition controller takes in two digital control signals and outputs a digital frequency control word. The *SUB* signal represents whether the frequency-divided and

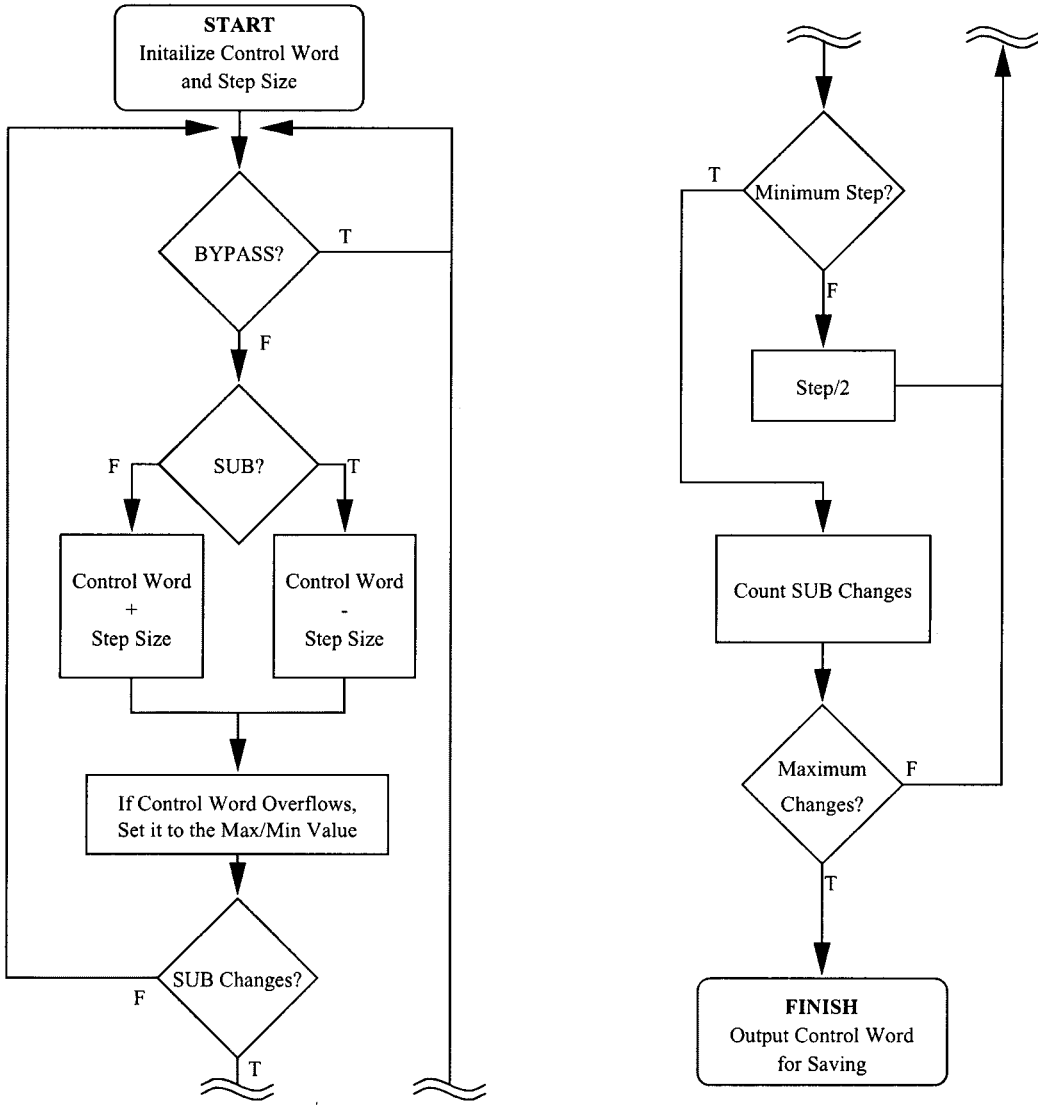


Fig. 6. Flow chart of the frequency acquisition algorithm.

delay-interpolated clock signal leads or lags the reference signal (9 MHz). We use another signal, *BYPASS*, to indicate if the digital frequency control word needs to be adjusted. When the *BYPASS* signal is low, the control word will be modified according to the polarity of the *SUB* signal.

The flow chart of the frequency acquisition algorithm is illustrated in Fig. 6. A binary search strategy is employed in the acquisition of the frequency control word. In the beginning, the control word and the step size are set to predefined values. When the *BYPASS* signal is low, the control word will be incremented or decremented by the step size. However, when the search direction is reversed, i.e., the *SUB* signal changes sign, the step size will be halved, thus effectively reducing the control word search range. Finally, when the step size reaches a predefined minimum, the step size is fixed at that value. A counter starts to count the number of polarity changes in the *SUB* signal after the step size reaches the minimum value. Searching the target control word using a minimum step size ensures that the search process will stop. Thus, the target control word generating the correct frequency can be found quickly. Once the digital frequency acquisition is achieved, the analog PLL is started to further tune the control current of the mixed-mode-controlled oscillator. In addition, this digital control word can be saved for later use. Next time when the same frequency needs to be synthesized, the corresponding control word can be loaded back. Hence, no digital acquisition process is required and the acquisition process can be sped up tremendously.

III. Circuit Design

A. MSCO Circuit

The core of the MSCO is made up of the following three parts: a digital-to-current converter, a voltage-to-current converter, and a current-controlled oscillator.

The digital-to-current converter converts the digital control word into an analog current and is implemented using a flash-type current-output DAC. With such a digital-to-analog converter, changes in the control word directly reflect on the output current, thus switching the oscillation frequency swiftly. The voltage-to-current converter is needed because the analog

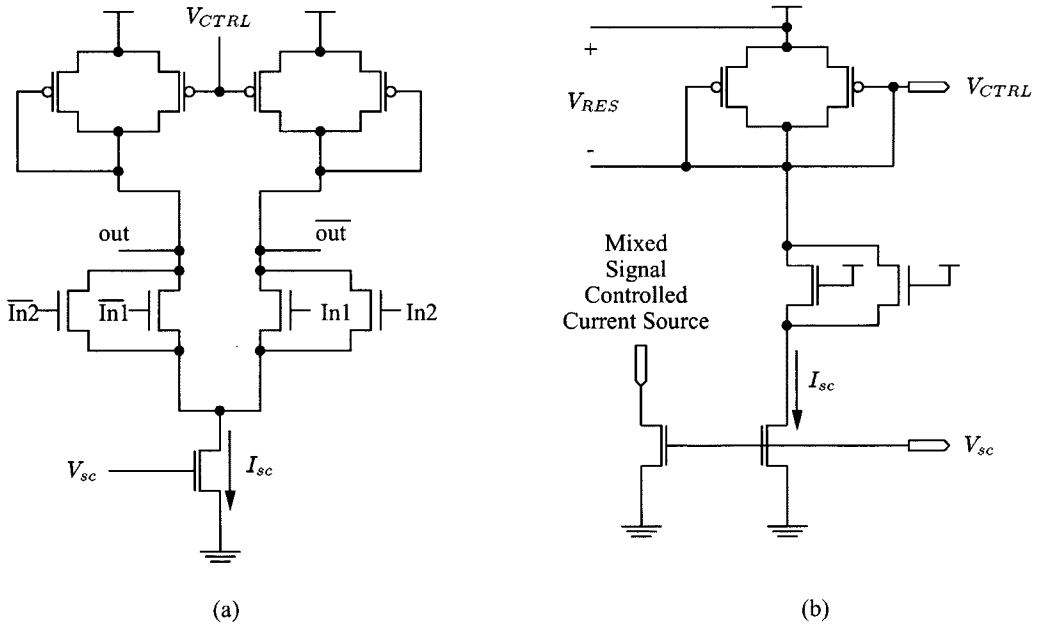


Fig. 7. (a) Basic delay stage of the array oscillator. (b) Bias generation.

control signal from the analog PLL loop filter is in the voltage form, so it needs to be converted to a current so as to be combined with the digital control signal (now in current form after the aforementioned DAC). The voltage-to-current converter is implemented by a simple MOS transistor working as the transconductance device that accomplishes the voltage-to-current conversion.

For the current-controlled oscillator, a 3×3 array configuration is adopted. The delay cell is a differential-mode dual-input inverter. To reduce noise coupled from the supply rail, a special type of load circuit, called symmetric load [9], is adopted. Although the linearity performance of the symmetric load is not perfect, its symmetric characteristic still provides good rejection to noise. The symmetric load is composed of a diode-connected PMOS device in shunt with an equal-sized PMOS device [see Fig. 7(a)]. The I–V characteristic is symmetric about the center of the voltage swing, thus it is called a *symmetric* load. V_{CTRL} is the bias voltage of the PMOS device. It controls the resistance of the symmetric load, thus controlling the delay of the dual-input inverter.

Fig. 7(a) shows the detail circuit diagram of the delay cell. In this cell, each input MOS device is divided into two MOS devices in shunt, resulting in a differential-mode dual-input inverting buffer. Two variables, V_{CTRL} and V_{sc}, control the delay of the delay cell. In addition, the current source needs be tuned according to the control voltage of the symmetric load to maintain proper voltage swing. Otherwise, first order noises can not be canceled. Fig. 7(b) illustrates the bias-generation circuit for the two bias voltages V_{CTRL} and V_{sc}. Note that I_{sc} mirror the sum of the two control currents, one from the digital loop and the other from the analog loop. With increasing I_{sc}, the driving capability of each delay cell is enhanced, thus reducing the delay and increasing the oscillation frequency.

Since the performance of a frequency synthesizer depends largely on its controlled oscillator, we conduct post-layout

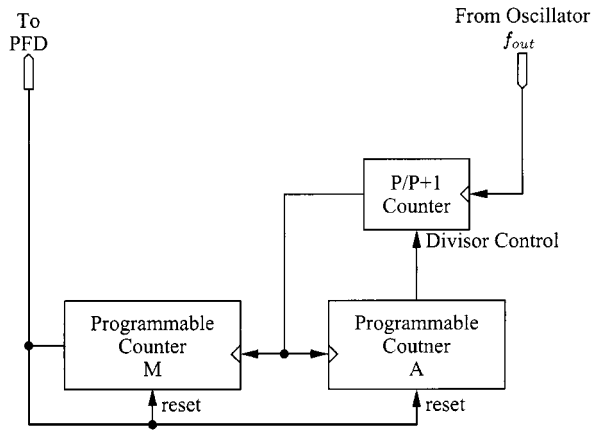


Fig. 8. Block diagram of the dual-modulus frequency divider.

circuit simulation for the proposed MSCO. Simulation results show the nine phases generated by the array oscillator are evenly spaced in one clock period. Further simulations reveal that with a 2-V supply voltage the oscillation frequency scales monotonically with the control current up to over 150 MHz. In addition, the output frequency scales almost linearly with the digital control word, from 20 to 160 MHz.

B. Frequency Divider

In the fractional-N frequency divider, we need a frequency divider that can divide the input oscillation signal at more than 150 MHz with 2-V supply voltage. We use the dual-modulus frequency divider [2] which includes a counter that has two possible counts and can operate only for integer divisors.

Fig. 8 shows the block diagram of the dual-modulus frequency divider. A dual-modulus divider consists of three counters, which are $P/P+1$, M, and A counters. The divisor of $P/P+1$ counter is controlled by the overflow signal of

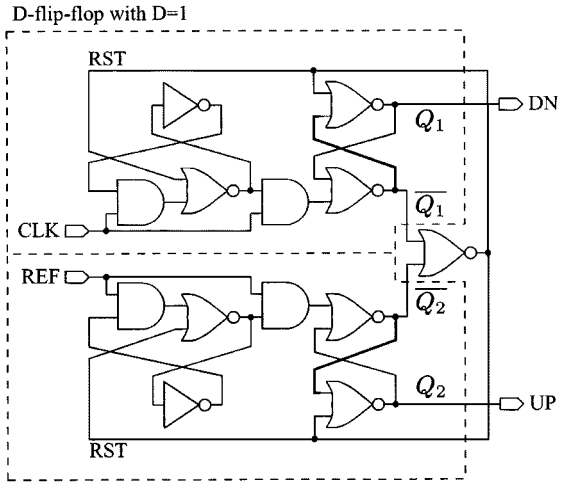


Fig. 9. Circuit diagram of the tri-state phase frequency detector.

the A counter. At the beginning of a divide cycle, both the M and A counters are set to zero, and the divisor of the $P/P+1$ counter is set to $P+1$. The output of the $P/P+1$ counter triggers both the M and A counters to increment by one. When the A counter overflows, the divisor of the $P/P+1$ counter is set to P. From then on, only the M counter is triggered and increments, whereas the A counter stays overflowed until the M counter also overflows. When the M counter also overflows, both the M counter and the A counter are reset back to zero and the divisor of the $P/P+1$ counter is also reset to $P+1$, completing a divide cycle. Therefore, the divisor of the dual-modulus frequency divider is given by

$$N = (M-A)P + A(P+1) = MP + A. \tag{1}$$

Since the reference frequency is 9 MHz, the divisor of the dual-modulus frequency divider is in the range of 6 to 18. We choose 2 as the value of P. The resultant range of M is from 3 to 9 and that of A is from 0 to 1. The A counter, counting only 0 or 1, is replaced by a multiplexer whose output controls the divisor of the 2/3 counter. Due to circuit speed concern at a low-supply-voltage setting, the 2/3 counter is simplified to some combinational logic and true single-phase-clock (TSPC) D-type flip-flops [10], [11]. Moreover, the M counter is implemented using synchronous counter made up of TSPC flip-flops. Its structure is modified to reduce its complexity and to synchronize with the delay-interpolation circuit.

With the dual-modulus frequency divider, fractional-N frequency division can be accomplished by switching the divisor of the dual-modulus divider according to a predetermined schedule.

C. Analog PLL

A traditional analog charge-pump PLL consists of the following four components: voltage-controlled oscillator, phase-frequency detector, and charge pump and loop filter. In the proposed frequency synthesizer, the MSCO acts as the controlled oscillator for both the digital control loop and the analog PLL. We will discuss only the remaining three components in this subsection.

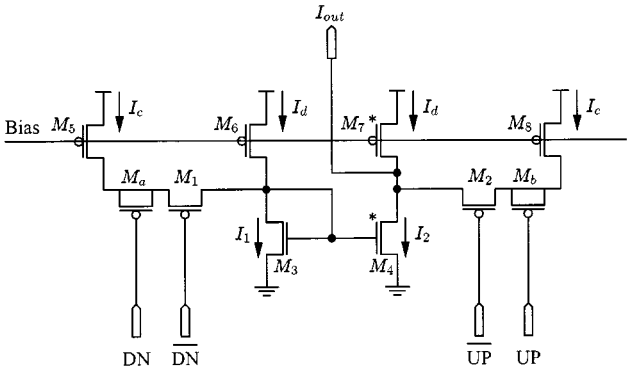


Fig. 10. Circuit diagram of the current-mode charge-pump circuit.

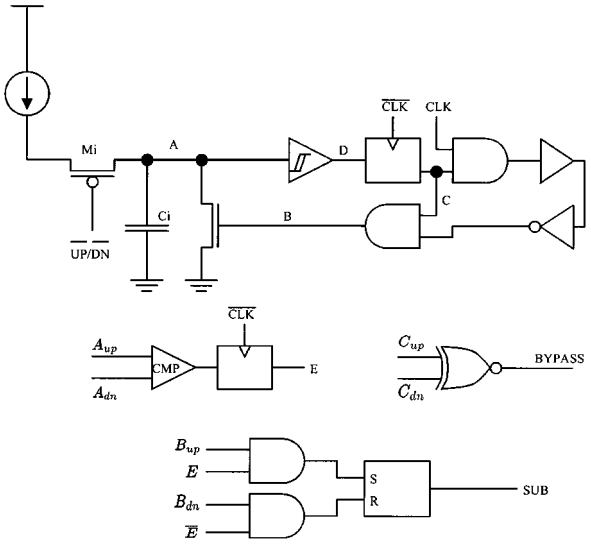


Fig. 11. Circuit diagram of the control signal (*SUB* and *BYPASS*) generator in the digital frequency acquisition controller.

Fig. 9 shows the tri-state phase frequency detector [12] employed in the frequency synthesizer. It consists of two D-type flip-flops and a NOR gate with inputs from the $\overline{Q}$ signals of the two D-type flip-flops. As soon as either of the $\overline{Q}$ signals is low, the NOR gate output resets both flip-flops. Since the *UP* or *DN* signals are generated after $\overline{Q_1}$ or $\overline{Q_2}$ is lowered, the minimum pulsewidth on *UP* and *DN* is only one gate delay, which results in lower jitter, better linearity, and smaller dead zone.

Fig. 10 illustrates the circuit diagram of the charge pump circuit in the proposed frequency synthesizer. When both *UP* and *DN* are low, M_1 and M_2 are turned off and $Iout$ is zero. With *UP* high and *DN* low, then $Iout$ equals $-Ic$. On the contrary, if *UP* is low and *DN* is high, then $Iout$ equals Ic. When both *UP* and *DN* are high, $Iout$ is again zero. In summary, the polarity of the charge-pump output current ($Iout$) depends on the *UP* and *DN* signals and its magnitude is equal to the current Ic.

The MOS devices M_a and M_b are dummy transistors to reduce the effect of clock feed-through. In addition, the MOS devices M_4 and M_7 are implemented using regulate cascode (RGC) technique [13], which can be viewed as a "super" MOS device that provides a very large output resistance without confining the output voltage swing.

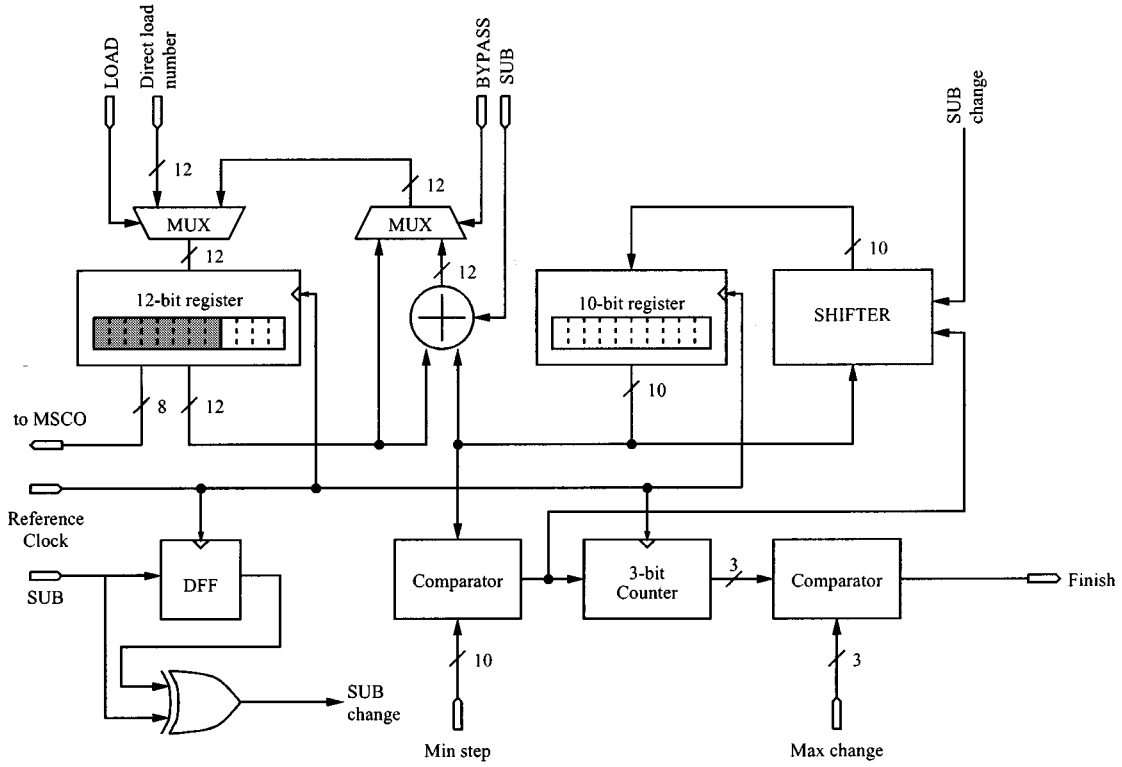


Fig. 12. The digital frequency acquisition circuit.

Another component in the charge-pump PLL is the loop filter. The loop filter used in our design is a second-order RC filter. The natural frequency and the damping characteristic are influenced by the gain of the controlled oscillator and the divisor. Since a digital control scheme is used, the loop filter is designed for best performance when the digital control word of the corresponding frequency has been found.

D. Digital Controller Circuit

Fig. 11 shows the circuit diagram of how the two digital control signals, *SUB* and *BYPASS*, are generated. Basically, two integrators are used to integrate *UP* and *DN* signals from the phase-frequency detector. When node A is high enough, a Schmidt trigger is enabled, thus making node *D* high. A register and some logic are used to produce a discharge signal *B*. After the charge in the capacitor is discharged, the integrating process starts over again.

By comparing the signals *Aup* and *Adn*, node *E* represents the direction that the control word should be adjusted. Two AND gates and na SR-latch are employed to generate the signal *SUB*. Furthermore, the signal *BYPASS* is generated by an XNOR gate.

The circuit diagram of the digital frequency acquisition controller is shown in Fig. 12. The length of the control word register is 12 bit. Only the eight most significant bits are used for the control of the MSCO. The four least significant bits act as a smoothing filter that will remove noises caused by spurious trigger signals. The step size register has a word length of 10 bits, providing a maximum step size as large as one quarter of the control word range. The counter that counts the change of the *SUB* signal is three-bit wide, so the maximum number of sign changes in the *SUB* signal is eight. Furthermore, to provide a direct load capability, a multiplexer is employed to select where the input of the control word register comes from.

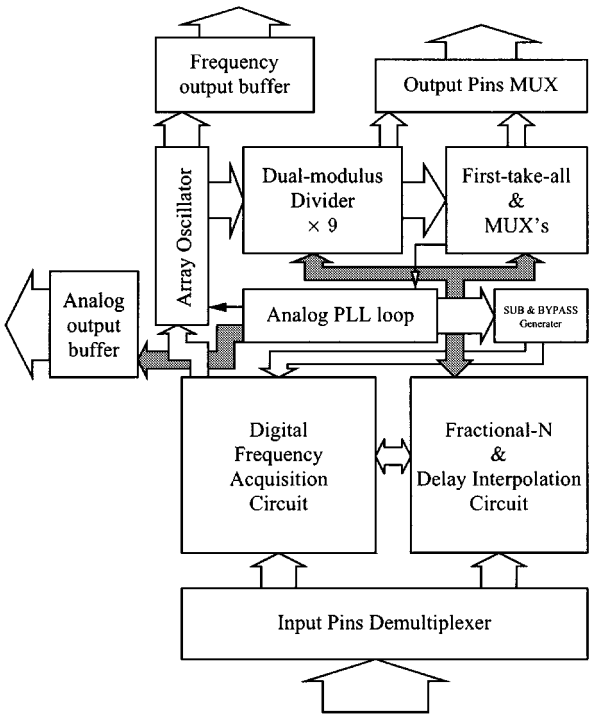


Fig. 13. Floorplan of the proposed frequency synthesizer.

IV. Experimental Results

The proposed mixed-signal controlled PLL frequency synthesizer chip is fabricated using a TSMC 0.6 μm n-well SPTM

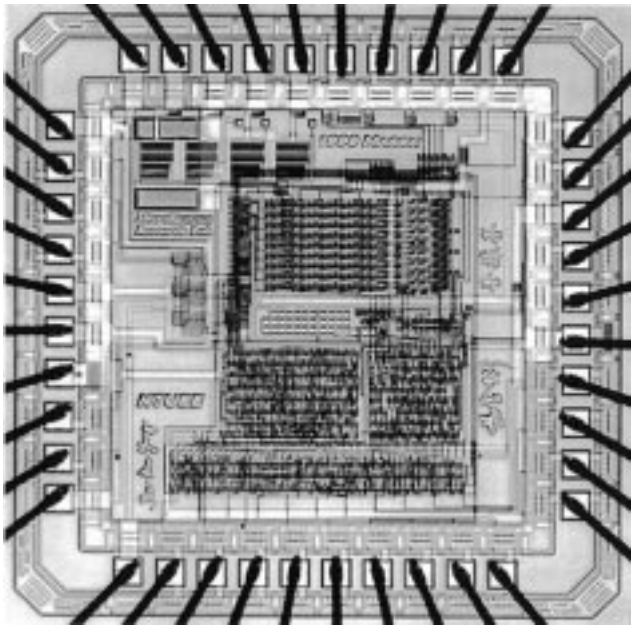


Fig. 14. Photograph of the proposed frequency synthesizer chip.

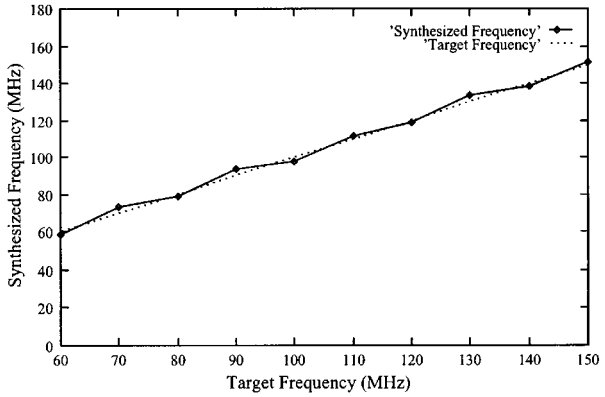


Fig. 15. Measurement results of the output frequency and the target frequency using only the digital loop.

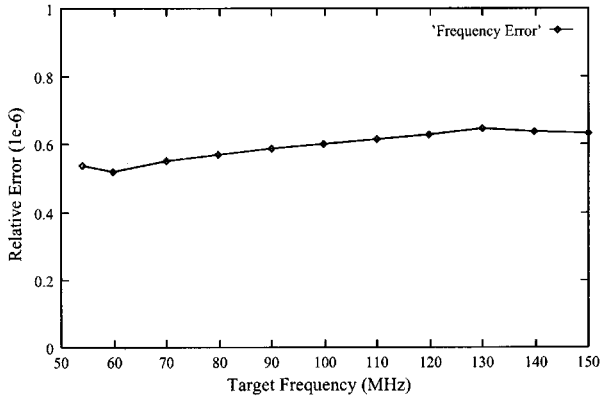


Fig. 16. Measurement results of the frequency error using both the digital and the analog loops.

CMOS process. The floorplan and the photograph of the chip are illustrated in Figs. 13 and 14, respectively.

To test the fabricated frequency synthesizer, we design a circuit board to connect the chip to a personal computer via an

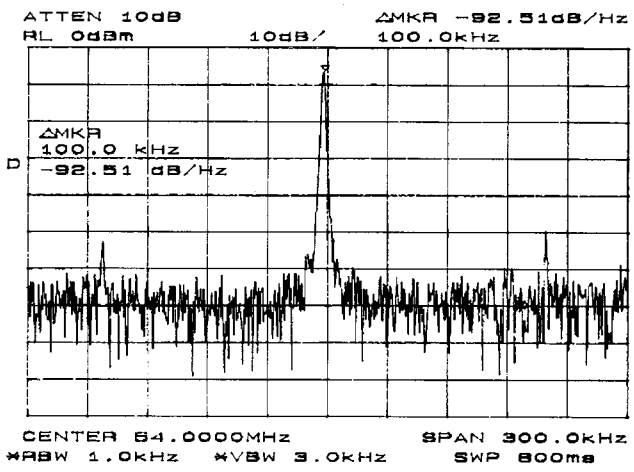


Fig. 17. Measured output spectra.

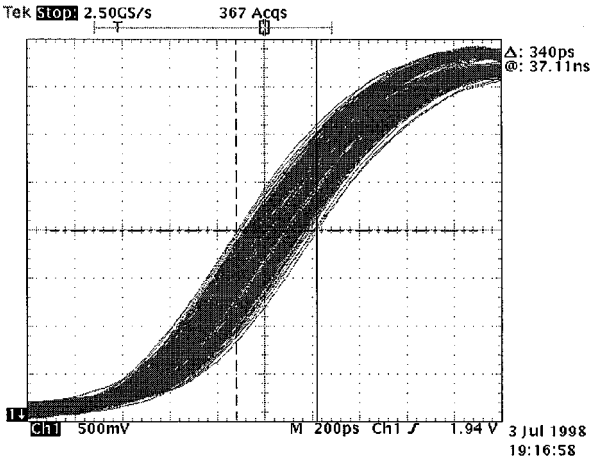
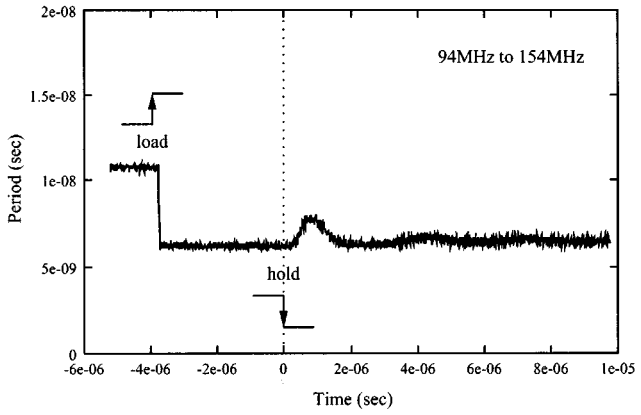


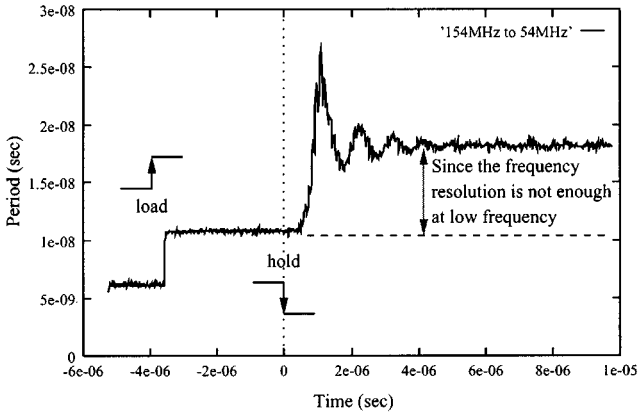
Fig. 18. Measured jitter.

8255 interface card. At first, the supply voltage is set to 2 V and only the digital loop of the frequency synthesizer is enabled. Fig. 15 shows the synthesized frequency and the target frequency with the digital loop in operation. To reduce the frequency error, the analog PLL is further activated. Fig. 16 shows the frequency error between the synthesized frequencies and the target frequency after both digital and analog loops are enabled. The frequency error is less than 1 ppm at all output frequencies. Fig. 17 show the measured spectra of the output frequency at 54 MHz. The phase noise is about −92 dBc/Hz at 100-KHz offset. The measured peak-to-peak jitter is about 340 ps, as shown in Fig. 18 and the rms jitter is about 62 ps.

Since the most important characteristic of the proposed frequency synthesizer is its switching speed, we next measure the performance of the frequency synthesizer chip during channel switching. The measured frequency switching performance is plotted in Fig. 19. Two cases are experimented: frequency switching from a low frequency (94 MHz) to the highest frequency (154 MHz) and frequency switching from 154 to 54 MHz. Since the control variable is a current, which is hard to observe from outside the chip, thus we measure the cycle time (period) distribution of the output oscillation signal. With a change in the divisor, a corresponding digital control word is loaded into the chip on a trigger from the *load* signal. Notice



(a) 94MHz to 154MHz.



(b) 154MHz to 54MHz.

Fig. 19. Measured output waveform period during frequency switching.

TABLE I
SUMMARY OF RESULTS

Technology	0.6 μm SPTM CMOS
Supply Voltage	2-3 V
Working Frequency	54-154 MHz @ 2V
Frequency Switching Time	$< 10\,\mu$s
Frequency Error	< 1 ppm
Jitter	340 ps (P-P); 62 ps (rms)
Phase Noise	-92 dBc/Hz @ 100 KHz ($Fout = 54$ MHz)
Power Consumption	47 mW @ 2V ($Fout = 154$ MHz)
Die Area	2.4×2.4 mm^2

how the cycle time change rapidly as soon as the new digital control word is loaded. At this juncture, the analog PLL is still disabled, so the cycle time of the output oscillation signal still deviates from the target value by a considerable amount. As the *hold* signal is lowered (the analog PLL activated), the whole synthesizer then settles to the new frequency very quickly. The measured switching time is less than 10 μs. Table I lists a summary of the frequency synthesizer chip.

V. CONCLUSION AND DISCUSSION

A 2-V fast-switching mixed-signal-controlled frequency synthesizer which can synthesize 100 frequencies is designed and implemented. In the proposed frequency synthesizer, a digital controlled PLL can acquire the frequency control word of a MSCO in a very short time. Another analog charge-pump PLL performs the phase tracking and frequency fine-tuning. In addition, to improve the acquisition speed and reduce jitter, several techniques are employed. Using a symmetric-load differential delay cell based array oscillator, rejection to power supply noise is enhanced. Using fractional-N frequency divider with a delay interpolation technique, the reference frequency is made higher without inducing noises usually caused by fractional-N frequency dividers. Furthermore, the charge pump performance is enhanced by using the regulate-cascode current mirrors.

The frequency synthesizer was fabricated through a 0.6 μm n-well SPTM CMOS technology. The range of frequency synthesis is from 54 to 154 MHz with 1-MHz spacing and its switching time is less than 10 μs while drawing only 47 mW from a 2-V power supply. Despite our efforts in reducing jitter (delay interpolation, symmetric-load delay cell, and RGC charge pump), the frequency synthesizer still does not perform very well in phase noise (-92 dBc/Hz) and rms jitter (62 ps), though it does excels in the other three important categories. It operates at a very low voltage (2 V) and consumes little power (47 mW at 154 MHz); its frequency switching time is very short (less than 10 μs); its frequency resolution is very high (1 ppm error at 1-MHz channel spacing).

The reason for poor jitter performance has been identified and is mainly due to poor isolation between the ground lines of the analog and the digital circuits in the chip. The contaminated ground line voltage has a peak-to-peak variation of about 500 mV. With the slew rate of the synthesizer output at about 2.5 mV/ps, the noise of the on-chip driver for the synthesizer output alone generates about 200-ps jitter. We believe that with better shielding from the ground/power bounce coupling between the analog and the digital portions of the chip, the frequency synthesizer should be able to generate oscillation signal with much better jitter/phase noise performance. Nevertheless, the proposed fast-switching frequency synthesizer is suitable for FHSS systems, such as WLAN, Bluetooth, and HomeRF, which use FSK modulation that puts less stringent requirement on the phase noise but demands frequency accuracy and fast switching speed. We believe that the proposed mixed-signal control concept and the frequency synthesizer architecture provide a very good foundation for designing future frequency synthesis systems.

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