

行政院國家科學委員會專題研究計畫成果報告

多媒體與多重服務之數位用戶迴路通訊系統 子計畫一 - DMT 傳收機系統架構及類比前端電路設計

System Architecture and AFE Designs of DMT Transceiver

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一、中文摘要

本計畫為三年計畫之第二年度，是發展使用 DMT 調變之數位用戶端迴路傳收機架構及類比前端電路設計技術，包括可調式濾波器與自動增益準位控制子系統。本計劃於第一年度期間，已設計出一基於 DMT 調變的數位用戶端迴路傳收機架構，與其超大型積體電路架構與規格，並且考量低電壓低功率之線路設計。在第二年度中對其類比前端之線路進行設計與模擬，以發展一可調式寬頻濾波器與準位控制系統。

關鍵詞：雙迴路、自動增益控制器、可調頻寬濾波器、超高速率數位使用者迴路、分散式多載波調變

Abstract

This project is for the 2nd of the three-year project that develops DMT-based xDSL transceiver architecture and explores analog front-end circuit design techniques including two key blocks in analog front-end, namely, tunable filter and magnitude control, will be designed. During the first period, the techniques of DSL transmission are studied. The architecture of the DMT-based xDSL transceiver is designed. The issues of VLSI circuit, namely, architecture and specifications, are investigated. Besides, practical circuit design considerations on low voltage and low power are taken into account. In the second period, the transceiver architecture is validated on a

basis of computer simulation in conjunction with theoretical analysis. Moreover, analog front-end circuits are designed and simulated. The issues of bandwidth-tunable filtering and magnitude control are both investigated.

Keywords: Dual-loop, Automatic Gain Control (AGC), Programmable Filter, VDSL, DMT

I. INTRODUCTION

AGC is usually configured as a negative-feedback closed-loop structure with variable gain stage on the signal path and magnitude detection/gain control on the feedback path. The acquisition time of conventional AGC is rather long due to its narrow loop bandwidth. Dual loop architecture can be employed for fast acquisition with small steady state error. The closed-loop magnitude dynamic behavior of a VDSL is much slower than the input signal, which enables the usage of lower frequency digital circuitry and thus lower power consumption. A dual-loop mixed-mode AGC architecture that utilizes analog forward signal path and digital feedback control path is devised.

II. ARCHITECTURE

The AGC as shown in Fig.1 consists of a variable gain amplifier(VGA), a shaping filter, a gain-and-buffer(G/B) and a digital feedback part. The VGA adjusts the gain to maintain the received signals magnitude. The shaping filter refrains from the out-of-band

noise and performs anti-alias filtering for analog-to-digital conversion. The G/B amplifies the signal and provides adequate driving capability of AGC. The feedback path includes a magnitude detector, a subtractor and a dual-loop bandwidth regulator. To extract the received signal amplitude, the output of ADC is rectified, integrated and dumped. Since the integrate-and-dump length is 32, a pre-filter is introduced to reduce the effects of pattern noise and to extract a DC-like control voltage. A dumped value is subtracted from V_{ref} which is employed to setup the desired level. An error voltage is thus generated for the dual-loop filters. A 1-bit quantizer functions as a switch and sets the threshold voltage to determine the loop filter paths. When the quantizer is in the ON state ($Q=1$), the wideband integrator dominates the regulator response. This results in faster convergence though it induces more in-band noise. Gradually, the output signal level approaches the reference voltage V_{ref} and the quantizer turns off ($Q=0$). The regulator bandwidth is immediately shrunk by the first loop filter. This narrow loop bandwidth provides a better noise rejection. The AGC possesses a wide loop bandwidth for fast tracking in the initial acquisition and a narrow loop bandwidth for good jitter performance during steady state, which mainly employs a digital loop regulator arranged in feedback magnitude control.

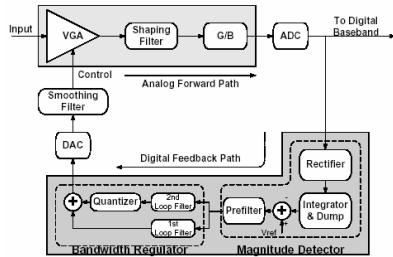


Figure 1. Block diagram of the dual-loop mixed-mode AGC

III. CIRCUIT DESIGN

A. VGA

Exponential VGA is required for a stable AGC loop bandwidth. CMOS transistor does not possess an exponential characteristic as a BJT does. Hence, pseudo

exponential approximation transfer curve can be used. Fig.2 shows the circuit with the property of pseudo exponential.

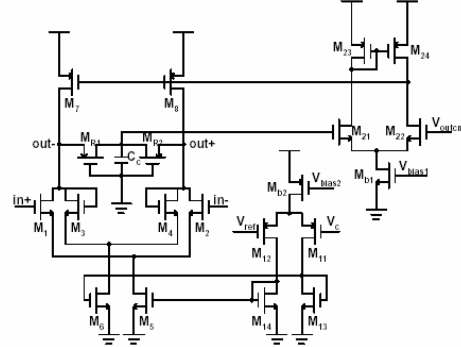


Figure 2. The pseudo-exponential VGA circuit

In the circuit schematic, the CMOS VGA consists of three parts, namely a gain cell, gain control and common mode feedback. The gain cell is composed of an input source-coupled pair (SCP) M_1 - M_2 and a pair of diode connected loads M_3 - M_4 whose bias currents are controlled by the current mirrors, M_5 - M_{14} and M_6 - M_{13} , respectively. Different control voltages applying to the SCP M_{11} - M_{12} change the transconductances of M_1 , M_2 , M_3 and M_4 .

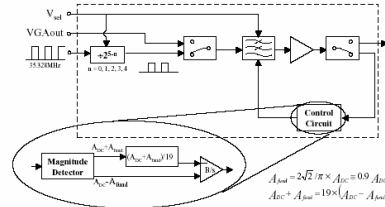


Figure 3. Filter and tuning circuit block

B. LPF

Fig.3 shows the complete block diagram of the filter and the tuning circuit. This filter incorporates the automatic gain-controlled amplifier (AGC) to accomplish the analog front end in the receiver chain. In order to conform the DMT VDSL system, the filter is configured as a 4-th order Chebyshev low-pass filter with 0.5dB ripple in the passband. The passband corner frequency is programmable to be 1.104×2^n MHz, where n is controlled by the V_{sel} signal. The filter is followed by an output buffer stage to drive the succeeding circuits in AGC. The switching circuits select the input signal of

the filter from the variable gain amplifier (VGA) in the previous stage and its output signal to ADC for digitization during general operational mode.

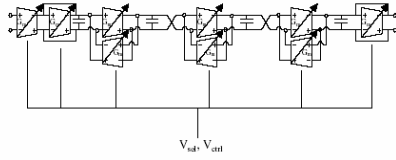


Figure 4. 4th order gyrator-c low-pass-filter

For high frequency operation and insensibility to process variation, a Gm-C circuit based on LC ladder prototype, as shown in Fig.4, is used to synthesize the filter. Each transconductor in this filter is designed to be programmed by the V_{sel} signal as indicated in the figure. The transconductance of G_{m_i} ranges from g_{mui} to $16g_{mui}$, where g_{mui} is the unit transconductance value. Fig.5 shows the transconductor schematic for the Gm-C filter. The input stage contains M_1 and M_2 that convert the voltage signal into current signal. The V_{sel} signal controls the transmission gate which turns on/off the bias current provided by M_{b1} to M_{b8} to select one of the five G_m values in each transconductor stage. A dummy input pair by M_3 and M_4 is added to compensate the parasitic capacitance at the input. V_{ctrl} is generated from the tuning circuits and used to fine tune the G_m value through the degeneration transistor M_{d1} such that the filter bandwidth can be set to the predefined value. To increase the output impedance without sacrificing power dissipation, the negative resistance load (NRL) by M_5 - M_8 is used.

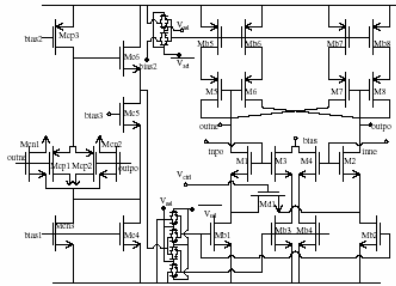


Figure 5. Gm cell using NRL (Negative Resistance Load)

A complementary common mode feedback (CMFB) is configured for

low-voltage operation. An n-type source-coupled pair (n-SCP) by M_{cn1} and M_{cn2} and a p-type SCP (p-SCP) by M_{cp1} and M_{cp2} are utilized as the input stage similar to conventional rail-to-rail amplifiers. The CMFB voltage is extracted by the n-SCP with a common gate amplifier and the p-SCP with a source follower and fed back to the tail currents for the core cell. The two pairs, n-SCP and p-SCP, compensate the nonlinearities of each other and increase the output swing of the Gm cell.

C. Gain/Buffer

The G/B stage is employed to amplify the signal and drive the output pads. Fig.6 depicts the circuit schematic of the G/B. It is composed of three parts, a transconductance stage, a current gain stage and a transimpedance stage. Input stage M_1 transforms the input voltage into current. Then, the current gain stages M_2 - M_4 and M_3 - M_5 utilize current mirror structure twice to offer current gains. Finally, transistors M_7 , M_8 and resistor R_f construct a shunt-shunt feedback transimpedance stage. Essentially there are no high impedance nodes internally.

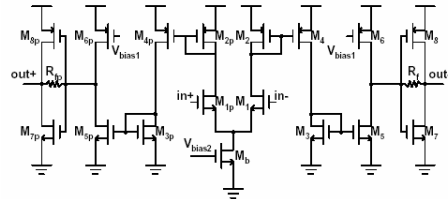


Figure 6. The wideband gain-and-buffer circuit

D. Digital Feedback Path

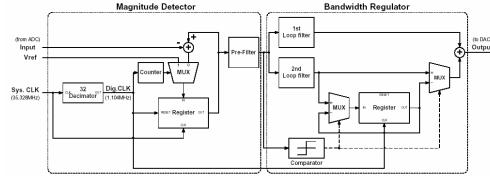


Figure 7. The circuit of the digital feedback control path

As shown in Fig.7, the magnitude detector and the bandwidth regulator constitute the digital feedback path. To reduce power consumption, a lower system clock that is generated by dividing the sampling clock of a factor 32. The magnitude

detector is composed of a MUX, a register and an adder. The reference voltage V_{ref} is firstly loaded into the register in each integrate-and-dump cycle while the 5-bit counter is 0. The stored value is then subtracted from the rectified ADC output and updated by the residual value iteratively until the integrate-and-dump cycle is finished.

In the acquisition process, the output of the bandwidth regulator is the summation of the first loop filter and the second loop filter. Meanwhile, the register keeps updated. When the pre-filter exceeds the threshold voltage, both of the MUXs are switched to the lower signal path by the output of the comparator. The latest value hold in the register is summed with the always-on 1st loop filter output. A steady state control voltage is then sent to VGA. The coefficients of the dividers and multipliers are power of two, i.e. 2^n or $1-2^{-n}$, which are just modified to perform shift-and-add technique.

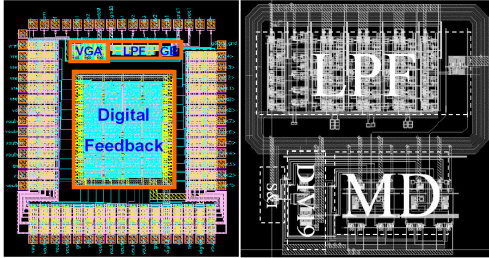


Figure 8. Chip Layouts of AGC and Programmable Filter

IV. IMPLEMENTATION AND SIMULATION RESULTS

Technology	TSMC 0.35 μ m CMOS 1P4M
Supply voltage	2V
Filter type	4-th Order Chebyshev LPF with $\delta_p = 0.5dB$
Cut-off frequency	1.014×2^n MHz with $n=0, 1, 2, 3, 4$
Total harmonic distortion	$< -55dB$ at $150mV_{pp}$ input
Power consumption	Filter: 2.8mW Output buffer: 19.2mW Tuning circuit: 6mW

Table 1. Programmable filter performance summary

The AGC and programmable filter are fabricated with 0.35 μ m 1P4M CMOS technology. Chip layouts are shown in Fig.8. The programmable filter and AGC performance summaries are shown in Table.1 and Table.2, respectively. Fig.9 shows the

AGC closed-loop simulation result.

Technology	TSMC 0.35 μ m CMOS 1P4M
Input Signal Range	26dB(20mV _{pp} ~ 400mV _{pp})
Passband Frequency	0MHz ~ 14MHz
Passband Ripple	$< 0.8dB$
Acquisition Time @0.1%	$< 0.5ms$
THD@ $V_i = 400mV_{pp}$	$< -44dB$ (with 5 harmonics in band)
Output Level	1V _{pp}
Die Size	1.9 \times 2.1 (mm ²)
Supply Voltage	Analog : 2V Digital : 3.3V
Power Consumption	Analog : 36mW Digital : 11mW

Table 2. AGC performance summary

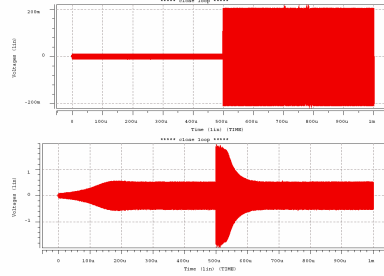


Figure 9. AGC closed-loop simulation

V. CONCLUSION

The dual-loop mixed-mode AGC for VDSL up/down stream AFE is presented in this report. With the aid of the digital bandwidth regulator, it provides two distinct loop-bandwidth responses, namely, 12KHz and 5.6KHz, to achieve a fast convergence during acquisition and stable and precise magnitude control at the steady state. The settling time is less than 0.5ms for 26dB dynamic input while the output maintains 1Vpp constant level.

VI. REFERENCES

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