Hole mobility enhancement of $Si_{0.2}Ge_{0.8}$ quantum well channel on Si

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The ultrathin strained $Si_{0.2}Ge_{0.8}$ quantum well channel (~5 nm) directly grown on Si substrates is demonstrated with low defect density and high hole mobility. The quantum well $Si_{0.2}Ge_{0.8}$ channel reveals an ~3.2 times hole current enhancement and an ~3 times hole mobility enhancement as compared with the bulk Si channel. The output current-voltage characteristics under the external mechanical strain confirm the compressive strain in the channel. The external compressive strain further enhances the hole mobility in a $Si_{0.2}Ge_{0.8}$ channel. © *2007 American Institute of Physics*. [DOI: 10.1063/1.2400394]

The superior transport property of Ge has high electron and hole mobilities and can reach the high performance target in the future Si technology. However, the cost and insufficient abundance of Ge in the Earth make it difficult to replace Si. The dual channel (strained Si and strained Ge)[1] and the Ge channel[2] on relaxed SiGe buffer structures have significant mobility enhancements but suffer the disadvantages of threading dislocation defect, rough surface, and high cost of SiGe virtual substrate. The ultrathin SiGe epitaxially grown directly on Si with compressive strain has the advantages of high mobility, low cost, and the compatibility with Si process. In the previous work, the hole mobility enhancements of ten times,[1] six times,[2] two times,[3] and three times[4] have been reported, and all are based on thick Ge layers (~400 nm) or SiGe buffers (1–2 μm). In this letter, we investigate the ultrathin SiGe channel of a *p*-channel field effect transistor (PFET) with the Schottky barrier source and drain.

The epi-Ge layer (~5 nm) was grown on a Si (100) substrate at 525 °C by ultrahigh-vacuum chemical vapor deposition. However, the fast diffusion of Si into Ge (Ref. 5) forms the $Si_{0.2}Ge_{0.8}$ layer at the final stage of the growth. To improve the interface between the gate insulator and the $Si_{0.2}Ge_{0.8}$/Si channel, a nominal ~3 nm Si cap layer is grown on the top of epi-Ge layer to passivate and smoothen the surface. Due to the slow diffusion of Ge into Si, the cap composition is dominated by Si. The roughnesses of nominal 3 and 1 nm Si caps on the $Si_{0.2}Ge_{0.8}$ channel are 0.5 and 0.62 nm, respectively, measured by atomic force microscope on the area of 10×10 μm^2. Tacking the process into consideration, the thin cap (1 nm) was completely oxidized due to the exposure to the air in the fabrication, and the inferior Ge oxide existed at oxide/$Si_{0.2}Ge_{0.8}$ interface with a large interface density of 1.5×10^{12} cm^{-2} eV^{-1} as compared to 2×10^{11} cm^{-2} eV^{-1} for an initial 3 nm cap. The Si cap in our device is a sacrificial and passivation layer for the SiGe channel, and its thickness is reduced after the device fabrication. However, if the Si cap can be maintained after the process, the thinner remaining Si cap can have a higher channel mobility.[6] As a result, the nominal ~3 nm Si cap layer is essential for our device and approximately 1 nm Si cap layer remains after processing. The gate stack consists of ~300 nm tetra-ethyl-oxy-silane (TEOS) gate dielectric and a polygate with P implantation activated by rapid thermal an-

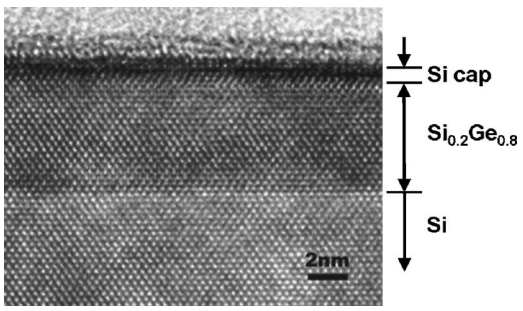

FIG. 1. TEM image of a $Si_{0.2}Ge_{0.8}$ quantum well on Si with a nominal ~3 nm Si cap layer. Due to consumption of the Si cap in the process, only an ~1 nm cap layer was observed by TEM.

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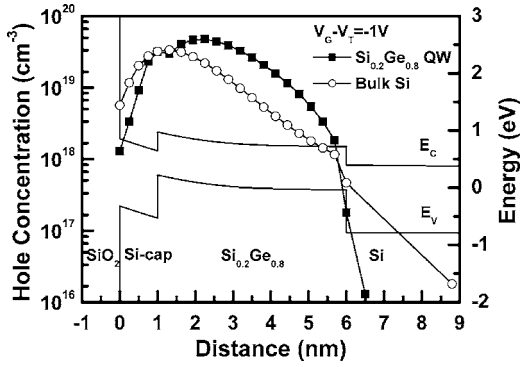

FIG. 2. Hole concentration for the $Si_{0.2}Ge_{0.8}$ quantum well device and the bulk Si device by quantum mechanical simulation. The hole concentration of the $Si_{0.2}Ge_{0.8}$ quantum well device is higher than that of bulk Si device due to the hole confinement in the $Si_{0.2}Ge_{0.8}$ quantum well channel.

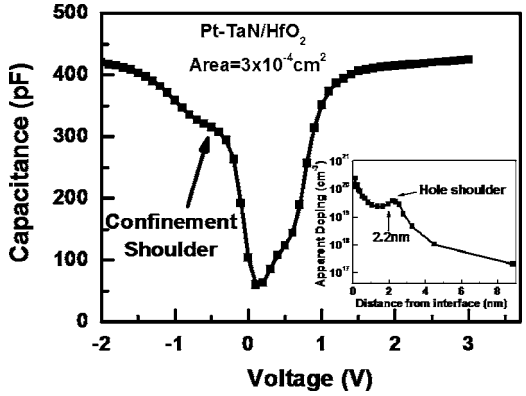

FIG. 3. *C-V* characteristics of $Si_{0.2}Ge_{0.8}$ quantum well metal-oxide-semiconductor capacitor on a *n*-type Si substrate with a Pt/TaN metal gate and a 5 nm HfO_2 insulator. The confinement shoulder in the *C-V* plot indicates the hole confinement in the $Si_{0.2}Ge_{0.8}$ quantum well.

nealing (650 °C, 10 s). The one-mask process was used to fabricate PFET,[7] and Pt was used as the Schottky barrier source and drain.[8]

The transmission electron microscope image of the $Si_{0.2}Ge_{0.8}$ layer with a nominal ~3 nm Si cap layer is shown in Fig. 1. Due to the consumption of the Si cap in the process, only an ~1 nm cap layer was observed. It shows no apparent defect or dislocation in the image. The 5 nm SiGe layer is too thin for the regular x-ray diffraction (XRD). The high intensity source was available in the synchrotron radiation and was used to probe the lateral lattice constant using the H scan (in-plane XRD). The 5 nm SiGe layer revealed the same lateral lattice constant as the Si substrate, and the Ge concentration estimated by Raman shift is about 80%. Figure 2 shows that the hole concentration of a $Si_{0.2}Ge_{0.8}$ quantum well at inversion bias is mainly located in the $Si_{0.2}Ge_{0.8}$ quantum well by the simulation with a 1 nm Si cap and a 5 nm $Si_{0.2}Ge_{0.8}$ well. The ~5 nm $Si_{0.2}Ge_{0.8}$ layer is sufficient for the hole conduction channel.

The 5 nm HfO_2 are deposited on the $Si/Si_{0.2}Ge_{0.8}/Si$ quantum well to measure the capacitance-voltage (*C-V*) characteristics. The results show that the equivalent oxide thickness is 2.5 nm and the leakage current is 7.3×10^{-5} A/cm^2 at 1 V. Figure 3 shows a shoulder on the *C-V* curve measured at 100 Hz, indicating the hole confinement in the $Si_{0.2}Ge_{0.8}$ quantum well. The existence of this shoulder at different measurement temperatures (−100–30 °C) suggests that it should not be originated from defects.[9] To observe the confinement shoulder in the *C-V* curve, the dielectric thickness should be comparable to the $Si_{0.2}Ge_{0.8}$ thickness, thus the thin HfO_2 is used. The centroid of hole concentration (inset of Fig. 3) extracted from the *C-V* plot[10] is 2.2 nm from the surface, which is consistent with the simulation result (Fig. 2).

The transfer characteristics measured at the drain bias=−0.1 V for a $Si_{0.2}Ge_{0.8}$ quantum well device and a control Si device are shown in Fig. 4(a). The I_{on}/I_{off} ratio is 4×10^6 for the $Si_{0.2}Ge_{0.8}$ device. The leakage current dominated by electron is still larger than that of the bulk Si device due to the lower barrier height (ϕ_{B_n}=0.78 eV) for electron injection in the off state than bulk Si device (ϕ_{B_n}=0.85 eV). The $Si_{0.2}Ge_{0.8}$ PFET shows an ~3.2 times drain current enhancement in the saturation region [Fig. 4(a)]. Due to the thick TEOS gate oxide needed for the one-mask process, the estimated ideal V_T for the control Si device is −5.4 V. The deviation between the ideal V_T and the experimental value (−8.3 V) may come from the fixed oxide charges and the interface trapped charges. The $Si_{0.2}Ge_{0.8}$ PFET has a relatively smaller magnitude of V_T (−7.4 V) than that of the control Si device (−8.3 V) due to the hole confinement in the SiGe quantum well. Figure 4(b) shows the hole mobility measured by the split *C-V* technique. The approximately

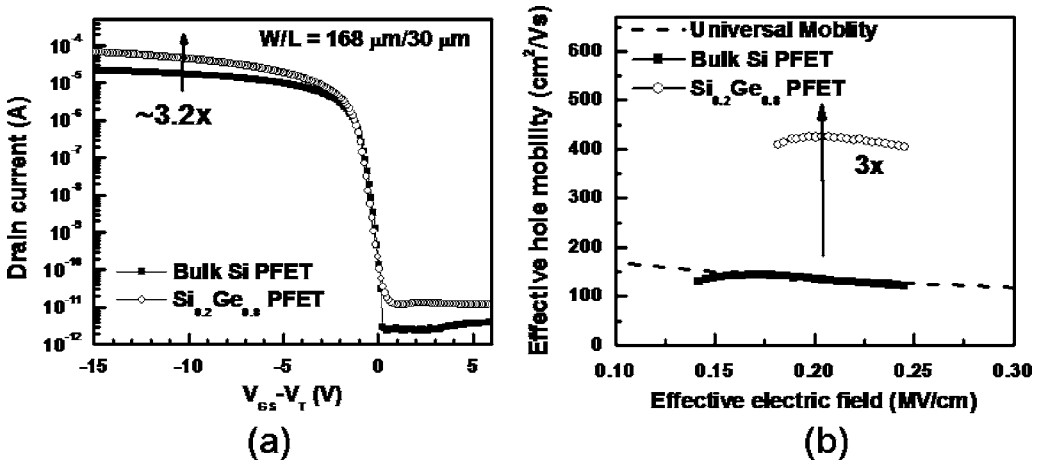

FIG. 4. Drain current characteristics of a $Si_{0.2}Ge_{0.8}$ quantum well device and a bulk Si device. (b) The hole mobility of a $Si_{0.2}Ge_{0.8}$ quantum well device and a bulk Si device from the split *C-V* measurement.

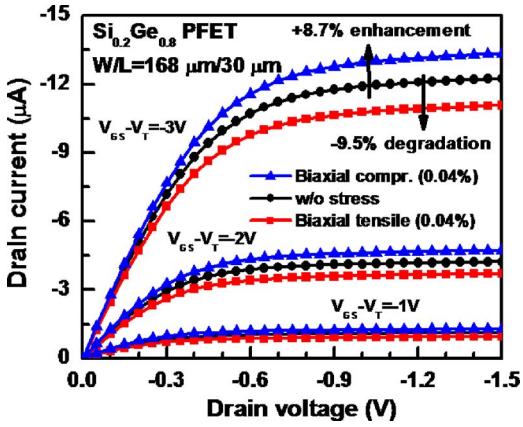

FIG. 5. Output characteristics of a $Si_{0.2}Ge_{0.8}$ quantum well PFET under external biaxial tensile/compressive mechanical strain.

three times hole mobility enhancement for the $Si_{0.2}Ge_{0.8}$ PFET is obtained as compared with the bulk Si device.

The $Si_{0.2}Ge_{0.8}$ device under external mechanical strain was examined (Fig. 5).[11] For the control Si device, the saturation current has relatively smaller alterations (−2.4% and 0.8% under the 0.04% biaxial tensile and compressive strains, respectively) than $Si_{0.2}Ge_{0.8}$ device. Both the compressive and tensile strains can enhance the relaxed Ge hole mobility.[12] The Ge riched $Si_{0.2}Ge_{0.8}$ is believed to have a similar trend. For our $Si_{0.2}Ge_{0.8}$ quantum well PFET, however, the drive current is enhanced with the biaxial compressive strain and degraded with the biaxial tensile strain. The scenario may be resulted from the built-in compressive strain in the $Si_{0.2}Ge_{0.8}$ quantum well. Thus, the addition of the external compressive strain and the built-in compressive strain in the $Si_{0.2}Ge_{0.8}$ layer will enhance the saturation current. The biaxial tensile strain, however, degrades the on current, due to the compensation of built-in compressive strain of the $Si_{0.2}Ge_{0.8}$ quantum well by the external tensile strain.

In conclusion, the high-Ge-concentration epichannel directly on Si is a promising low-cost solution for the future Si technology nodes, beside the bulk Ge and the SiGe graded buffer technologies.

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