

A Dual-band IEEE 802.11a/b/g Receiver Front-end Using Half-IF and Dual-Conversion

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Abstract—This paper presents a dual-band receiver front-end architecture which combines the dual-conversion [4] and half-IF techniques for IEEE 802.11a/b/g. The proposed architecture receives dual-band signal with single receiver chain to reduce components count such as the 2nd down-conversion mixer and VCO. The required LO frequencies of the dual-band application can be synthesized by only one VCO in combination with a divide-by-four circuit. An LC tank aided mechanism of mixer is also proposed to deal with the flicker noise. The core portion of the front-end receiver has been fabricated in 1P6M 0.18 μ m CMOS technology. The delivered gain, noise figure, and IIP3 are 20 dB, 3.5 dB, and -13 dBm, respectively simulated. The chip occupies an area of 1.21 \times 1.46mm² and the power consumption is 24mW under the supply voltage of 1.8V.

Index Terms—Dual-band, dual-conversion, flicker noise, half-IF, LNA, mixer, WLAN.

I. INTRODUCTION

In the market of wireless local area network (WLAN), multi-standard transceivers have been the trend. The IEEE 802.11b standard at the 2.4 GHz ISM band provides data rates up to 11 Mbits/s [2]. The 802.11a standard at the 5GHz U-NII bands provides data rates up to 54 Mbits/s using OFDM modulation [1]. Released in 2003, the 802.11g standard, operated at the same band of 802.11b, uses the modulation method of 802.11a and provides data rates up to 54 Mbits/s [3]. Many products in the market can support each of the standards simultaneously, and the employed transceiver architectures are usually the direct-conversion ones.

As for the published dual-band architectures, most of them receive the two-band signal by two signal paths and the direct-conversion architecture is mostly adopted, too [5-7]. In this paper, a new architecture is proposed that can receive signal at two-band, 5.8GHz and 2.4GHz, with the same receiver chain. Due to the elaborate frequency conversion planning, the troublesome image problem is relaxed in this design. The organization of this paper is as follows. The receiver architecture is described in Section II. In Section III, the circuit topologies meeting the requirements of this architecture are presented. Finally, the simulation results and conclusions are given in Section IV and V, respectively.

II. RECEIVER ARCHITECTURE

The proposed receiver front-end architecture is shown in Fig. 1. The components inside the dashed frame can be implemented into a single chip, and those outside the frame are the lumped components, which are switch, diplexer, and band-select band-pass filters. Two band-pass filters instead of one are used in order to provide sufficient rejection of the out-of-band interferences for each band. When the desired signal is at 5.8 GHz, the frequency conversion method, shown in Fig. 2., is used [4]. The 3.465GHz image is 2 GHz far away from the desired signal, and it can be filtered out by the band-pass nature of the on-chip amplifiers. The first local oscillator (LO) frequency, which is 4.62 GHz, is four times of the second LO, and thus they can be synthesized by a single voltage controlled oscillator (VCO) and a divide-by-four circuit. Because the VCO frequency is different from the signal frequency, the LO pulling problem will not occur.

This dual-band receiver architecture can also be switched to half-IF conversion to receive 2.4GHz RF signal, as shown in Fig. 3. The utilized 1.2 GHz LO frequency can be obtained by the same circuits composed of one VCO with 4.8-5 GHz tuning frequency and a divide-by-four circuit. As shown in Table I, the VCO frequency range of the two bands is close, so a VCO with wide tuning range can deliver the required LO frequencies for dual-band application. At the same time, the 90^o phase shifter can be eliminated due to the utilization of dividers. Another benefit of this dual-band receiver is that the IF frequencies are close for this dual-band signal, so there is an ease to implement the circuits after the first down-conversion. As for the image signal around the zero frequency, the attenuation contributed by amplifiers and lumped components such as antenna and band-select filter is very large, and thus the image rejection ratio can be as high as 60dB [8]. Two problems that should be taken into account are the upconversion of flicker noise to IF frequency and the DC-offset that comes from LO-to-IF feedthrough. The circuits proposed in the next section will deal with the first problem. For the DC-offset problem, a high-pass filtering offset-cancellation circuit can solve it [8]. The SNR degradation due to the filtering is not significant because for IEEE 802.11a/g, the OFDM modulation leaves the center sub-carrier empty, and for IEEE 802.11b, spread-spectrum modulation is used.

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III. CIRCUIT TOPOLOGIES

The only RF circuits that need to be carefully designed for our receiver architecture are the LNA and the first mixer. The design of other components is the same as the single band ones. For example, the VCO required is just a wide-tuning-range one. Besides, the second mixer and the amplifiers at baseband have single-band nature because the IF bandwidth is not very wide, which has been shown in the last section.

The LNA schematic is shown in Fig. 4. Because the LNA is designed to have the ability to receive and amplify the two-band signal, it has a load that contains two inductors and two capacitors [9]. The function of this LC tank can be comprehended as follows. When the frequency is low, the L and C in series are capacitive in effect. When the frequency is high, they are inductive in effect. Thus, the LC tank has two peaks in the frequency domain. The input matching of the LNA is achieved by off-chip microstrip lines, which are combinations of some open-stubs on the PCB board.

The mixer schematic is shown in Fig. 5. It is a gilbert-cell type mixer with source degeneration resistors to enhance the linearity. The mixer is a wide-band device in nature, so signal can drive the input ports and LO ports directly. Also, because signal frequency at the output of the mixer is about 1 GHz for both the two-band operation, the output port is single-band in nature and thus only one inductor is used, instead of the two-inductor case in LNA.

The mixer in [8] prevents the up-conversion of flicker noise of the transconductance stage to IF, but ignores the flicker noise of the switching pairs. The mixer proposed here uses an LC tank to achieve the filtering function. The resonant frequency of the LC tank is at the signal frequency such that it blocks the signal from passing through it. As for the flicker noise around zero frequency, it sees a short because the LC tank has an inductor in parallel. The circuit can thus be reduced to the half circuit as shown in Fig. 6. The topology of mixer is destroyed, and the flicker noise in neither the transconductance stage nor the switching stage will be up-converted to IF.

The linearity of amplifiers is an important consideration for wireless communication. When the signal received by the antenna is not very large, the third-order intermodulation signal located at the signal frequency band because of the adjacent-channel interferences and the non-linearity of amplifiers must be low enough in order not to degrade the SNR. For WLAN, the IIP3 of the receiver chain should be at least -26dBm to meet this requirement. Meanwhile, when the input signal is large, which is at most -30dBm , -10dBm , and -20dBm for IEEE 802.11-a/b/g respectively, the amplifiers may be saturated. Moreover, for IEEE 802.11a/g that have 52 subcarriers, another add-on power back off of 10dB is needed to accommodate the large peak-to-average ratio (PAR). Thus, a gain-adjusting mechanism is necessary for the front-end amplifiers. A variable resistor can be placed in parallel with the load inductor, and in this case it is replaced by a

digitally switched PMOS, as shown in Fig. 7. Discrete gain steps can also be achieved by many of such PMOS placed together.

IV. SIMULATION RESULTS

The input return loss of the LNA is shown in Fig. 8., in which two bands matching is achieved, with bandwidth larger than 200 MHz in ISM band and larger than 300 MHz in the upper U-NII band. The S21 of LNA is shown in Fig. 9. The gain at each band is about 10 dB. The image rejection ratio (IRR) provided by this amplifier is larger than 60 dB for upper U-NII band, and 30 dB for ISM band. The noise figure of the LNA and mixer operated at 2.4 GHz when no LC tank is inserted in the LO switching pair is shown in Fig. 10. The up-converted flicker noise has a significant influence on the noise figure. After the LC tank is inserted, the influence from the flicker noise vanishes, as shown in Fig. 11.

Table II is the summary of the simulation results of the LNA and mixer. From the comparison between the two circuits with and without LC tanks to block the up converting of flicker noise, it can be observed that the noise figures for both bands improve. However, the conversion gain and IIP3 is not the case. This is because that the gain depends on the quality factor of the LC tanks and the linearity depends on the harmonic termination [10], which is not the same for the two bands.

The power consumption of the core circuit is 24mW. It has been fabricated by TSMC 1P6M 0.18 μm CMOS. The chip area is 1.21 \times 1.46 mm² and its microphotograph is shown in Fig. 12.

IV. CONCLUSION

A dual-band receiver front-end architecture is proposed in this paper. It combines the advantage of dual-conversion and half-IF receivers to provide IRR of 60dB and 30dB for U-NII and ISM band signal respectively. The IF frequency range of 1.14 to 1.24GHz relax the component requirement after the first downconversion. The dual-band LNA and mixer have been designed to deliver a conversion gain of 20dB and IIP3 of -14dBm with a power consumption of 24mW. The troublesome flicker noise problem in half-IF conversion has been solved by a circuit topology proposed in this paper.

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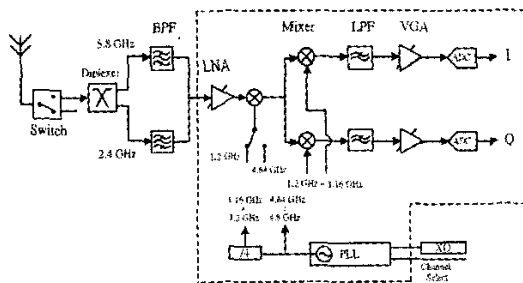


Fig. 1. Block diagram of the receiver.

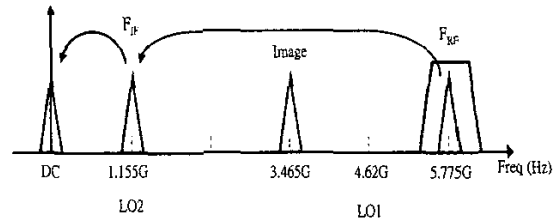


Fig. 2. Frequency planning of 5 GHz signal.

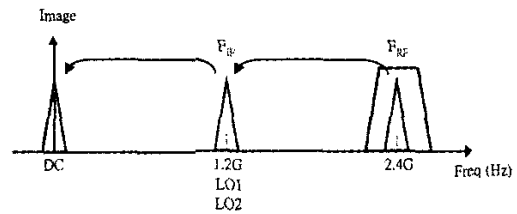


Fig. 3. Frequency planning of 2.4 GHz signal.

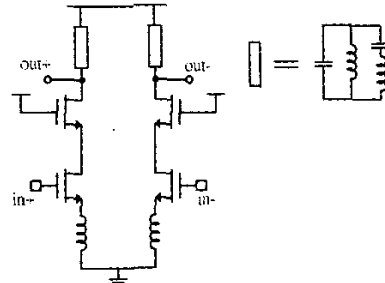


Fig. 4. Schematic of the LNA.

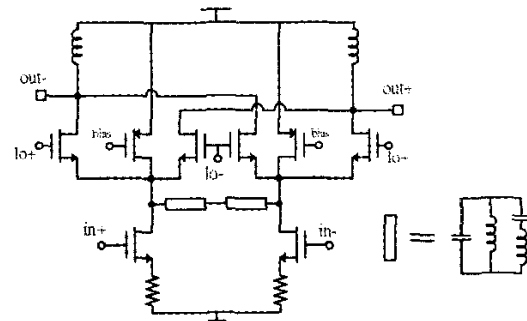


Fig. 5. Schematic of the first mixer.

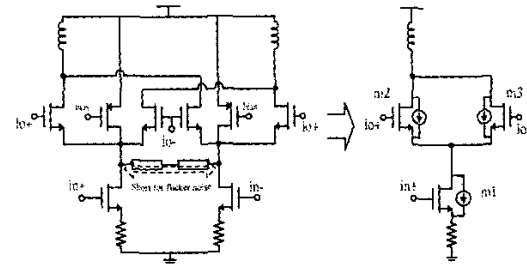


Fig. 6. Filtering mechanism for flicker noise.

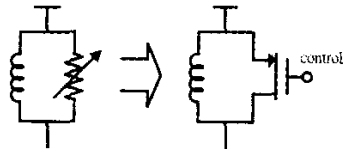


Fig. 7. Gain-adjusting circuit.

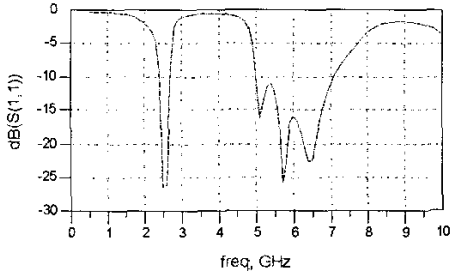


Fig. 8. Input return loss of the LNA.

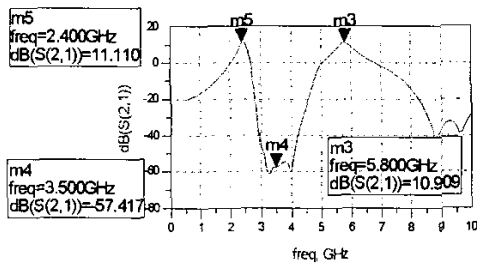


Fig. 9. S21 of the LNA.

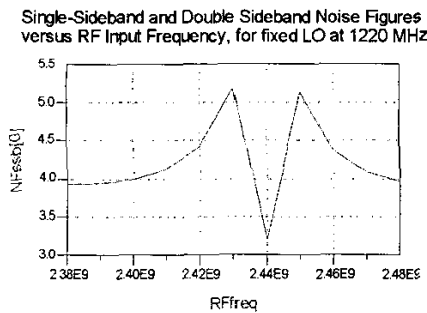


Fig. 10. Noise figure at the 2.4 GHz band, without LC tank inserted.

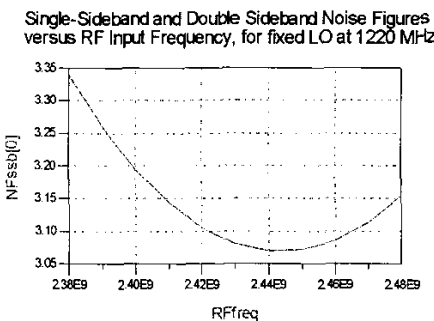


Fig. 11. Noise figure at the 2.4 GHz band, with LC tank inserted.

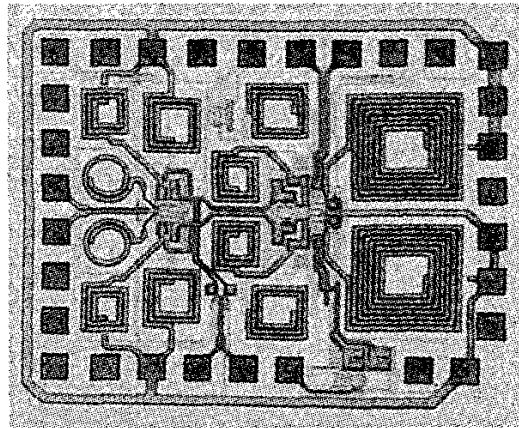


Fig. 12. Chip photograph.

TABLE I
FREQUENCY RANGE OF EACH STAGE

Frequency Band	Frequency Range	VCO Range	IF Range
Upper U-NII Band (GHz)	5.725-5.825	4.58-4.66	1.145-1.165
ISM (GHz)	2.40-2.4835	4.8-4.967	1.2-1.242

TABLE II
SIMULATED LNA AND MIXER PERFORMANCE.

Parameters		LNA+Mixer without flicker noise filtering circuitry	LNA+Mixer with flicker noise filtering circuitry
Supply Voltage		1.8 V	1.8 V
Power Consumption (without biasing and output driver circuits)		24 mW	24 mW
2.4 GHz	Gain	21.3 dB	20 dB
	NF	>4.5 dB	3.1 dB
	IIP3	-16.5 dBm	-13.4 dBm
	LO Power	-2 dBm	-2 dBm
5.8 GHz	Gain	16.4 dB	18.8 dB
	NF	4.25 dB	3.55 dB
	IIP3	-8.8 dBm	-11.4 dBm
	LO Power	-2 dBm	-2 dBm
Technology		TSMC 1P6M 0.18μm CMOS	
Chip Area		1.21×1.46 mm ²	