K-Band HBT and HEMT Monolithic Active Phase Shifters Using Vector Sum Method

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***Abstract*—Two monolithic 3-bit active phase shifters using the vector sum method to K-band frequencies are reported in this paper. They are separately implemented using commercial 6-in GaAs HBT and high electron-mobility transistor (HEMT) monolithic-microwave integrated-circuit (MMIC) foundry processes. The MMIC HBT active phase shifter demonstrates an average gain of 8.87 dB and a maximum phase error of 11° at 18 GHz, while the HEMT phase shifter has 3.85-dB average measured gain with 11° maximum phase error at 20 GHz. The 20-GHz operation frequency of this HEMT MMIC is the highest among all the reported active phase shifters. The analysis for gain deviation and phase error of the active phase shifter using the vector sum method due to the individual variable gain amplifiers is also presented. The theoretical analysis can predict the measured minimum root-mean-square phase error 4.7° within 1° accuracy.**

***Index Terms*—Active phase shifter, HBT, high electron-mobility transistor (HEMT), K-band, monolithic microwave integrated circuit (MMIC), vector sum method.**

I. Introduction

In MODERN communication systems, e.g., an electronically array system, the phase shifter is the key component to provide differential phase shifter to scan an angle of broad band [1]. Active phase shifters [2]–[6] using the vector sum method can provide a phase-shifting function with signal gain rather than loss as for the passive ones. There are several architectures to implement the vector sum method for active phase shifters. Conventional approaches [2]–[5] involve several 90° and 180°couplers, thus resulting in large circuit sizes. Recently, the circuit reported in [6] demonstrated a small circuit size since it simply utilized one 90° coupler and one 180° delay line.

The block diagram of the recent reported 2-GHz hybrid active phase shifter using the vector sum method is shown in Fig. 1 [6]. The dual-gate field-effect transistors (DGFETs) were used for the variable gain amplifiers (VGAs) to adjust the gain to achieve the phase shift. However, the operating frequency of the phase shifter is limited to low microwave frequencies since the variations of the parasitic parameters in a packaged DGFET model are increased at high frequencies [7]. The other disadvantage is the large size and asymmetry of VGAs when implemented with a packaged DGFET for VGAs. Instead of using a packaged DGFET, there are two basic monolithic-microwave integrated-circuit (MMIC) VGA design approaches proposed in [8]. The first one is the current steering technique usually designed in an emitter coupled transistor network. The other method used for gain control adopts an electronically controlled variable resistor in the parallel path of a common-emitter amplifier. These two VGA design approaches are well suited to replace the DGFET and to be integrated into the circuit.

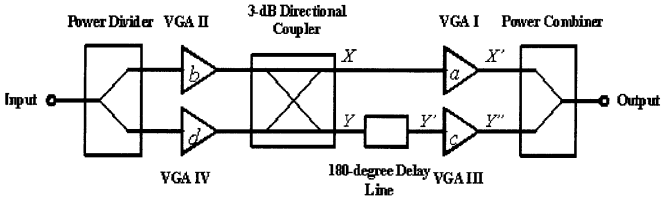

Fig. 1. Architecture of an active phase shifter using a vector sum theorem.

In this paper, we propose to use a similar VGA architecture as reported in [8] to implement the active phase shifters and successfully extended the operating frequency to 20 GHz. Two K-band active phase shifters using GaAs-based HBT and high electron-mobility transistor (HEMT) MMIC technologies, respectively, were designed, fabricated, and tested. The measurement results of these two chips demonstrated the phase-shifting function with a phase error of 11°. Since the gain and phase of the VGA will both affect the performance of the active phase shifter, the sensitivity of the phase-shifter performance due to the phase and gain deviations of the VGA was also investigated.

This paper is organized as follows. In Section II, the design equations of active phase shifters are presented in detail. Furthermore, the sensitivity of the phase shifter due to the VGA are taken into consideration and discussed. Section III describes design and simulation of the active phase shifters using HBT and HEMT MMIC technologies at K-band. The critical components are the VGAs, which are realized with the two different VGA design approaches. The experiment results of the 18-GHz HBT and 20-GHz HEMT MMIC active phase shifter are presented in Section IV.

II. Theoritical Analysis

The proposed active phase shifter using the vector sum method includes the following passive elements:

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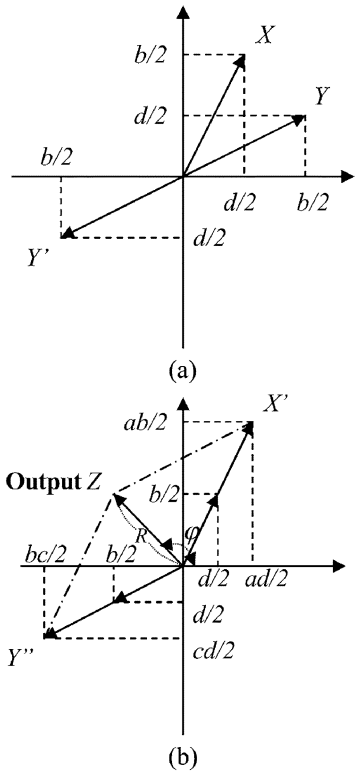

Fig. 2. (a) Vector diagram of an active phase shifter at the input of second stage VGAs. (b) Vector diagram of an active phase shifter at the output of second-stage VGAs. (Vector X, X', Y, Y', and Y'' are defined in Fig. 1.)

TABLE I
GAIN STATES OF THE FOUR VGAS FOR EIGHT PHASE STATES OF A PHASE SHIFTER

VGA	Gain	0°	45°	90°	135°	180°	225°	270°	315°
Amp I	*a*	***H***	***H***	***H***	***H***	***L***	***L***	***L***	***H***
Amp II	*b*	***L***	***H***	***H***	***H***	***H***	***H***	***L***	***L***
Amp III	*c*	***L***	***L***	***L***	***H***	***H***	***H***	***H***	***H***
Amp IV	*d*	***H***	***H***	***L***	***L***	***L***	***H***	***H***	***H***

(***H***: high-gain state; ***L***: low-gain state)

1) 3-dB quadrature coupler;
2) 180° delay line;
3) power combiner/divider together with four VGAs similar to that in [6].

The architecture of an active phase shifter is shown in Fig. 1 with VGA I, VGA II, VGA III, and VGA IV indicating the four different VGAs, and the gain of the corresponding amplifier is a, b, c, and d, respectively. The vector analysis has been derived in [6]. For K-band applications, the gain and phase imbalance in VGAs will significantly degrade the phase-shifter performance and, thus, the error analysis of the vector sum method is further investigated in this paper.

Fig. 2(a) illustrates the vector diagram at the input of second-stage VGAs, where X and Y represent the vectors at the output of a 3-dB directional coupler, and Y' is the output of a 180° delay line. The gain difference between VGA II and VGA IV can create the phase difference between vector X and Y. After adding a 180° delay line at the lower signal path, X and Y' can be placed in different quadrants, which is essential to generate an output vector Z in Fig. 2(b) that can cover four quadrants.

From the vector diagram shown in Fig. 2(a) and (b), the output vector Z can be thought of as the sum of four RF signals on the axes, i.e., ab, ad, bc, and cd. If we need the output vector Z pointed to 0°, then the gains a and d should be much higher than gains b and c. If we need the output vector Z located at the first quadrant, then the gains a, b, and d should be much higher than gain c. According to Fig. 2(b), the output vector Z can be derived as

$$Z = X' + Y' = \left(\frac{ad}{2} - \frac{bc}{2}\right)\mathbf{a_x} + \left(\frac{ab}{2} - \frac{cd}{2}\right)\mathbf{a_y} \qquad (1a)$$

or expressed in another form as follows:

$$Z = R\cos\varphi\mathbf{a_x} + R\sin\varphi\mathbf{a_y}$$

where

$$R = \frac{1}{2}\sqrt{(a^2+c^2)(b^2+d^2) - 4abcd}$$
$$\varphi = \tan^{-1}\left(\frac{ab-cd}{ad-bc}\right). \qquad (1b)$$

According to (1a) and (1b) described above, the phase of the output signal can be tuned to the desired phase if the gains of the VGAs are properly adjusted.

In a 3-bit digital phase shifter, there are eight phase states, i.e., 0°, 45°, 90°, 135°, 180°, 225°, 270°, and 315°. There are two cases of the gains states in each stage VGA; i.e., one is higher or lower than the other. For the eight states of the phase control, two gain states of four VGAs could result in 16 combinations of the gain states of VGAs in a phase shifter. There is an economic way to reduce the numbers of the gain states required to control [6]. The relation between the eight phase states and the four VGAs gain states as proposed in [6] are listed in Table I, where ***H*** is the high-gain state and ***L*** is the low-gain state.

According to Table I, there exist two operation conditions, i.e., (I): two VGAs are in the high-gain state and two VGAs are in the low-gain state and (II): three VGAs are in the high-gain state and one is in the low-gain state. To achieve the gain balance in each phase state of phase shifter, the magnitudes of these two cases should be equal. In this situation, parameter R in (1b) is derived by higher gain M and lower gain kM. The variable k is set that $0 < k < 1$. The equation is obtained as follows [6]:

$$\sqrt{2}M^2(1-k) = M^2\left(1-k^2\right). \qquad (2)$$

The roots of $k = 1$ and $k = \sqrt{2} - 1$ are obtained in (2) and only $k = \sqrt{2}-1$ is inside the range of k. The 3-bit phase control can be achieved through a combination of the two gain states of four VGAs with 7.66 dB $(-20\log(\sqrt{2}-1))$ gain difference.

There are some assumptions for the discussion above about how to operate the phase shifting of the circuit effectively. First, according to the algorithm described above, the VGA operating in the high- and low-state gains must have the same phase of the small-signal gain. The other is that the low- and high-state gains of the VGA need to have 7.66-dB gain difference to achieve gain balance of each phase state in the phase shifter. However, the phase equivalence and gain difference of high and low operating states of the VGA are difficult to realize simultaneously.

For convenience of analysis, the sensitivity of the active phase shifter due to the VGA, the S_{21} phase deviation of high- and low-gain state of VGAs, is defined as $\Delta\varphi$. The gain-difference deviation of the VGA is defined as $\Delta\kappa$. The phase deviation and gain imbalance of the resulted active phase shifter are defined as $\Delta\theta$ and ΔK, respectively.

A. Phase Deviation of Phase Shifter due to VGA Phase- and Gain-Difference Deviation

Case (I): Two high-gain VGAs and two low-gain VGAs.

From the previous section, there are two operating conditions that lead to difference phase deviation. In Case (I), there are two amplifiers in high states and two in low states. The VGA states of 0° phase state, e.g., are

$$a = M\angle 0^\circ = Me^{j0} \tag{3a}$$
$$b = (k\cdot\Delta\kappa)M\angle\Delta\varphi = (k\cdot\Delta\kappa)Me^{j\Delta\varphi} \tag{3b}$$
$$c = (k\cdot\Delta\kappa)M\angle\Delta\varphi = (k\cdot\Delta\kappa)Me^{j\Delta\varphi} \tag{3c}$$
$$d = M\angle 0^\circ = Me^{j0}. \tag{3d}$$

From (1a), the output vector can be obtained such that

$$\begin{aligned} Z &= \frac{1}{2}(M^2 - (k\cdot\Delta\kappa)^2M^2e^{j2\Delta\varphi}) \\ &= \frac{1}{2}\left[M^2 - (k\cdot\Delta\kappa)^2M^2\cos(2\Delta\varphi)\right] \\ &\quad - \frac{j}{2}\left[(k\cdot\Delta\kappa)^2M^2\sin(2\Delta\varphi)\right] \end{aligned} \tag{4}$$

The phase deviation $\Delta\theta$ can be derived from the real and imaginary parts of (4) with the parameters $\Delta\varphi$ and $\Delta\kappa$ being considered. The detailed derivation is shown in Appendix A. The final results of $\Delta\theta$ in Case (I) is

$$\Delta\theta = \tan^{-1}\frac{-(k\cdot\Delta\kappa)^2\sin(2\Delta\varphi)}{1-(k\cdot\Delta\kappa)^2\cos(2\Delta\varphi)}. \tag{5}$$

Case (II): Three high-gain VGAs and one low-gain VGA.

In Case (II), there are three amplifiers in the high-gain state and the other is in the low-gain state. The VGA states of 45° phase state, e.g., are

$$a = M\angle 0^\circ = Me^{j0} \tag{6a}$$
$$b = M\angle 0^\circ = Me^{j0} \tag{6b}$$
$$c = (k\cdot\Delta\kappa)M\angle\Delta\varphi = (k\cdot\Delta\kappa)Me^{j\Delta\varphi} \tag{6c}$$
$$d = M\angle 0^\circ = Me^{j0}. \tag{6d}$$

From (1a), the associated output vector Z is

$$\begin{aligned} Z &= \frac{1}{2}\left(M^2 - (k\cdot\Delta\kappa)M^2e^{j\Delta\varphi}\right) \\ &\quad + \frac{j}{2}\left(M^2 - (k\cdot\Delta\kappa)M^2e^{j\Delta\varphi}\right) \\ &= \frac{M^2}{2}\left[1 + (k\cdot\Delta\kappa)(\sin\Delta\varphi - \cos\Delta\varphi)\right] \\ &\quad + j\frac{M^2}{2}\left[1 - (k\cdot\Delta\kappa)(\sin\Delta\varphi + \cos\Delta\varphi)\right]. \end{aligned} \tag{7}$$

The phase deviation $\Delta\theta$ in Case (II) can be derived similarly as in Case (I). The detailed derivation of Case (II) is shown in Appendix B. The final results of $\Delta\theta$ in Case (II) is

$$\Delta\theta = \tan^{-1}\frac{-(k\cdot\Delta\kappa)\sin(\Delta\varphi)}{1-(k\cdot\Delta\kappa)\cos(\Delta\varphi)} \tag{8}$$

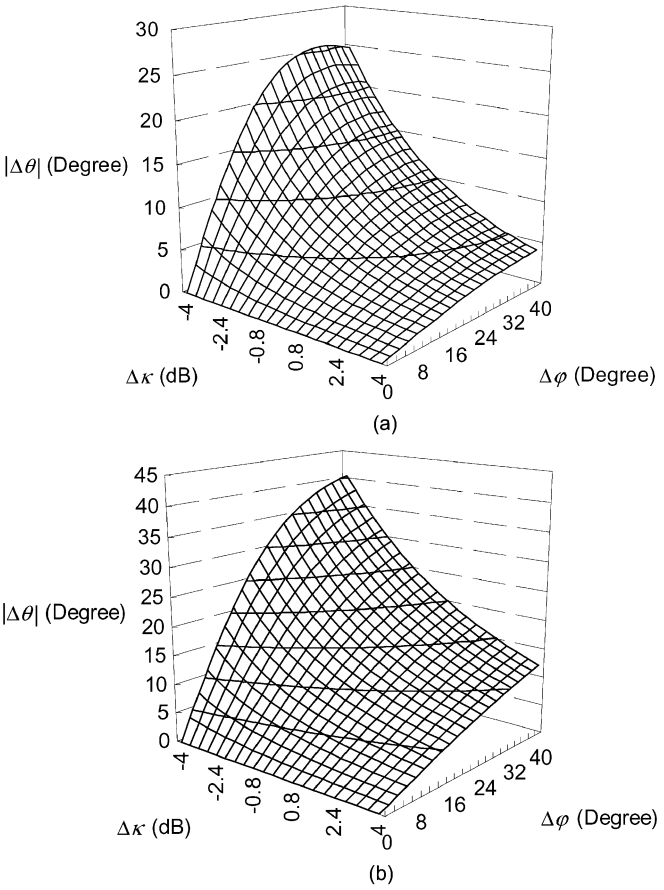

Fig. 3. (a) Influence of phase error $\Delta\theta$ with gain-difference deviation $\Delta\kappa$ and phase deviation $\Delta\varphi$ in Case (I). (b) The influence of phase error $\Delta\theta$ with gain-difference deviation $\Delta\kappa$ and phase deviation $\Delta\varphi$ in Case (II).

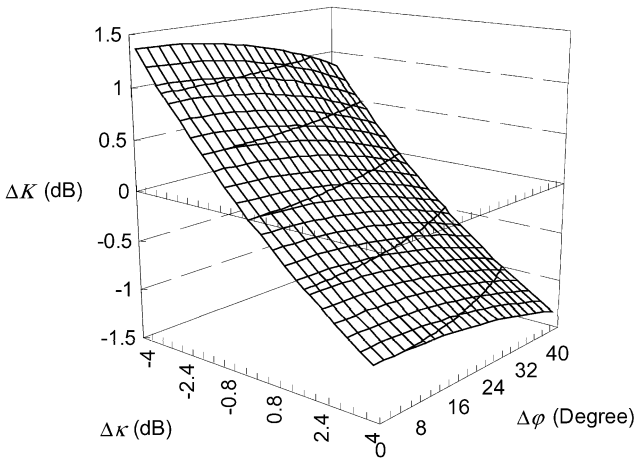

Fig. 4. Influence of gain imbalance ΔK with gain-difference deviation $\Delta\kappa$ and phase deviation $\Delta\varphi$.

According to (5) and (8), Fig. 3(a) and (b) illustrates total phase-shifter phase errors $\Delta\theta$ related to the phase difference of S_{21} of the VGA as $\Delta\varphi$ or Cases (I) and (II). The results explain that the phase error of the phase shifter will be larger than 10° if $\Delta\varphi$ is larger than 30° even if 7.66 dB ($\Delta\kappa = 0$ dB) of gain difference is achieved exactly. Once gain difference reaches

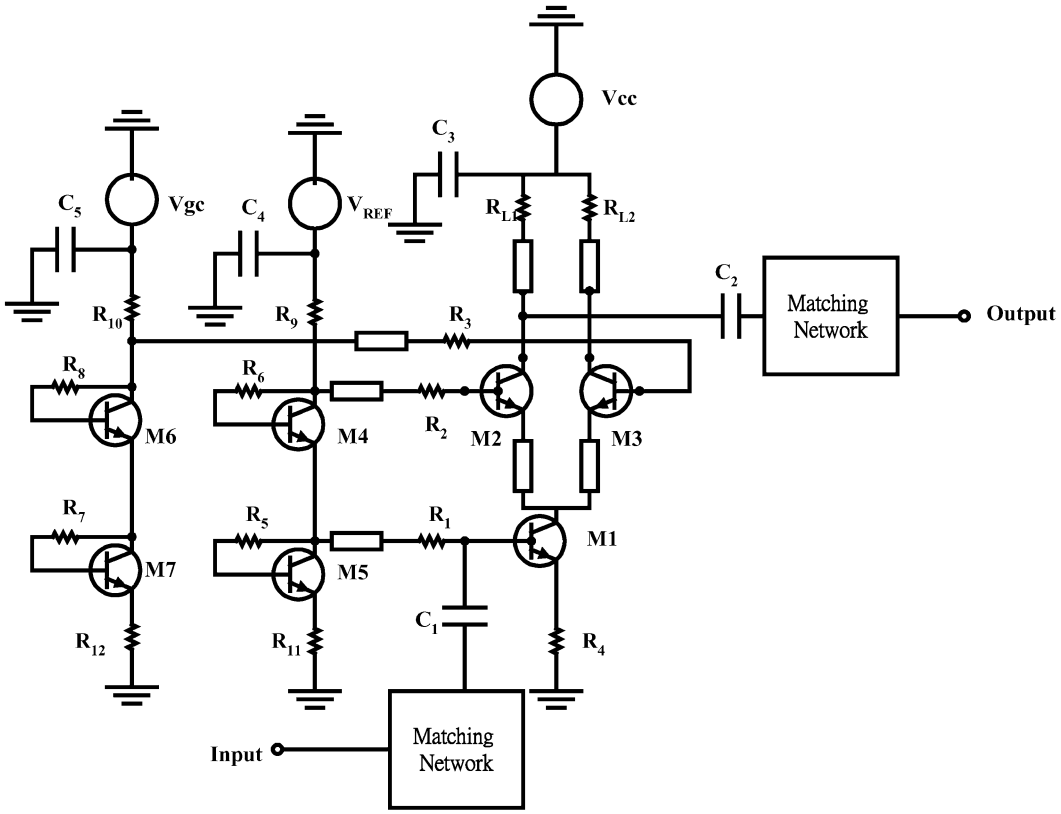

Fig. 5. Architecture of the VGA using a GaAs HBT process.

9.66 dB ($\Delta\kappa = 2$ dB), the phase error will add at least 5° when $\Delta\varphi$ is larger than 20°.

B. Gain Imbalance of Phase Shifter due to VGA Phase- and Gain-Difference Deviation

It was described that, in order to achieve gain balance of different phase states in the phase shifter, the high- and low-state gain should separate 7.66 dB. However, the phase difference of $S_{21}(\Delta\varphi)$ between the high- and low-gain states of VGAs will affect the gain imbalance of the phase shifter. Besides, the gain difference is not easily adjusted to achieve 7.66 dB over the entire band. Due to the variation in the MMIC process, the devices will have different bias conditions to achieve the same performance in different circuits. Thus, S_{21} phase deviation of high- and low-gain states of VGAs, i.e., $\Delta\varphi$, and magnitude difference deviation of the VGA $(\Delta\kappa)$ both need to be included in the derivation of the gain imbalance in phase shifters. The high-state gain is defined as M and the low-gain state is defined as $(k \cdot \Delta\kappa)M$, where $k = \sqrt{2} - 1$. From deriving (4) and (7) for Cases (I) and (II), respectively, the magnitudes of the output vectors are

$$|Z_1| = \frac{M^2}{2}\sqrt{1 + (k \cdot \Delta\kappa)^4 - 2(k \cdot \Delta\kappa)^2 \cos 2\Delta\varphi} \tag{9}$$

and

$$|Z_2| = \frac{M^2}{\sqrt{2}}\sqrt{1 + (k \cdot \Delta\kappa)^2 - 2(k \cdot \Delta\kappa) \cos \Delta\varphi} \tag{10}$$

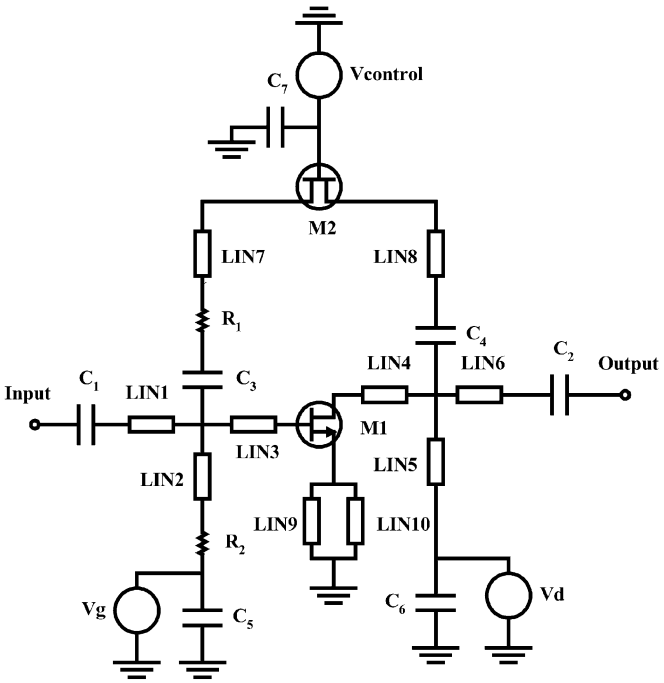

Fig. 6. Architecture of a VGA using a GaAs HEMT process.

where $|Z_1|$ and $|Z_2|$ are the magnitudes of the output vectors of the phase shifter in Cases (I) and (II), respectively.

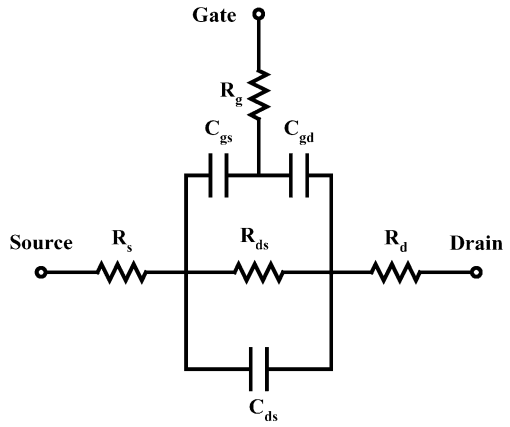

Fig. 7. Equivalent circuit of a variable resistance FET.

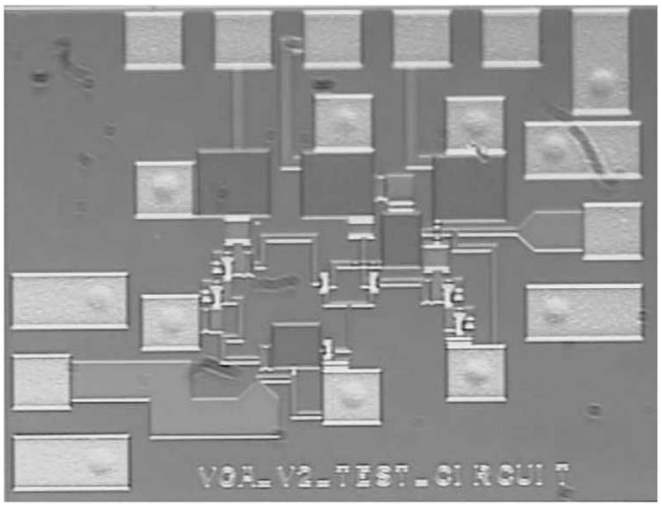

Fig. 8. Chip photograph of the 18-GHz VGA as a test circuit.

The magnitude of the gain imbalance parameter ΔK is expressed as follows:

$$\Delta K = \frac{|Z_2|}{|Z_1|} = \frac{\sqrt{2}M^2\sqrt{1+(k\cdot\Delta\kappa)^2-2(k\cdot\Delta\kappa)\cos\Delta\varphi}}{M^2\sqrt{1+(k\cdot\Delta\kappa)^4-2(k\cdot\Delta\kappa)^2\cos 2\Delta\varphi}}. \tag{11}$$

The mathematical form of gain imbalance of a phase shifter is calculated with MATLAB and is shown in Fig. 4. The gain imbalance and magnitude difference deviation $\Delta\kappa$ are transformed to a decibel unit for convenience. In simulation, the gain imbalance would be larger than 1 dB if magnitude $|\Delta\kappa|$ is larger than 3 dB. However the phase difference $\Delta\varphi$ does not strongly influence the gain imbalance. It is observed that, even with 40° phase deviation, it only results in 0.5-dB gain imbalance in maximum.

III. Circuit Design

The components of the active phase shifter are a 3-dB 90° directional coupler, power combiner/divider, 180° delay line, and four VGAs. The Lange-coupler architecture are adopted for the 3-dB 90° directional coupler in these two MMIC processes. The power divider and combiner use a Wilkinson structure [9]. Based on the vector sum method, an 18-GHz HBT MMIC active phase shifter and a 20-GHz HEMT MMIC active phase shifter are designed.

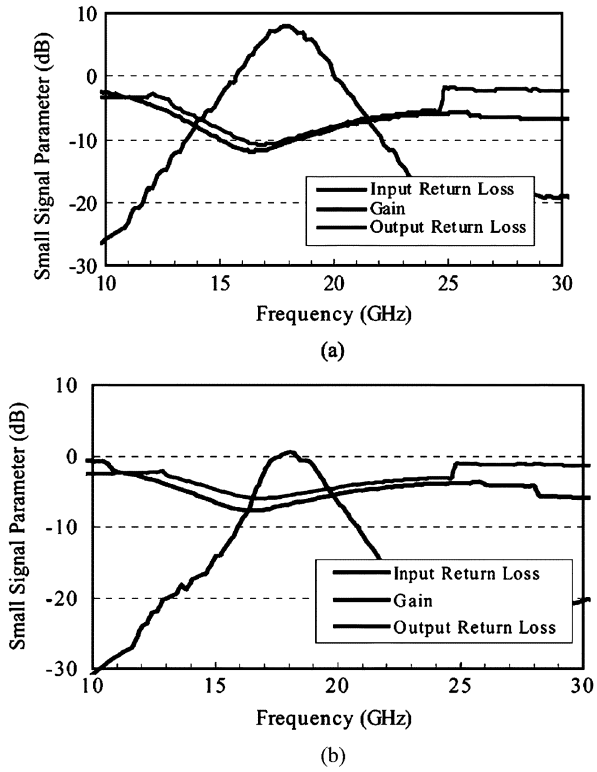

Fig. 9. Measured results of a 18-GHz VGA for the: (a) high- and (b) low-gain state.

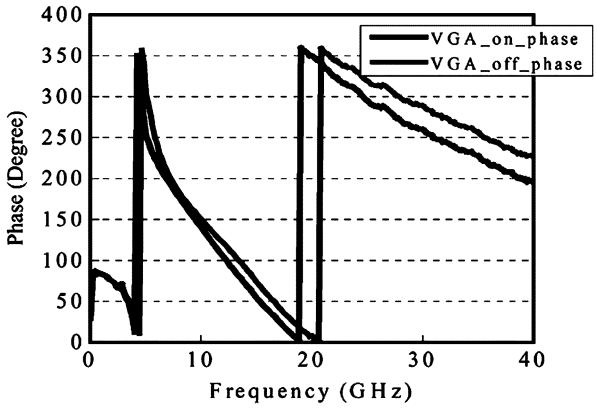

Fig. 10. Measured low- and high-grain state S_{21} phase comparison of the 18-GHz VGA.

A. 18-GHz HBT MMIC Active Phase Shifter

The active phase-shifter circuit was fabricated using a GaAs HBT MMIC foundry on a 4-mil GaAs substrate provided by the WIN Semiconductors Corporation, Taiwan, R.O.C. The emitter size of the HBTs was 2 μm × 10 μm. This HBT device has a unit current gain frequency of 36 GHz and a maximum oscillation frequency of 64 GHz. The maximum current density of the collector metal is 1.5 mA/μm. The thin-film resistor of this process has a sheet resistance of 50 $\Omega/\square$ using sputtered TaN. The through via-holes used for grounding are realized by an inductively coupled plasma (ICP) etch.

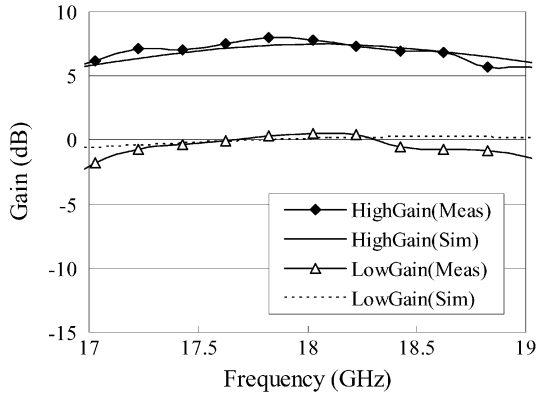

Fig. 11. In-band measured and simulated low- and high-gain state S_{21} comparison of the 18-GHz VGA. The gain difference between low- and high-grain state is very close to the theoretical gain difference (7.66 dB).

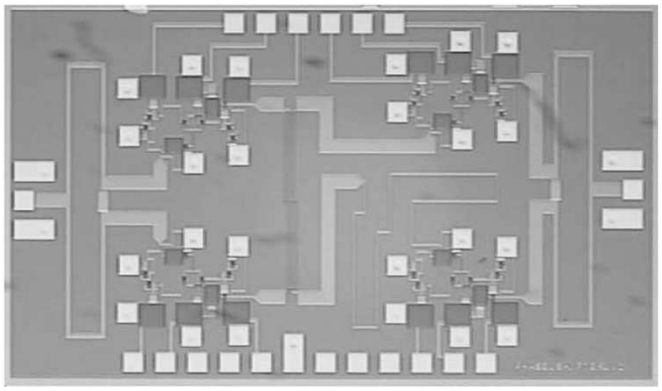

Fig. 12. Chip photograph of the 18-GHz HBT active phase shifter.

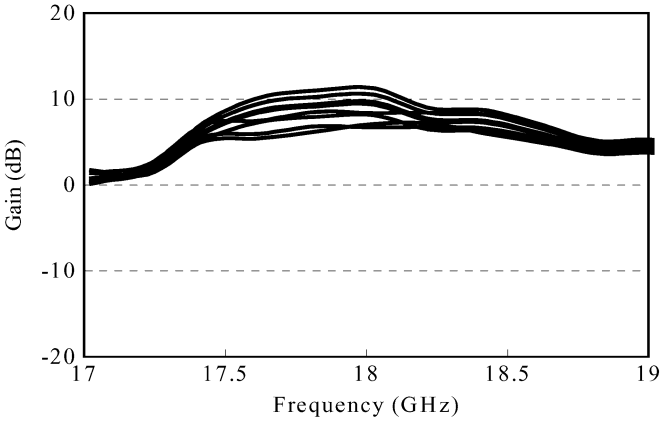

Fig. 13. Measured gain for different phase states of an 18-GHz HBT active phase shifter.

The critical components in the HBT phase shifter are VGAs, which adopt the current steering topology. The architecture is similar to the circuits in [10] and [11]. It provides the single-ended input/output to allow simple connection with other components. The schematic diagram of the VGA is shown in Fig. 5. The emitter-coupled pair (M2, M3) follows input transistor M1. The resistor R_4 provides the feedback of the first stage and stabilizes the dc biasing due to temperature variation. The resistors R_{L1} and R_{L2} are used for better return loss in the common base connected second stage M2. The input transistor M1 and output transistor M2 are biased with transistors M4 and M5 from the voltage source V_{CC}. The comparing transistor M3 has a base current from current mirrors M6 and M7. The resistors R_5, R_6, R_7, and R_8 added between the collectors and bases of transistors M4–M7 are used for the base-current stabilization and protection from current rising. The matching network is used in both input and output ports to optimize the performance at 18 GHz.

The gain of the VGA is controlled with two external voltage sources. The reference voltage (V_{REF}) gives a fixed voltage to activate transistors M1 and M2. By setting the control voltage (V_{gc}) to zero, the comparing transistor M3 is closed and all the bias current goes through the output transistor (M2); thus, the gain is in a high state. On the contrary, by setting the control voltage (V_{gc}) to high voltage, the dummy transistor M3 shares the bias current and the current going through M2 decreases; thus the gain of the VGA is low.

The active phase shifter designed at 18 GHz is composed of VGAs described above and other passive components. The length of a 180° delay line is a 3100-μm line with a linewidth of 10 μm. The lines connecting these elements are also taken into consideration. In the two main branches of the phase shifter, the connecting lines are of equal length and have 50-Ω characteristic impedance to prevent phase imbalance.

B. 20-GHz HEMT MMIC Active Phase Shifter

The 20-GHz HEMT active phase shifter was implemented using an AlGaAs–InGaAs–GaAs 0.15-μm low-noise pseudomorphic high electron-mobility transistor (pHEMT) process on a 4-mil GaAs substrate provided by the WIN Semiconductors Corporation. This HEMT device has a unit current gain frequency of 100 GHz and a maximum oscillation frequency of 165 GHz. The HEMT gatewidth of 50 μm with two fingers was chosen to achieve high-frequency operation to 20 GHz.

The architecture of the VGA in an HEMT process uses a variable feedback transistor architecture [12], [13]. The configuration is shown in Fig. 6. The amplifier consists of a field-effect transistor (FET) (M1) for amplification, an FET (M2) as a variable resistor, capacitors, fixed resistors, and a matching network. The dominant FET (M1) with a common source configuration is connected with a source inductor to improve the stability. Resistor R_2 is also used for stability of the circuit. DC blocking capacitors C_1 and C_2 are placed in the input/output ports. The bypass capacitors C_5 and C_6 are all large enough to provide a nearly RF short to ground at 20 GHz. The voltage source (V_{control}) gives the transistor M2 gate bias with bypass capacitor C_7.

The equivalent circuit of the FET M2, as a variable resistor or a switch, is shown in Fig. 7. Drain and source terminals of M2 are floating. While the gate control voltage (V_{control}) is set to a low value, the intrinsic resistor R_{ds} of M2 is high. The VGA works as a normal amplifier as usual. It is also well known that when R_{ds} of transistor M2 is adjusted to a small resistance value, a strong negative feedback will occur and the gain of the VGA will drop. Finally, the total phase-shifter circuit designed at 20 GHz is simulated with all the components described above.

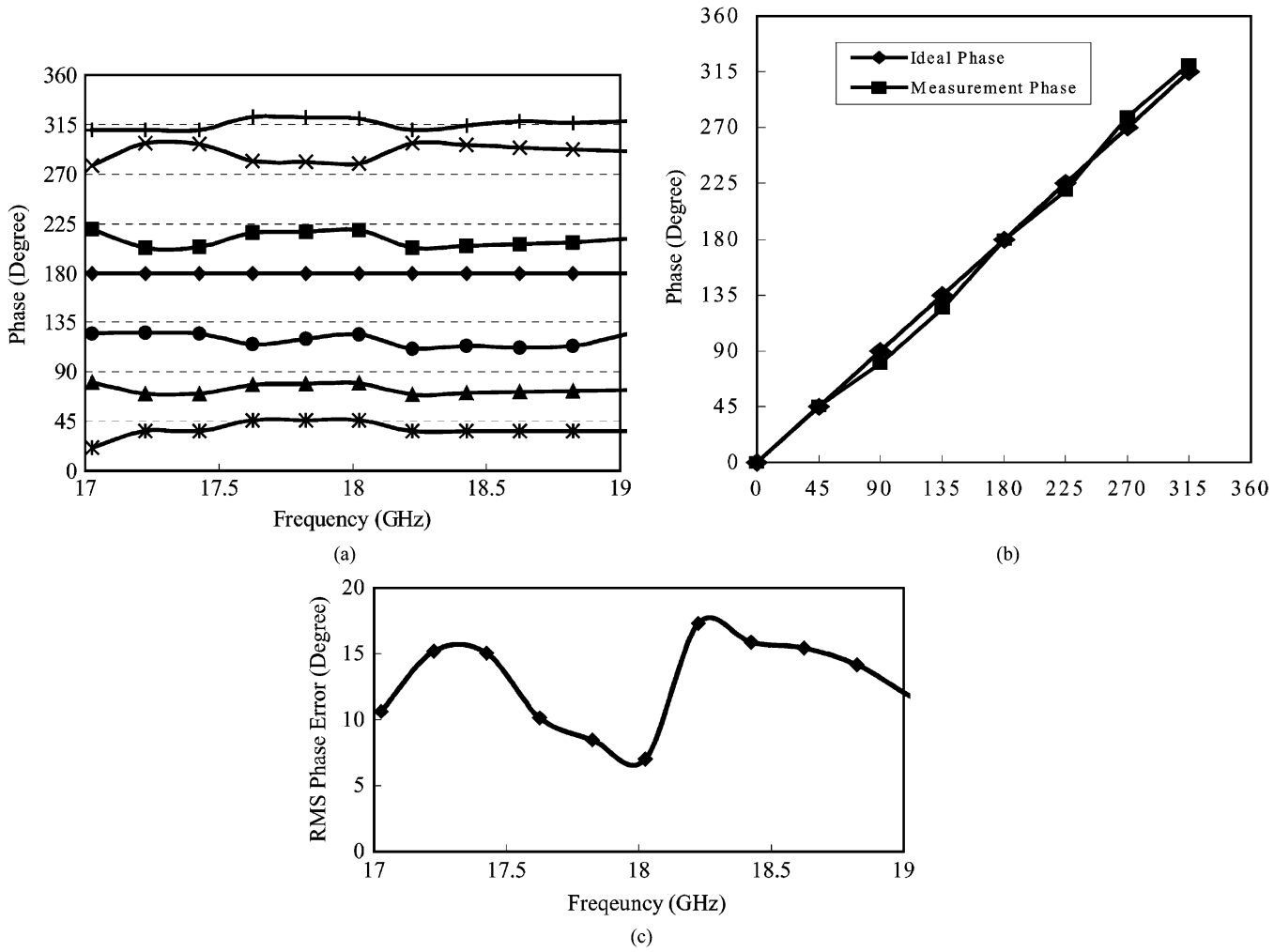

Fig. 14. (a) Measured phases for eight states of a 18-GHz phase shifter. (b) Comparison of the ideal and measured phase at fixed 18 GHz. (c) Root-mean-square phase error.

The advantage in using a variable feedback transistor architecture in the HEMT process is that the HEMT transistors can provide a better characteristic of a variable resistor than the HBTs. For chip area concerns, the HEMT process is not suitable for the current steering design.

IV. Measurement Results

A. 18-GHz HBT MMIC Active Phase Shifter

The chips including the VGA and phase shifter are measured via on-wafer probing. Fig. 8 presents a photograph of the test circuit: a VGA with a chip size of 1.2 mm $\times$ 1.0 mm. The chip on a high-gain state is biased at $V_{cc} = 7$ V and $I_{cc} = 28$ mA, while $V_{\rm REF} = 6.2$ V, $I_{\rm REF} = 25$ mA, and V_{gc} is set to 0 V. For low-gain state, V_{gc} is risen up to 5.3 V. The measured high- and low-gain state performance of the VGA are presented in Fig. 9(a) and (b), respectively. The gain achieves 7.83 dB at 18 GHz in the high state and decreases to 0.56 dB when turned to a low-gain state, as expected. The S_{21} phase difference between two gain states, illustrated in Fig. 10, is 17° at 18 GHz. Fig. 11 plots the in-band measured and simulated VGA gain performance using Agilent's ADS simulator and the Gummel–Pool model provided by the foundry. The data can be used to estimate the phase error and gain imbalance of phase shifter with (5), (8), and (11).

The active phase-shifter chip photograph is shown in Fig. 12 with a chip size of 3 mm $\times$ 2 mm. Fig. 13 shows the small-signal gain of eight states with an average gain of 8.87 dB. The maximum gain is 11 dB and the minimum one is 6.7 dB. The measured phase performance over 17–19 GHz is exhibited in Fig. 13(a), while phase states at 18 GHz are compared to an ideal phase, as shown in Fig. 14(b). The maximum phase error of the phase state at 18 GHz is 11°, while the minimum one is 0.63°. The plotted root-mean-square phase error reached 6.9° in Fig. 14(c). To compare the theoretical error analysis in Section II with the measured results, the measured phase difference of two different states in the VGA is 17° in Fig. 10. It is also observed that the measured gain-difference deviation $(\Delta\kappa)$ is from -2 to 2 dB due to the VGA port mismatch and bias point variations. According to the theoretical estimation in Figs. 3 and 4, the measured phase- and gain-difference deviation between two VGAs can produce larger than 15° phase error and 2-dB gain imbalance in the active phase shifter, respectively. The theoretical minimum phase error at 0-dB gain difference and 17° phase difference is 6.4° in Fig. 3, which is consistent with the measured minimum root-mean-square phase error 6.9° in Fig. 14.

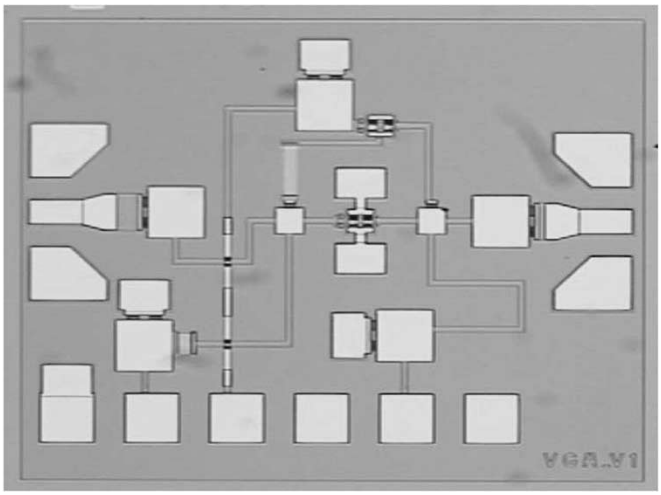

Fig. 15. Chip photograph of the 20-GHz VGA as a test circuit.

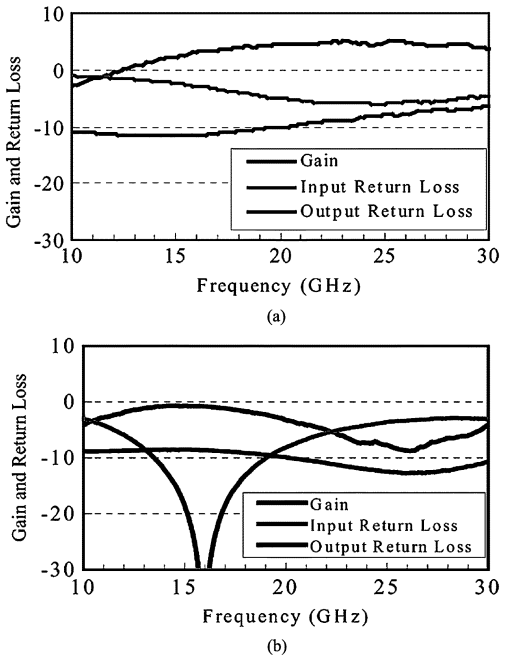

Fig. 16. Measured results of the 20-GHz HEMT VGA for the: (a) high- and (b) low-gain state.

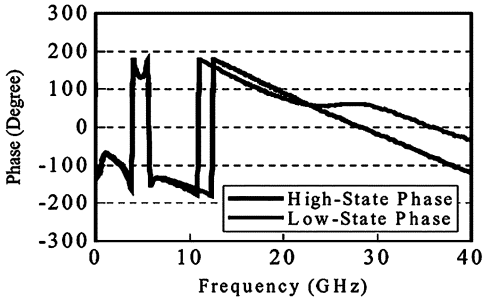

Fig. 17. Measured low- and high-grain state S_{21} phase comparison of the 20-GHz HEMT VGA.

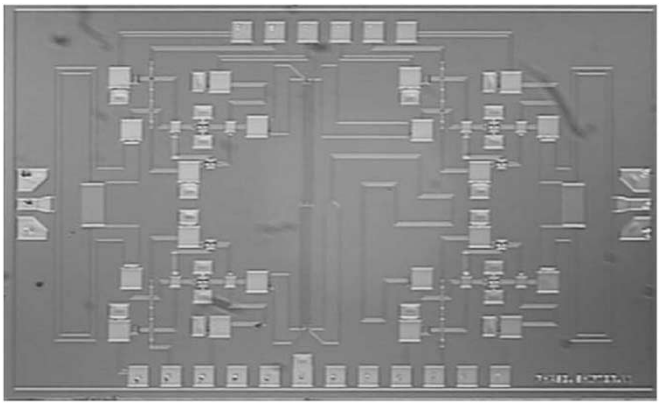

Fig. 18. Chip photograph of the 20-GHz HEMT active phase shifter.

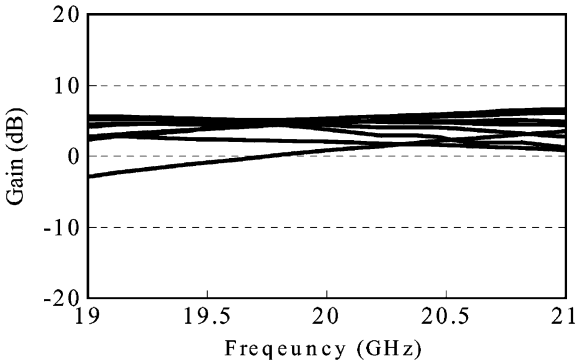

Fig. 19. Measured gain for different phase states of the 20-GHz HEMT active phase shifter.

B. 20-GHz HEMT MMIC Active Phase Shifter

The chip photograph of the HEMT VGA test circuit is presented in Fig. 15 with a chip size of 1.2 mm $\times$ 1 mm. The high-gain state reaches 4.6 dB and turns to -3.2 dB when the low-gain state is operated at 20 GHz. The results are illustrated in Fig. 16(a) and (b). The plotted phase difference between the low- and high-gain states at 20 GHz is 14° in Fig. 17.

Fig. 18 shows the chip photograph of the total phase shifter with a chip size of 3 mm $\times$ 2 mm. The small-signal gain of the phase shifter corresponding to eight phase states is presented in Fig. 19. The phases of eight states from 19 to 21 GHz are plotted in Fig. 20(a). The maximum and minimum phase errors at 20 GHz are 11° and 2.3°, respectively. Fig. 20(b) gives the measured eight state phases compared to an ideal phase at 20 GHz. The maximum gain of phase states is 5 dB and the minimum one is 1 dB. The average gain is 3.85 dB. To compare the theoretical error analysis in Section II with the measured results, the measured phase difference of two different states in the VGA is 14° in Fig. 17. The measured gain-difference deviation between two VGAs is also estimated from -2 to 2 dB. According to the theoretical estimation in Figs. 3 and 4, the measured phase- and gain-difference deviation between two VGAs can produce larger than 10° phase error and 2-dB gain imbalance in the active phase shifter, respectively. The theoretical minimum phase error at 0-dB gain difference and 14° phase difference is 5.4° in Fig. 3, which is consistent with the measured minimum root-mean-square phase error 4.7° at 20.4 GHz in Fig. 20.

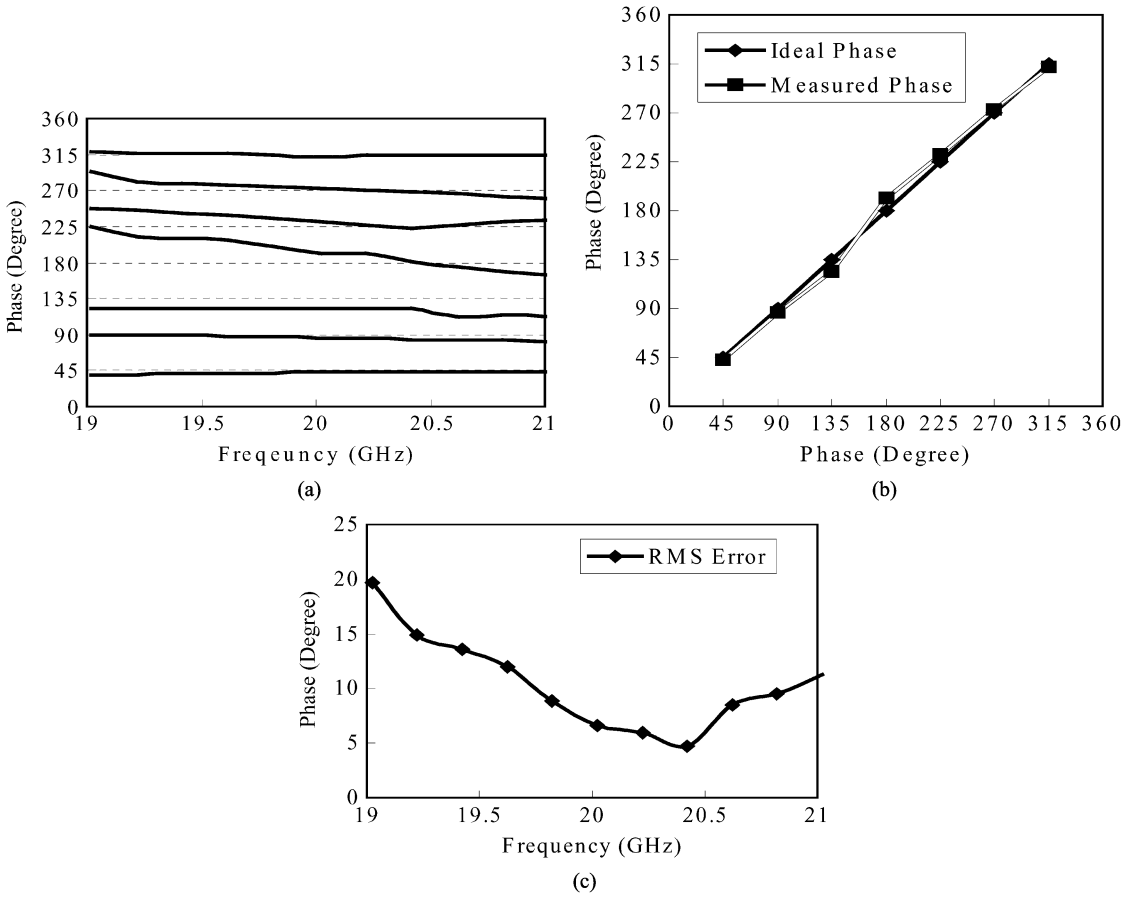

Fig. 20. (a) Measured phases for eight states of the 20-GHz phase shifter. (b) Comparison of ideal and measured phase at fixed 20 GHz. (c) Root-mean-square phase error.

TABLE II
SUMMARIZED MEASUREMENT PERFORMANCE OF HBT AND HEMT ACTIVE PHASE SHIFTERS

	HBT active phase Shifter	HEMT active phase shifter
Frequency	18 GHz	20 GHz
Maximum Phase Error	11°	11°
Measured RMS Phase Error	6.9° (Min.)	4.7° (Min.)
Theoretical Phase Error	6.4° (Min.)	5.4° (Min.)
Average Gain	8.87 dB	3.85 dB
Gain imbalance	4.6 dB	4 dB
Chip Size	3mm x 2mm	3mm x 2mm
Input Return Loss	> 5 dB	> 20 dB
Output Return Loss	> 8 dB	> 5 dB

TABLE III
GAIN STATES OF THE FOUR VGAS FOR CASE (I)

VGA	Gain	0°	90°	180°	270°
Amp I	a	Me^{j0}	Me^{j0}	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$
Amp II	b	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	Me^{j0}	Me^{j0}	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$
Amp III	c	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	Me^{j0}	Me^{j0}
Amp IV	d	Me^{j0}	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	Me^{j0}

V. CONCLUSION

This paper has investigated the designs of two active phase shifter using a vector-sum method. These MMIC circuits using HBT and HEMT processes are designed at K-band. The performances of these circuits are summarized in Table II. The phase deviation and gain imbalance of this phase-shifter architecture have been analyzed and derived in this paper. The minimum phase error from theoretical analysis is consistent with the measured minimum root-mean-square phase error. To our knowledge, this study is the first attempt to design active phase shifters using MMIC technology at 18 and 20 GHz.

APPENDIX A

In Case (I), there are two amplifiers in high states and two in low states. According to Table I, the VGA states of four phase states in Case (I) are shown in Table III. The high-gain state magnitude is set to M and the low-gain state one is kM, where $k=\sqrt{2}-1$.

From Table III and (1a), the output vector Z of four phase states in Case (I) are

$$Z(0^\circ+\Delta\theta)=\frac{1}{2}\left(M^2-(k\cdot\Delta\kappa)^2M^2e^{j2\Delta\varphi}\right) \quad (A.1)$$

$$Z(90^\circ+\Delta\theta)=jZ(0^\circ+\Delta\theta) \quad (A.2)$$

$$Z(180^\circ+\Delta\theta)=-Z(0^\circ+\Delta\theta) \quad (A.3)$$

$$Z(270^\circ+\Delta\theta)=-jZ(0^\circ+\Delta\theta). \quad (A.4)$$

TABLE IV
GAIN STATES OF THE FOUR VGAS FOR CASE (II)

VGA	Gain	45°	135°	225°	315°
Amp Ⅰ	a	Me^{j0}	Me^{j0}	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	Me^{j0}
Amp Ⅱ	b	Me^{j0}	Me^{j0}	Me^{j0}	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$
Amp Ⅲ	c	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	Me^{j0}	Me^{j0}	Me^{j0}
AmpⅣ	d	Me^{j0}	$(k\cdot\Delta\kappa)Me^{j\Delta\varphi}$	Me^{j0}	Me^{j0}

Equation (A.1) can be derived as

$$Z(0^\circ+\Delta\theta)=\frac{1}{2}\left[M^2-(k\cdot\Delta\kappa)^2M^2\cos(2\Delta\varphi)\right]-\frac{j}{2}\left[(k\cdot\Delta\kappa)^2M^2\sin(2\Delta\varphi)\right] \quad (A.6)$$

The phase deviation $\Delta\theta$ can be derived from the real and imaginary parts of (A.6) as follows:

$$\tan(0^\circ+\Delta\theta)=\frac{-M^2(k\cdot\Delta\kappa)^2\sin(2\Delta\varphi)}{M^2\left(1-(k\cdot\Delta\kappa)^2\right)\cos(2\Delta\varphi)}. \quad (A.7)$$

The resulting $\Delta\theta$ is shown in (5), which is applicable to all other three phase states in Case (I), i.e., 90°, 180°, and 270° phase states.

APPENDIX B

In Case (II), there are three amplifiers in high states and one in low state. According to Table I, the VGA states of four phase states in Case (II) are shown in Table IV.

From Table IV and (1a), the output vector Z of four phase states in Case (II) are

$$Z(45^\circ+\Delta\theta)=\frac{1}{2}\left(M^2-(k\cdot\Delta\kappa)M^2e^{j\Delta\varphi}\right)+\frac{j}{2}\left(M^2-(k\cdot\Delta\kappa)M^2e^{j\Delta\varphi}\right) \quad (B.1)$$

$$Z(135^\circ+\Delta\theta)=jZ(45^\circ+\Delta\theta) \quad (B.2)$$

$$Z(225^\circ+\Delta\theta)=-Z(45^\circ+\Delta\theta) \quad (B.3)$$

$$Z(315^\circ+\Delta\theta)=-jZ(45^\circ+\Delta\theta). \quad (B.4)$$

Equation (B.1) can be derived as

$$Z(45^\circ+\Delta\theta)=\frac{1}{2}\left[M^2-(k\cdot\Delta\kappa)M^2\cos(\Delta\varphi)+(k\cdot\Delta\kappa)M^2\sin(\Delta\varphi)\right]+\frac{j}{2}\left[M^2-(k\cdot\Delta\kappa)M^2\cos(\Delta\varphi)-(k\cdot\Delta\kappa)M^2\sin(\Delta\varphi)\right]. \quad (B.5)$$

The phase deviation of the active phase shifter can be obtained as

$$\tan(45^\circ+\Delta\theta)=\frac{1+\tan(\Delta\theta)}{1-\tan(\Delta\theta)}=\frac{1-(k\cdot\Delta\kappa)\cos(\Delta\varphi)-(k\cdot\Delta\kappa)\sin(\Delta\varphi)}{1-(k\cdot\Delta\kappa)\cos(\Delta\varphi)+(k\cdot\Delta\kappa)\sin(\Delta\varphi)} \quad (B.6)$$

then

$$\tan(\Delta\theta)=\frac{-(k\cdot\Delta\kappa)\sin(\Delta\varphi)}{1-(k\cdot\Delta\kappa)\cos(\Delta\varphi)}. \quad (B.7)$$

The resulting $\Delta\theta$ is shown in (8), which is applicable to all other three phase states in Case (II), i.e., 135°, 225°, and 325° phase states.

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