行政院國家科學委員會專題研究計畫 期中進度報告

可應用於軟性電子的TFT電路設計技術之開發--子計畫四：適用於軟性面板製程之高效能數位信號處理器之設計(1/3)

期中進度報告(完整版)

計 畫 類 別 ： 整合型
計 畫 編 號 ： NSC 95-2220-E-002-020-
執 行 期 間 ： 95 年 08 月 01 日至 96 年 07 月 31 日
執 行 單 位 ： 國立臺灣大學電子工程學研究所

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處 理 方 式 ： 期中報告不提供公開查詢

中 華 民 國 96 年 05 月 30 日

行政院國家科學委員會補助專題研究計畫成果報告

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※　　適用於軟性面板製程高效能數位訊號處理器之設計　　※
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中　華　民　國　95 年　5　月　28　日

一、 中文摘要

軟性電子的領域包含了在如塑膠之軟性基板上之元件、材料、電路設計之相關研究，而製作出來的電路天生就有可撓曲或是可摺疊之特性，此外，製造成本也可能可以用 roll-to-roll 的印刷製作技術進一步的降低，故可用以生產出大尺寸、低成本的裝置，也因此可被用於許多新興的產品及應用之上。在另一方面，有一個新的概念，稱為面板系統(system-on-panel)也逐漸被重視，在面板系統中，使用和製作面板像素相同的薄膜電晶體的製程製作類比及數位電路而和面板整合在一起，如此一來，可以進一步降低成本。在面板系統上的數位電路所處理的工作多半跟數位訊號處理有關，在本計畫之中，同時考慮軟性電子以及面板系統，我們的目標為設計一適用於軟性面板製程之高效能之數位信號處理器。

英文摘要

Flexible electronics encompasses a rather diverse range of device, material, and design technology that are built on flexible substrates, such as plastic. The flexible circuits inherently can be rolled or folded, and the cost can be reduced with roll-to-roll printing process. Therefore, the size of the circuits could be large with low cost, which will introduce many new applications, especially for flexible display related applications. In addition, a recent trend called “system-on-panel,” where the analog and digital circuits are implemented with the same TFT (thin-film-transistor) process as the pixels and are integrated with the panel as a system, has picked up steam quite rapidly. Since digital signal processing is always an important task for such kind of applications, the target of this project is to design a high performance digital signal processor on flexible panel process.

二、計畫的緣由與目的

There are many design challenges to design digital circuits on flexible process. The major problems come from the non-ideal properties of the flexible devices, such as the high supply voltage requirement, complex organic/semiconductor junction, lacking of complement transistor technology, immature printing process, device modeling, circuit simulation, low device stabilization, and low mobility. For digital circuit design, low mobility and device stabilization are the main design challenges. Low mobility will cause slow switching speed of the circuits and will constrain the performance of the circuits; device stabilization will lead to the unpredictability of the circuits and will make the circuit design and simulation very difficult.

In this project, we will design a high performance digital signal processing engine conquering these problems in three different levels. In circuit level, we will start from good device modeling for the target flexible process. To deal with the poor device stabilization, that is, the property of different transistors may be quite different, asynchronous design may be a possible solution. We will also consider the global asynchronous local synchronous (GALS) approach, which was used for nano-scale silicon process. In

architecture level, we will try to improve the performance of the digital signal processor with parallel processing technique. The parallel datapath architecture, such as VLIW, will be taken into consideration. Besides, the multiprocessor or array processor architecture will be considered as well. Finally, in the design flow and methodology level, both the design methodologies for digital circuit design on flexible process and asynchronous circuit design will also be discussed in this project.

Flexible electronics will enable a new field of electronics named “macroelectronics” and will introduce new applications and products. Digital circuit design is one of the key issues for flexible electronics. In this project, we will design a digital signal processing engine on flexible process with asynchronous circuit design and parallel architecture. The related design methodologies for digital circuit design on flexible process and asynchronous design will be developed at the same time. We believe the key technologies developed by this project will be valuable for the flexible electronics industry in the future.

三、方法及結果:

Architecture

(1) Technology

Unlike CMOS circuit, flexible electronics often use TFT to implement. The technology we use is the amorphous silicon provided by ITRI. We don’t have accurate model for the amorphous silicon yet. So building an accurate model for amorphous silicon is very important in the first year of this project. To achieve low cost, we only use N-type TFT. Thus we can have half number of masks.

(2) Architecture

To be familiar with amorphous silicon, we use SPICE model from ITRI to do some simulations to get basic parameters, such as threshold voltage. The figure and table below are the I-V curve of the TFT provided by ITRI and simulation environment.

VDD(Volt)	Width(um)	Length(um)	Temperature(°C)
10V	24 um	8 um	27°C

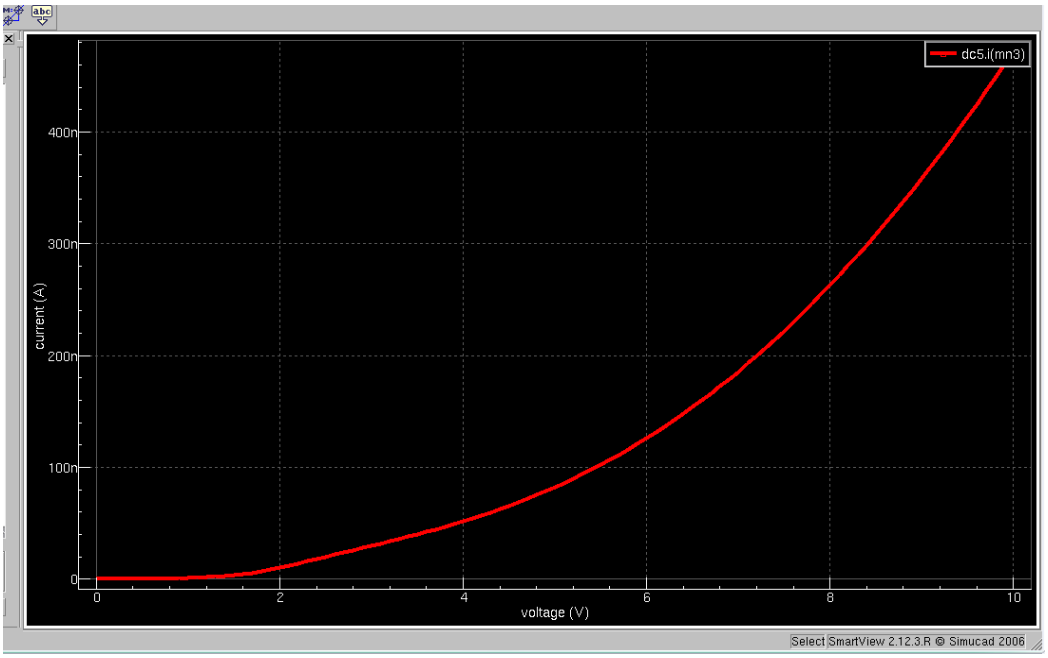
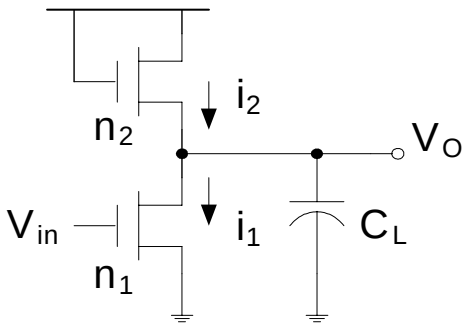


Fig. 1

From Fig. 1 we can see that the threshold voltage of this a-Si TFT is about 1.5 volts.

Because we only have N-type MOS, we can't use circuit technique like CMOS to build symmetric logic. Here we choose pseudo-nmos to implement because it can maintain the property of restoration by using only one type of MOS.

In pseudo-nmos, the pull-up circuit is an always on MOS. So the size ratio of pull-up MOS and pull-down MOS becomes an important issue. From the previous simulation result, the threshold voltage is about 1.5 volts with V_{DD} 10 volts. Here we use this parameter and an inverter to derive the size ratio of pull-up and pull-down circuit.



$$i_1 = k_n \frac{W_1}{L}(V_{in} - V_{th} - \frac{1}{2}V_{OL})V_{OL}$$

$$i_2 = \frac{1}{2}k_n \frac{W_2}{L}(V_{DD} - V_{OL} - V_{th})^2$$

$$i_1 = i_2$$

We can get the relation between $\boldsymbol{V_{OL}}$ and size ratio ***r.***

$$VDD = 10v, Vin = VDD - V_{th} = 8.5v, r = \frac{W_1}{W_2}$$

$$V_{OL} = \frac{17 + 14r - \sqrt{196r^2 + 187r}}{2(r+1)}$$

The follow is a table of V_{OL} with different size ratio ***r.***

r	1	2	3	4	5
V_{OL}***(V)***	2.86	1.83	1.35	1.07	0.88

From the table we can see that for size ratio 3 the output low will be less than threshold voltage, but here we choose size ratio 5 because of the following reasons.

- The SPICE model may not be accurate enough.
- The threshold voltage is just an estimation value from the IV curve, not an accurate value.
- We use inverter to derive the relation of output low and size ratio. But besides the inverter there are other kind of logic gates, such as NAND and NOR.
- TFT parameters may change with environment.

Because the parameters of thin film transistor may change with environment, it is not appropriate to use synchronous circuit. Here we use asynchronous circuit to overcome parameter variation and enhance the circuit performance.

The major difference between synchronous and asynchronous circuit is the existent of global clock. In synchronous circuit, data transfer happens at specific time (clock rising of clock falling) and in asynchronous circuit latches transfer data by using handshake protocol. Handshake protocol is a data transfer method by adding two signals – request and acknowledge. Request is used to ask other latch to transfer data and acknowledge is used to response the data transfer, shown in Fig. 2.

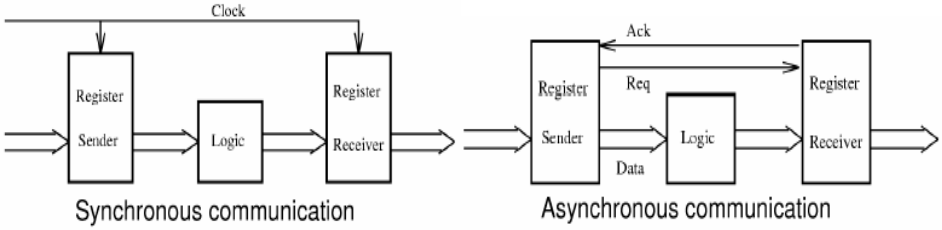


Fig. 2

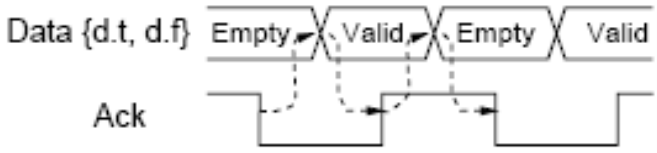
There are several advantages compared with synchronous circuit:

- High operation speed: Thin Film Transistors have different parameters between different transistors and also have parameter variation in different environments. If we design a circuit based on synchronous circuit design, critical path delay may be very long due to some worse transistors although most other transistors work good. This may be inefficient.
- Low power consumption: In synchronous circuit, the clock signal consumes a lot of power.

Although the circuit doesn't have to turn on, the clock signal also consumes power except that we use gated clock to turn it off. But in asynchronous circuit there is no clock signal and it saves a lot of power. If we apply it into some electronic devices, we can use the devices for a longer time and we don't have to frequently recharge the battery.

- Better stability: TFT characteristic may change after turning on for a long time. If we use synchronous circuit, the performance degradation of a transistor may cause timing violations. Thus use handshake protocol becomes a better choice. Handshake protocol transfer the data depends on the characteristic of TFTs. We don't have to worry about the timing problem.
- Modularity: In synchronous circuit if we have to combine circuits with different time domains, we have to design very carefully. But in asynchronous circuit, we can just use handshake protocol to communicate between blocks and blocks.

In asynchronous circuit there are several handshake protocols. The common handshake protocols are 2-phase Bundled-data, 4-phase Bundled-data, 2-phase Dual-rail, and 4-phase Dual-rail. Bundled-data protocol needs path delay in advance. This is not appropriate because we do not know the specific characteristic of TFTs. Thus we choose dual-rail protocol. In dual rail protocol we use two wires to represent one bit signal. One wire represents logic one and the other represents logic zero. The truth table and timing diagram are as follows, where d.t and d.f represent logic one and logic zero, respectively.



	d.t	d.f
Empty ("E")	0	0
Valid "0"	0	1
Valid "1"	1	0
Not used	1	1

Fig 3.

In dual-rail protocol, there is no request signal. Here we use data to represent request. If all the data is valid "0" or valid "1", i.e. not empty, then the latch is ready to transfer data. Thus we don't have to know the path delay in advance. There are 2 kinds of dual-rail protocol. One is 2-phase and the other is 4-phase. The major different between the two protocols is 4-phase protocol will return every wire to 0. Compare with 4-phase protocol, 2-phase protocol use the transition of acknowledge to inform other latches and it needs more complex circuit. In the situation that we don't know the specific characteristic of TFTs and without the EDA tool's help, we choose 2-phase protocol for safety.

In this project, we will design a multiply-and-accumulator (MAC) and a fixed-coefficient FIR filter. We will describe the design process of these two circuits in sequence.

MAC is very important in digital circuit and microprocessors. In the first year of our project, the

MAC is our goal and we will integrate with other components in other subprojects in the future. The following figure illustrates the architecture of an MAC, where L1, L2, and L3 are asynchronous latches.

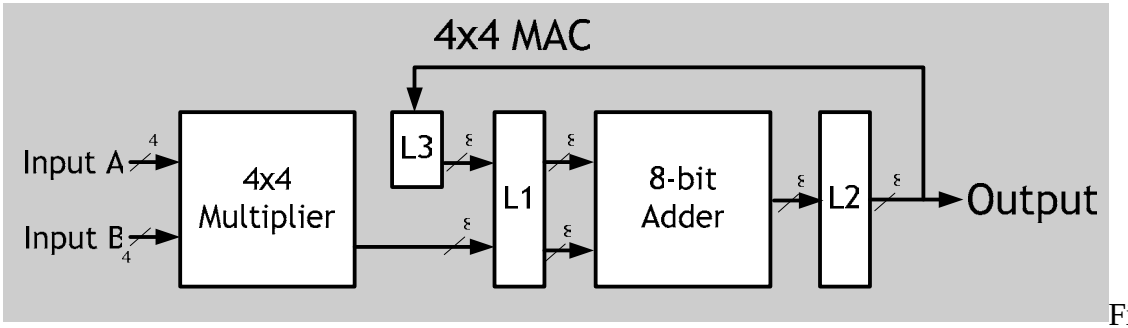


Fig. 4

Multiply-and-accumulator consists of three parts:

(a) Multiplier: Here we implement a 4x4 dual-rail signed multiplier. There are several methods to implement a multiplier. We use Wallace tree, which is based on carry-save adder. This kind of multiplier has shorter operation time to compute the product.

(b) Adder: Because we use handshake protocol, data will not transfer together at specific time. Thus it is not essential to implement the adder with some carry-look-ahead technique. Carry-ripple adder is enough here.

(c) Asynchronous latch: Dual-rail asynchronous latch consists of data and acknowledge signal. The datum has been received if one of the two wires is high. Then set acknowledge high to let the previous latch know that the datum has been received. If both the wires are low, this latch is ready to receive datum. Thus we set acknowledge low to inform the previous latch. The follow is the architecture of asynchronous latch.

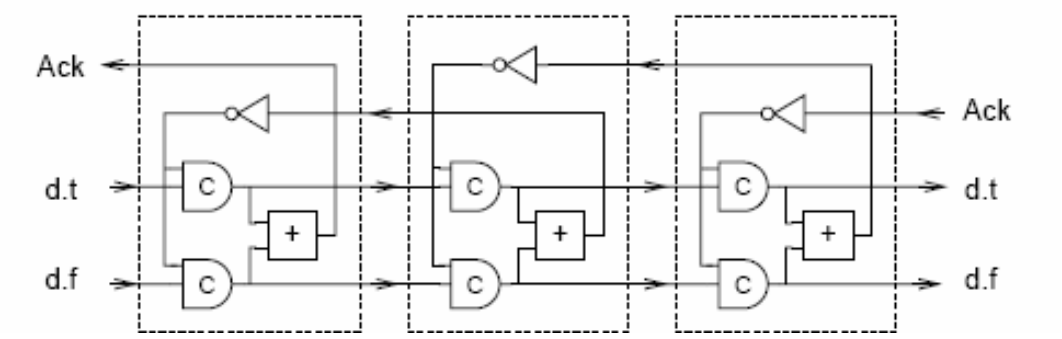


Fig 5

Design Flow

The follows are design flow of MAC.

(1) Use SPICE to measure the amorphous silicon characteristics.

(2) Do transistor-level simulation and verification by using SPICE (pre-layout simulation).

(3) Use Cadence Virtuoso to layout.

(4) Use Calibre to run layout versus schematic(LVS) verification.

Simulation Result

The pre-layout simulation of 4x4 MAC is correct. It can compute about 3000 data per second (like work at 3KHz in synchronous circuit).

Specifications

Power Supply	10V
Data/s	~3000
Transistor Number	3844
Chip Area	12mm*8mm
IO Number	49

(1) A 4x4 MAC out and verify the correctness of functionality.

(2) In addition to 4x4 MAC, we also test some basic logic block, such as full adder and C-Element.

(3) In MAC, the input pattern will go through multiplier first. Thus if we connect the multiplier outputs to chip outputs, then we can verify the functionality of multiplier if the MAC is fail to work. The layout of 4x4 MAC is in Fig. 6.

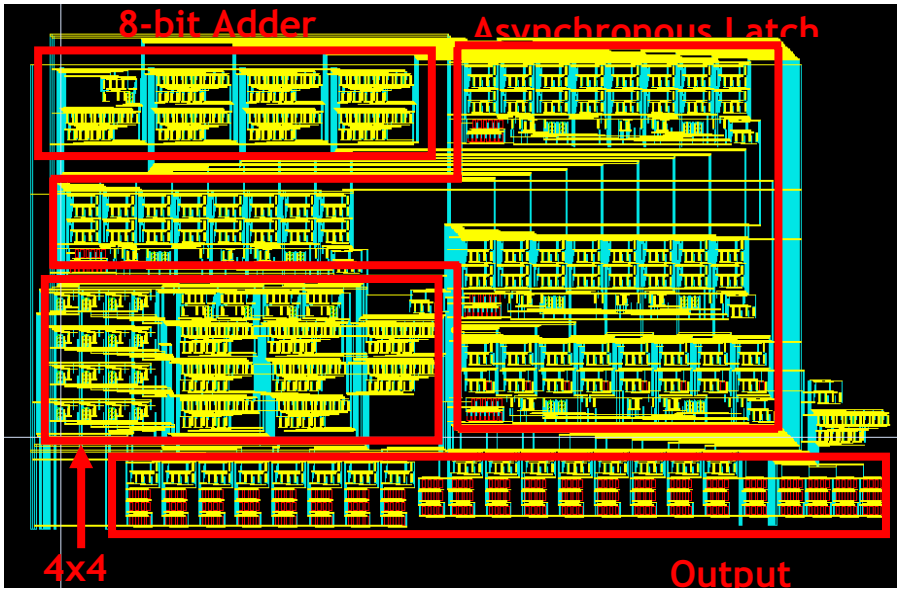


Fig 6: Layout of the asynchronous MAC circuit.

The FIR filter has six taps. We adopt the fixed coefficient design for simplicity, that is to say, shift operation have replaced the multiplication.

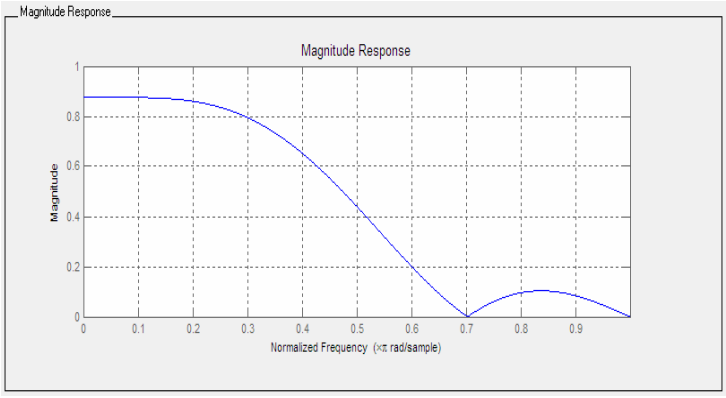


Fig. 7: Frequency response of the FIR filter

Table 1: Coefficient & shift operation

Coefficient	Input data D
-0.062500	-(D >> 4)
0.125000	D >> 3
0.375000	D >> 2 + D >> 3
0.375000	D >> 2 + D >> 3
0.125000	D >> 3
-0.062500	-(D >> 4)

Fig. 8 illustrates the architecture of the asynchronous FIR filter.

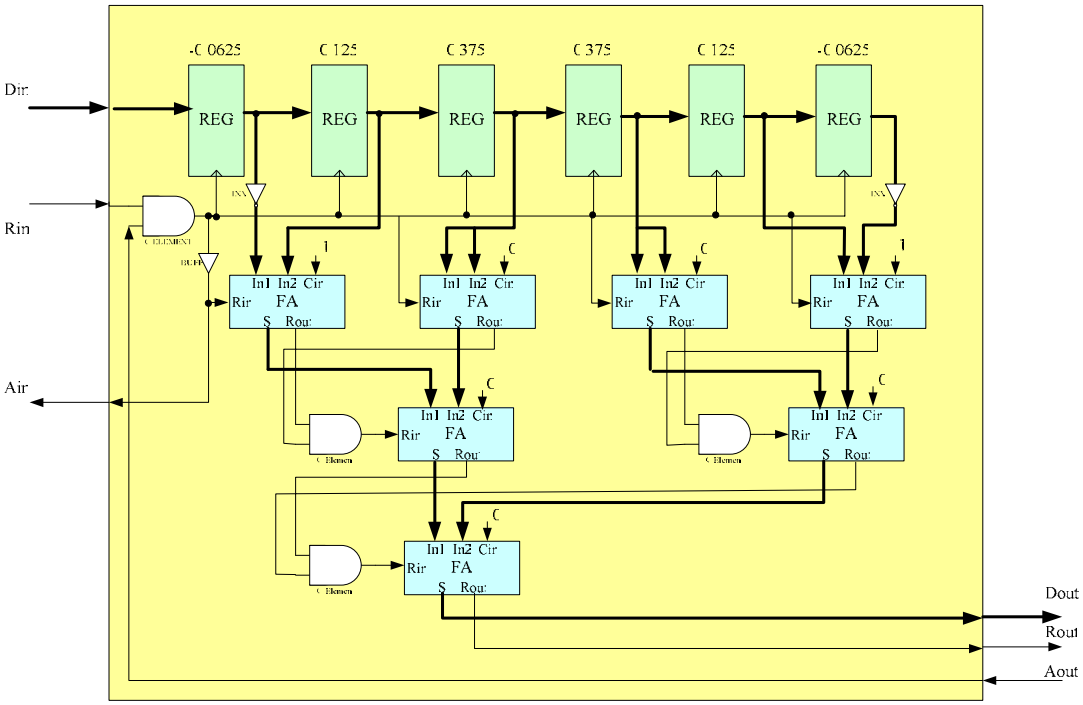


Fig. 8: Asynchronous fixed coefficient FIR filter architecture

Basically, the internal circuit are all combinational circuit, the multiplication and accumulation

operation completed by the shift wire assign and adder tree. We use the 2-bit asynchronous full-adder[3], it is similar to the dynamic logic in the synchronous circuit, only when request is high, the FA can work, or it is always in the pre-charge state. Figure4 is the circuit of a 2-bit full-adder S0-parts. Besides, because of the process only have the NMOS, so all the PMOS for pre-charge are changed to always-on NMOS.

Specifications of the FIR filter:

Item	Specification	measure
Vdd (supply voltage)	10 V	N/A
Propagation delay	2500us → 400Hz	Yes
Transistor count	3315	N/A
Area	1.2mm x 1.0mm	N/A
Pad number	74	N/A

Test consideration：

We design the additional test port, there are each FA output, for one thing, we can know FA works correct or not, on the other hand, we can ensure the asynchronous communication protocol is right.

We also place some test component. If the chip can not work, we can find the solution from these test component :

- Asynchronous 2-bit Full Adder
- Latch based register
- C-element

The layout of 6-tap FIR filter is shown in Fig. 9.

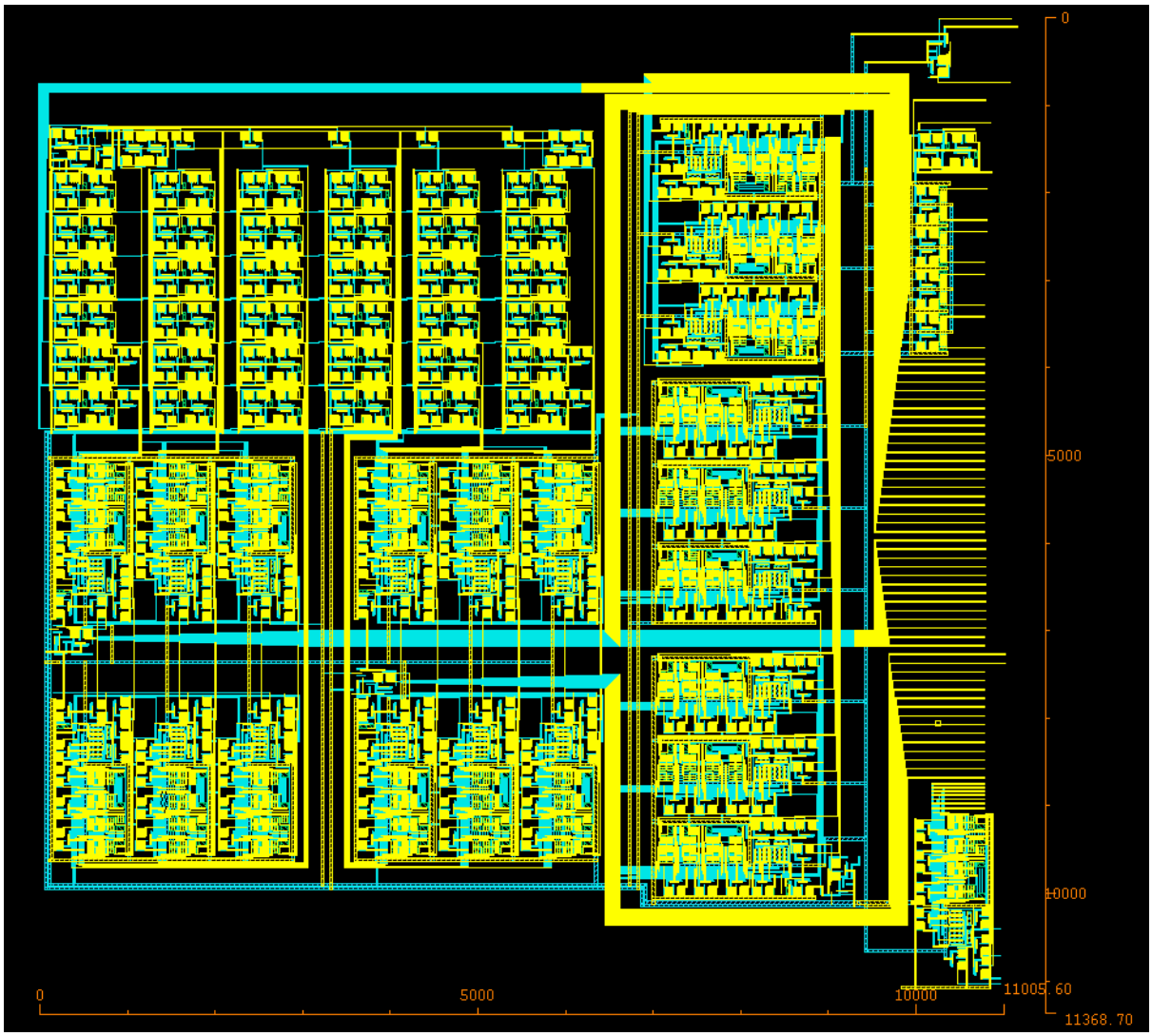


Fig. 9: Layout of the 6-tap FIR filter using asynchronous logic.

四、結論與討論

In this project, we have designed two important signal-processing module using asynchronous design on a a-Si process provided by ITRI. They are a 4x4 MAC circuit and a 6-tap fixed-coefficient FIR filter. We expect to receive the fabricated circuits and have the preliminary test results in September, 2007.

五、參考文獻

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六、計畫成果自評

本計劃於第一年度間主要工作項目為了解製程與其元件特性，於年度結束前二個月，我們已設計完成各種以 TFT 為基礎之 MAC/FIR filter 電路並已下線至工研院，預期將於 3-4 月後可以獲得完成的量測結果。有關研究成果論文則因電路尚待製作與量測，目前正整理研究成果為論文中。