行政院國家科學委員會專題研究計畫 期中進度報告

可應用於軟性電子的TFT電路設計技術之開發--子計畫六：可應用於軟性電子數位電路測試及容錯技術之開發(1/3)

期中進度報告(完整版)

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執 行 期 間 ： 95 年 08 月 01 日至 96 年 07 月 31 日

執 行 單 位 ： 國立臺灣大學電子工程學研究所

計 畫 主 持 人 ： 李建模

報 告 附 件 ： 出席國際會議研究心得報告及發表論文

處 理 方 式 ： 期中報告不提供公開查詢

中 華 民 國 96 年 05 月 25 日

行政院國家科學委員會補助專題研究計畫成果報告

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※ 可應用於軟性電子數位電路測試及容錯技術之開發 ※

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計畫參與人員：鄭啟玄，沈學聰

執行單位：國立臺灣大學電子工程學研究所

中　華　民　國　95 年　5　月　24　日

1. 中文摘要

第一部份為軟性電子製程之自我偵錯設計：四位元全加法器，此偵錯技術主要是為了可撓曲性的軟性電子電路。如果電路中有元件或導線遭受折疊或暫時故障而造成輸出錯誤時，便可以送出訊號告知此電路目前是輸出錯誤的。此技術將有助於大型電路設計的錯誤訊號容錯。第二部份為軟性電子製程之可測試式非同步電路：掃描鏈的設計。雖然非同步電路沒有時脈訊號的控制，但我們依然可以利用非同步電路傳送訊號的原理與特徵，在其中插入掃描鏈來輸入測試訊號與擷取訊號，如此將可提高非同步電路的測試功能。

2. Abstract

In this design there are two function blocks. The First part is an self-testable full adder design in TFT. This technique is designed for flexible characteristics of TFT chip. If the outputs are erroneous due to some folded elements or wire, the designed block can send a signal to notice that the output is error. This technique will be helpful to fault-tolerance in VLSI design. The second part is DFT in asynchronous: scan chain. Although the asynchronous circuit has no clock to control, we can still insert scan chain according to the signal transmitting method. This will enhance testability of asynchronous circuits.

3. Self-testable 4-bit full adder

Full Adder plays an important role in μ-processor and DSP design. The circuits in TFT may have transient or permanent errors due to flexible material. If we know whether the output is erroneous or not, the control unit will be able to manager the errors and let the system work correctly. Then the reliability will be higher.

3-N code algorithm is applied in this technique: multiply the input data by 3 and divide the output data by 3. For example, if an 3+5 operation is required, it can multiply the two inputs by 3 and then adds them. Finally the output will be divided by 3 and the result value is the required output (Figure-1).

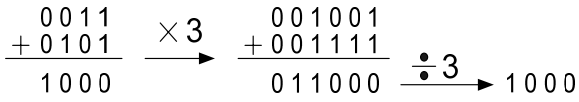

Figure-1：3-N code for “3+5” operation

If there are some faults in the adders or multiplier, remainder will exist after the operation of divider according to the theorem of 3-N code algorithm. Thus the erroneous outputs will be detected (Figure-2).

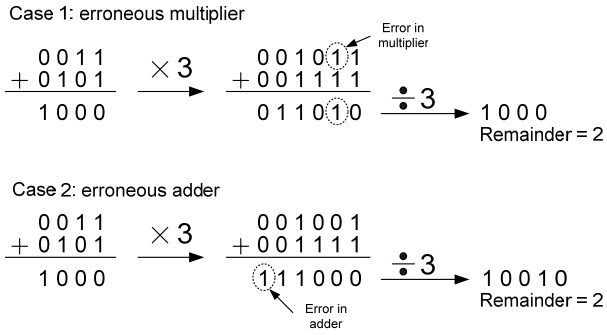

Figure-2：3-N code operation with error bit

In the architecture of the self-testable full adder (Figure-3), PLA design is considered since the number of gates in multiplier and divider is enormous. The difficulties of verification are also considered. The PLA is designed by NOR-NOR logic because there is only NMOS in amorphous silicon (a-Si) process. Thus we use pull-down logic to

design inverter and NOR logic.

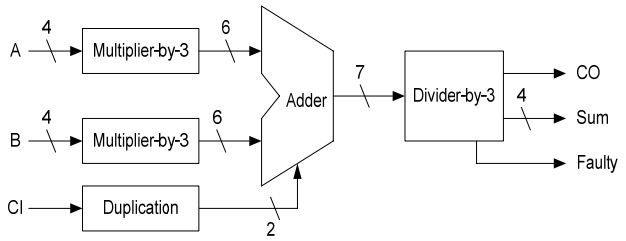

Figure-3：Self-Testable full adder

In the 6-bit full adder of Figure-3, pass-transistor method is considered in one-bit full adder since it conserves power and area, and it doesn't need CMOS technique. Therefore the 6-bit full adder is composed of series 1-bit full adder (Figure-4). Because pass-transistor will degrade V_{OH} for each stage, inverters are inserted between the pass transistors in this design (Figure-5).

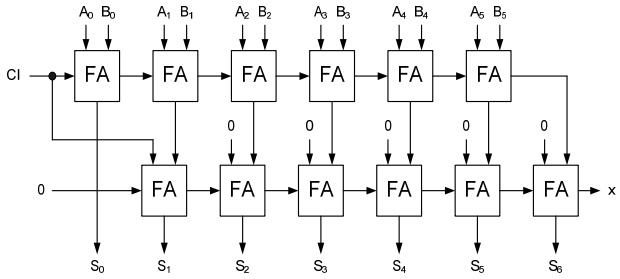

Figure-4：6-bit full adder

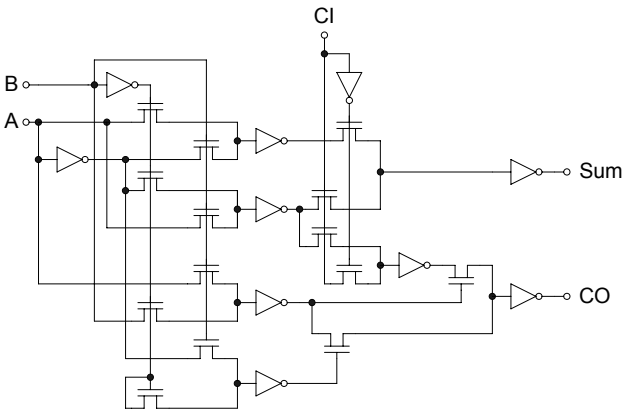

Figure-5：1-bit full adder with pass-transistor

4. Asynchronous circuit in DFT (scan chain)

The scan chain block diagram for four-phase dual-rail asynchronous circuit is shown in Fig.6.

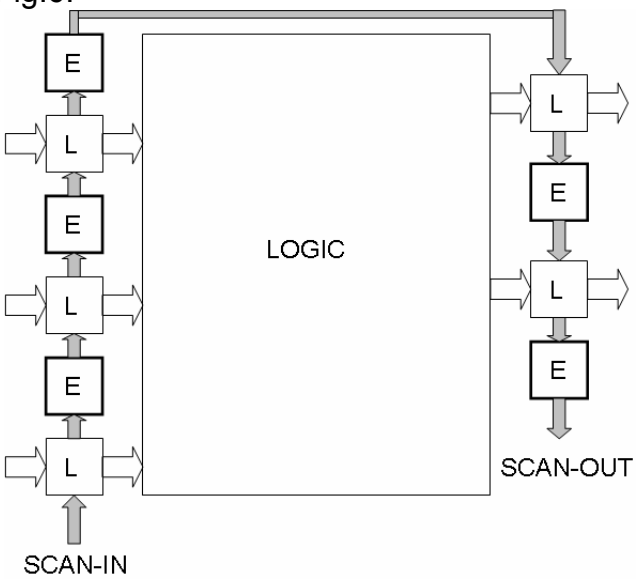

Fig-6

The empty-cells have been inserted between every two latch-cells in the four-phase dual-rail asynchronous circuit. The original latch-cell and a new inserted empty-cell are combined to form one new scan-cell as shown in Fig.7. All scan-cells are serial connected as a scan chain.

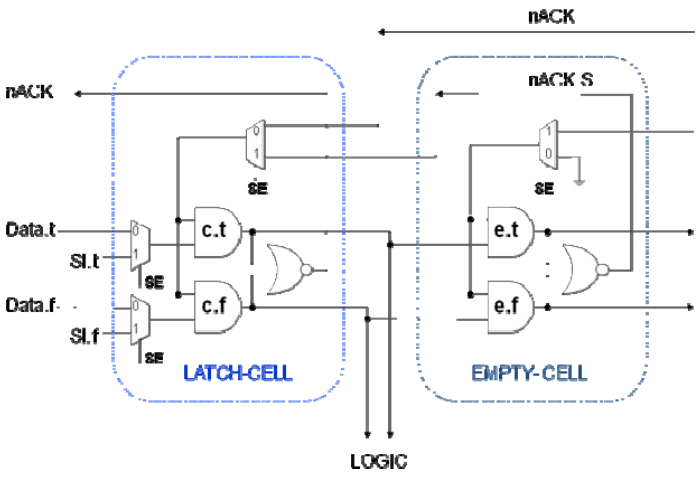

Figure-7

In normal operation mode (SE=0), the control signals between latch-cell and empty-cell are opened by multiplexer and the values contain in empty-cells are locked to “empty” (e.t=e.f=0).

In test mode (SE=1), the control signals between latch-cell and empty-cell are connected. The Fig.8 shows the equivalent circuit of scan-cell under test mode.

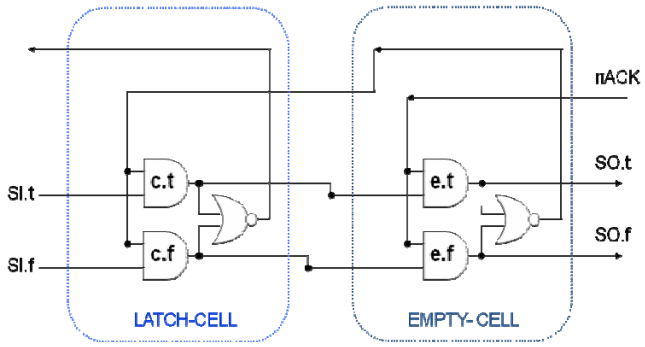

Fig.8

5. Simulation results

In this paragraph the SPICE simulated results in each block will be shown: 1-bit full adder, self-testable 4-bit full adder and asynchronous scan chain.

(1) 1-bit full adder

The test patterns are {A,B,CI} = 000~111. The simulation result is in Figure-9.

(2) Self-testable 4-bit full adder

The simulations take two parts: the first is a fault-free simulation (Figure-10). This can expect the operation time of this circuit. The test patterns are {A[3:0],B[3:0],CI} = {[1100],[0110],1},{[0011],[1011],0},{[1111],[0001],0},{[1101],[1111],1},{[0110],[0100],0}. The frequency of these patterns is 2kHz. From the result we can expect the operation time of this circuit is 200us~400us.

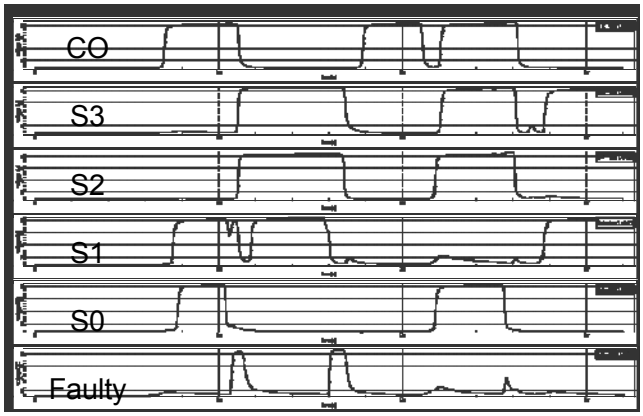

Figure-9：Self-testable full adder fault-free simulation

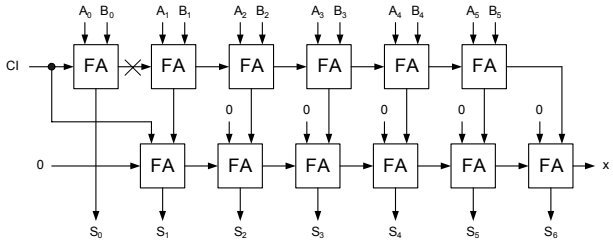

Figure-10：One condition of fault site

The second part is a fault simulation: one fault exists in the 6-bit full adder. The site of error is random chosen to open the wire (Figure-10). This method can simulate the condition of folded circuit in the real world. The test patterns are the same as part 1 and the simulated result is in Figure-11. And the faulty signal tells us that the output {CO,S3,S2,S1,S0} is erroneous if faulty = 1.

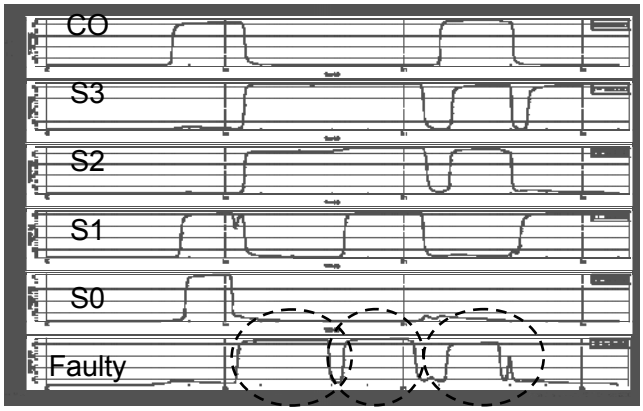

Figure-11：Self-testable full adder in fault simulation

(3) Asynchronous scan chain

In test mode, the scan-cell is able to shift the test vector bit by bit. The test vectors for four-phase dual-rail asynchronous circuit should insert “EMPTY” bit between every non-empty bit.

In Fig.12, the test vector : EMPTY(SI.t=0, SI.f=0), TRUE(SI.t=1, SI.f=0), EMPTY(SI.t=0, SI.f=0), and False(SI.t=0, SI.f=1) are shifted from SI to the SO sequentially.

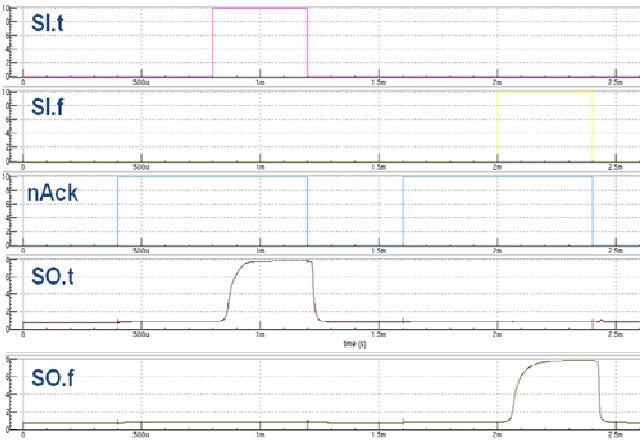

Fig.12

6. Floorplan and layout view

Figure-13 is the floorplan of this chip.

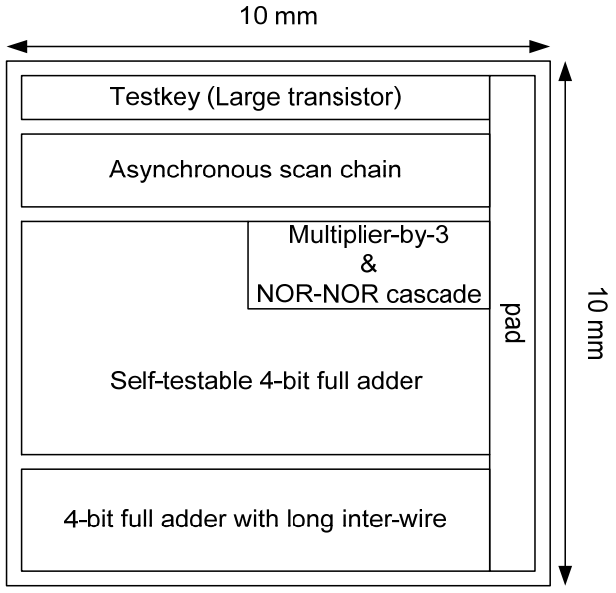

Figure-13 Floorplan of the full circuit

The special blocks are Testkey and 4-bit full-adder with long inter-wire. Testkey (large transistor) is designed for measurement of destructed NMOS. This will be helpful to expect the folded element in TFT.

Full adder with long inter-wire is designed to measure its delay behavior. Because TFT has a special characteristic of large area, the measurement will be a good reference in TFT circuit delay expectation.

Figure-14 is the total layout view.

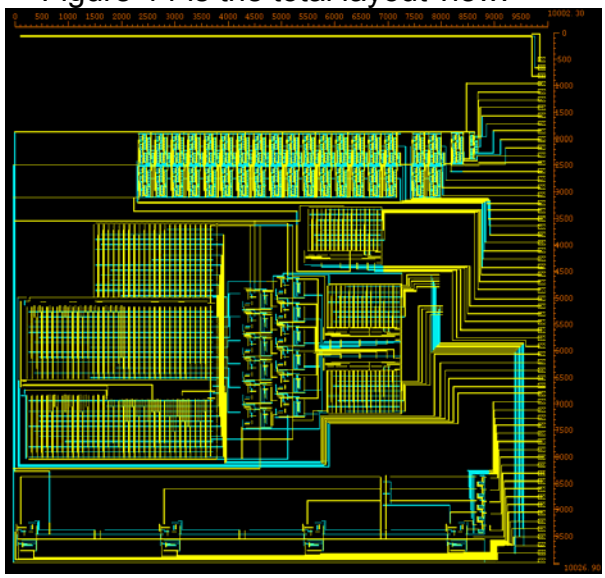

Figure-14 Layout view of full circuit

7. Reference

1. [Avizienis 71] Avizienis, A “Arithmetic error codes: Cost and effectiveness studies for application in digital system design,” *IEEE Transactions on Computers*, Vol. C-20, No. 11, November 1971, pp. 1322-1331.

2. [Johnson 89] B. W. Johnson, *Design and Analysis of fault-tolerant Digital Systems*, Addison-Wesely, 1989.

3. [Sparsø 01] J. Sparsø and S. Furber Principles of Asynchronous Circuit Design ~ A Systems Perspective, Kluwer, 2001.

出席國際學術會議心得報告

計畫編號	NSC 95-2220-E-002-022
計畫名稱	可應用於軟性電子的 TFT 電路設計技術之開發--子計畫六：可應用於軟性電子數位電路測試及容錯技術之開發(1/3)
出國人員姓名 服務機關及職稱	台大電子所 李建模
會議時間地點	May6-10, 2007
會議名稱	VLSI Test Symposium 2007
發表論文題目	

一、參加會議經過

二、與會心得

In nano-meter technology, IC diagnosis has become one of the most important topics. There are two sessions in the VTS this year.

Also, small delay testing is gaining importance and many people are trying to find test solutions.

Low power testing, on the other hand, has gradually phased out and no more paper this year.

Test compaction is still one of the important topics to watch.

SOC testing has been gradually slow down and no very new research.