A 1.5-V 10-ppm/°C 2nd-Order Curvature-Compensated CMOS Bandgap Reference with Trimming

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***Abstract*—A 2nd-order curvature-compensated CMOS bandgap reference circuit with a novel trimming technique is described. The 2nd-order curvature compensation is implemented by using a temperature-dependent resistor ratio generated by a poly resistor and a diffusion resistor. A trimming technique with digital switches is utilized to increase or decrease resistance bi-directionally and therefore to minimize the variance of resistance. The proposed voltage reference operates down to a 1.5 V supply and consumes a maximum supply current of 55 μA. The experimental prototype circuit in a standard 0.35-μm CMOS process achieves a temperature coefficient of 10 ppm/ °C and occupies an area of 0.71 mm².**

Keyword: CMOS bandgap reference, curvature compensation, trimming, low voltage.

I. INTRODUCTION

A precision voltage reference is always essential in many applications such as data and power converters. To achieve a precision voltage over a wide range of temperature, the bandgap circuit is most frequently adopted. In CMOS technology, a parasitic vertical bipolar junction transistor (BJT) formed in p- or n-wells is usually used to implement the bandgap circuit [1]. The emitter-base voltage of the parasitic vertical BJT has a negative temperature coefficient. By compensating the temperature characteristics of the emitter-base voltage, bandgap references can work over a broad range of temperature. High-order compensation is generally utilized to obtain a low temperature coefficient [1]-[3]. A 2nd-order temperature-compensated bandgap reference based on a temperature-dependent resistor ratio scheme [3] is presented in this paper. The two different positive-temperature-coefficient resistors, poly resistor and diffusion resistor, in CMOS process are used to implement the temperature-dependent resistor ratio. A new trimming method is further utilized to prevent resistor ratio values from process deviation without any expensive trimming setup.

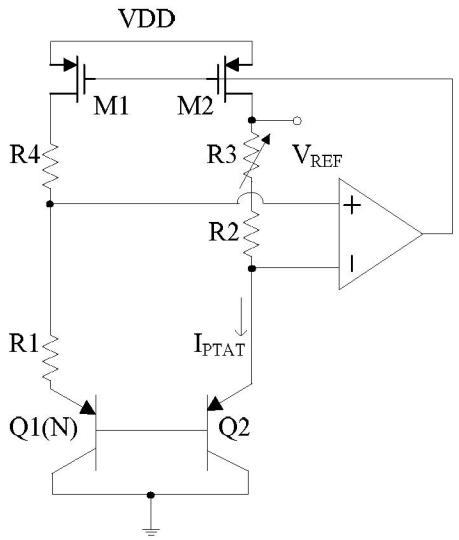

Fig. 1. Architecture of the CMOS bandgap reference.

In recent years, demands for low-voltage bandgap reference circuits have increased enormously due to widespread applications of portable electronic appliances. Bandgap voltage reference works use either resistive subdivision or low threshold voltage devices to overcome the low supply voltage issue [4], [5]. To operate under a low voltage environment, the restraint of opamp is significant and should be considered. A pre-amplifier stage is utilized in the opamp design to lower the limitation of supply voltage in this design. It could be operated with a supply voltage down to 1.5 V.

In Section II, a brief analysis of the bandgap architecture is introduced. The proposed trimming technique is explained in Section III. The measured results are presented in Section IV.

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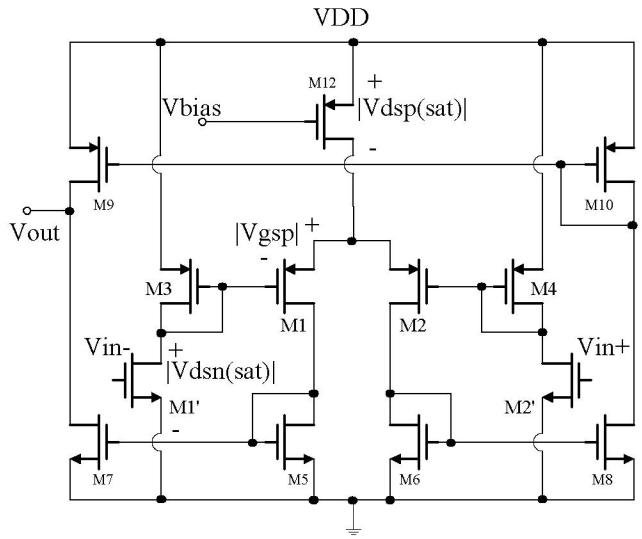

Fig. 2. Opamp with a pre-amplifier input stage.

II. BANDGAP REFERENCE

A. Curvature-Compensated CMOS Bandgap Reference

The architecture of the bandgap reference circuit is illustrated in Fig. 1. By compensating the emitter-base voltage of Q2, a stable voltage reference over a wide range of temperature could be generated. A current proportional to absolute temperature, I_{PTAT}, is produced and used to compensate the negative temperature coefficient of the emitter-base voltage through the negative feedback effect of the opamp. I_{PTAT} can be presented as

$$I_{PTAT} = \frac{1}{R_1} \cdot \ln(N) \cdot \frac{k \cdot T}{q} \tag{1}$$

where k is the Boltzmann's constant, q is the charge of an electron, and N is the emitter-area ratio of Q1 and Q2. The two different resistors are both with positive temperature coefficients. R1, R2, and R4 are poly resistors while R3 is a P+ diffusion resistor. When I_{PTAT} passes through two resistors of different materials, R2 and R3, the reference voltage, V_{REF}, can be derived by

$$V_{REF} = V_{EB2} + \left[\frac{R_2}{R_1} + \frac{R_3(T_o)}{R_1(T_o)}\right] \cdot \ln(N) \cdot \frac{k \cdot T}{q} + \frac{R_3(T_o)}{R_1(T_o)} \cdot (K_{pdiff} - K_{poly}) \cdot \ln(N) \cdot \frac{k \cdot T}{q} \cdot (T - T_o) \tag{2}$$

where V_{EB2} the emitter-base voltage of Q2, T_o is the reference temperature, K_{poly} is the temperature coefficient of poly resistor, and K_{pdiff} is the temperature coefficient of P+ diffusion resistor. Due to the temperature coefficient difference between the two resistors of different materials, a 2nd -order temperature compensation of the bandgap reference can be achieved.

B. Low Voltage Opamp Design

The minimum supply voltage is limited by the two factors [4]. The 1st factor is the reference voltage around 1.25 V. As shown in Fig. 1, the supply voltage is limited by

$$VDD > V_{REF} + |Vdsp(sat)|. \tag{3}$$

The 2nd factor is low-voltage design of I_{PTAT} generation loop limited by the common-collector structure of the parasitic vertical BJT and the input common-mode voltage of the opamp. The opamp is therefore designed with an nMOS pre-amplifier input stage (M1', M2', M3 and M4) followed by a pMOS differential-pair stage (M1 and M2) for low-voltage operation of the bandgap circuit. It is illustrated in Fig. 2. The lower limitation of supply voltage can be expressed as

$$VDD > Vdsn(sat) + |Vgsp| + |Vdsp(sat)|. \tag{4}$$

VDD is allowed to go under 1.5 V with proper design.

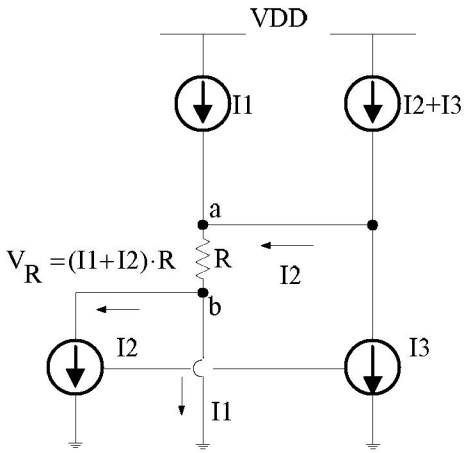

Fig. 3. Conceptual operation of trimming for increasing R.

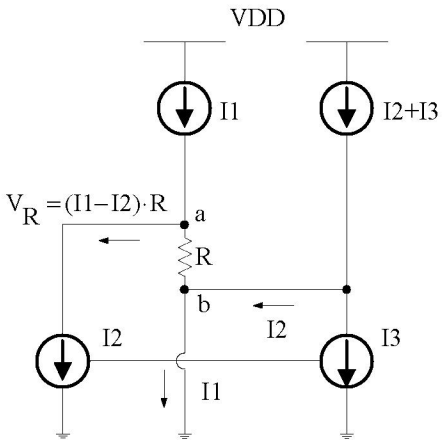

Fig. 4. Conceptual operation of trimming for decreasing R.

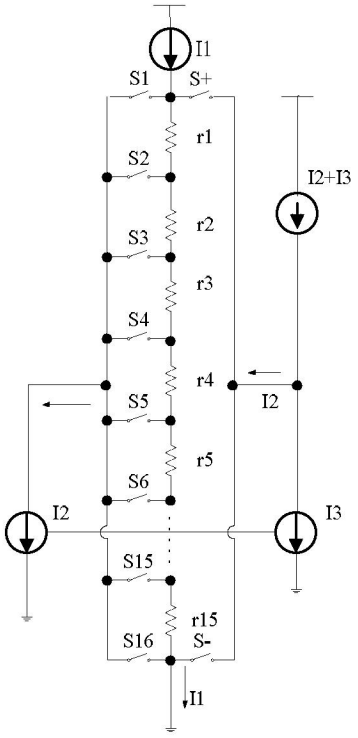

Fig. 5. Implementation of the trimmed resistor R3

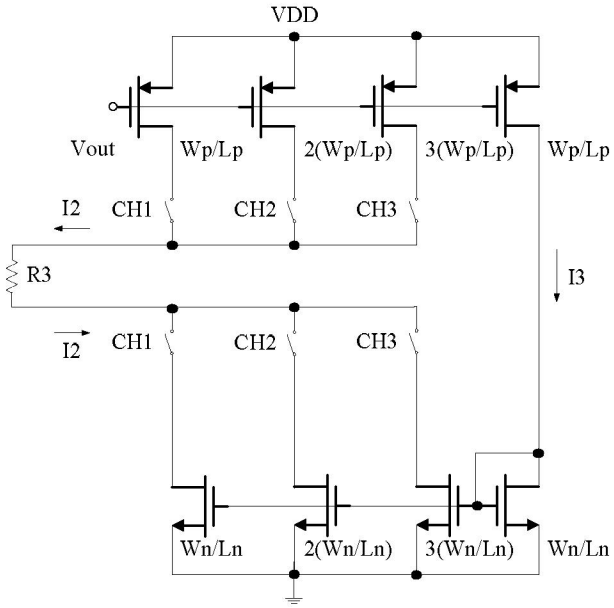

Fig. 6. Implementation of the trimmed current I2.

III. TRIMMING TECHNIQUE

Based on equation (2), the accuracy of the ratios of R2/R1+ $R3(T_o)/R1(T_o)$ and $R3(T_o)/R1(T_o)$ is the most important factor in deciding the effect of compensation and therefore the performance of the bandgap reference. In order to ensure the two ratios are correct, a new trimming technique is proposed. Instead of conventional resistor trimming, e.g. laser cut, to adjust the voltage across the trimmed resistor, currents over the resistors are controlled by switches to obtain the same effect. Only the resistor, R3, that involves in both coefficients of the 1st-order and the 2nd-order terms is trimmed in our design.

A. Principles of the Trimming Method

As shown in Fig. 3, R is the resistor to be trimmed and there is a current I1 (i.e. I_{PTAT} in our design), flowing through it originally. When trimming occurs by controlling digital switches, an extra current I2 is added into this resistor segment. Therefore, the voltage across R changes from R·I1 to R·(I1+I2), namely, a resistance value of R·I2/I1 is added. In addition, a current mirror must be used to make I2 leave the path after flowing through R to ensure the extra current could only affect the "trimmed" resistor R.

When decrease on resistance is required, instead of adding current I2 on the resistor R, current should be subtracted. Current subtraction can be implemented by reversing the current direction of I2 between nodes a and b as shown in Fig. 4. The current passing through R would be decreased from I1 to I1-I2. Hence the resistance value of the "trimmed" resistor R is subtracted by R·I2/I1.

B. Implementations of Trimmed Resistor and Current

The two factors that affect the accuracy of the trimming technique are the trimmed resistance and the extra current through the segment. There are two methods that are implemented to control the efficiency of these two factors in our design.

In order to increase the precision of the trimming technique on resistance, R3 is practically divided into 15 small segments with 16 switches, S1 to S16, as illustrated in Fig. 5. Only one switch would be turned on among these 16 switches whenever trimming is applied. Comparing with one resistor segment only, the precision can be enhanced by 15 times. The switches S+ and S- are used to control whether the resistance is required to be increased or decreased.

To expand the viability and precision of the extra current I2, I2 is practically composed of three channels of currents controlled by current mirrors with the ratio 1:2:3 as shown in Fig. 6. Using the output, Vout, of the opamp to bias the mirrored transistors and setting switches CH1, CH2, and CH3 to control each channel, a combination of currents from one-unit current to six-unit current can be realized.

If the unit extra current is i and each small segment has resistance r, the available trimming range could vary from +90 i·r to -90 i·r by using the two methods described above. The total trimmed resistor is a fraction of R3; while the total trimmed current is a fraction of I_{PTAT} because the output of

the opamp is used to mirror the trimmed transistors. After trimming, the reference voltage, V_{REF}, would become

$$V_{REF} = V_{EB2} + \left[\frac{R_2}{R_1} + \frac{R_3(T_o)}{R_1(T_o)} \cdot (1 + \alpha \cdot \beta)\right] \cdot \ln(N) \cdot \frac{k \cdot T}{q} + \frac{R_3(T_o)}{R_1(T_o)} \cdot (1 + \alpha \cdot \beta) \cdot (K_{pdiff} - K_{poly}) \cdot \ln(N) \cdot \frac{k \cdot T}{q} \cdot (T - T_o) \quad (3)$$

where α and β represent the trimmed fractions of R3 and I_{PTAT}, respectively.

IV. MEASUREMENT RESULTS

The proposed bandgap reference circuit in Fig. 1 with trimming techniques mentioned above is implemented in 0.35-μm CMOS technology. The chip micrograph is shown in Fig. 7 with an area of 0.71 mm^2. The measured results are illustrated in Table I.

Fig. 8 shows the temperature dependence of the reference voltage with supply voltage of 1.5 V. When operated without trimming, the measured temperature coefficient is 63 ppm/ °C and the reference voltage is 1.112 V. After trimming, the measured temperature coefficient goes down to 10 ppm/ °C. The supply current is 55 μA.

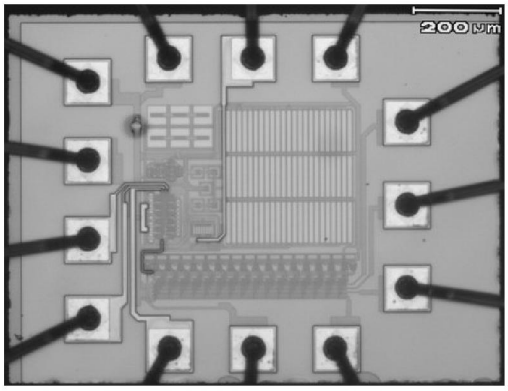

Fig. 7. Chip micrograph of the bandgap voltage reference

Table I. Summary of the measured results

Technology	CMOS 0.35-μm
Supply voltage	1.5 V
Reference voltage	1.112 V
Temperature coefficient	10 ppm/ °C
Chip area	0.71 mm^2
Supply current	55 μA

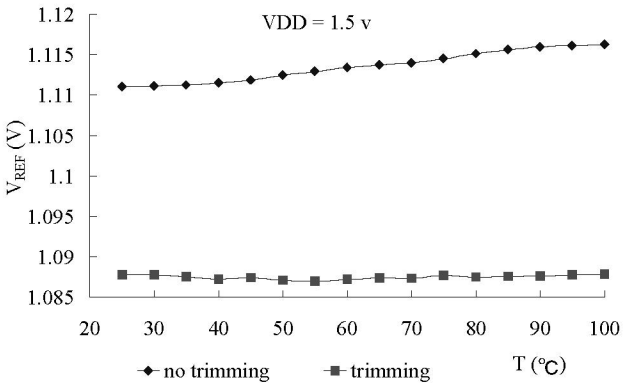

Fig. 8. Measured temperature dependence with VDD = 1.5 V

V. CONCLUSION

A low-voltage 2nd -order curvature-compensated bandgap circuit with a new trimming technique is proposed with a performance of 10 ppm/ °C at supply voltage 1.5 V. The technique makes the chip adjustable and each state can be restored by the respective digital input. With the trimming mechanism on resistances, a mismatch on resistance in process can be effectively corrected and therefore benefit the performance of a curvature-compensated bandgap reference circuit enormously.

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