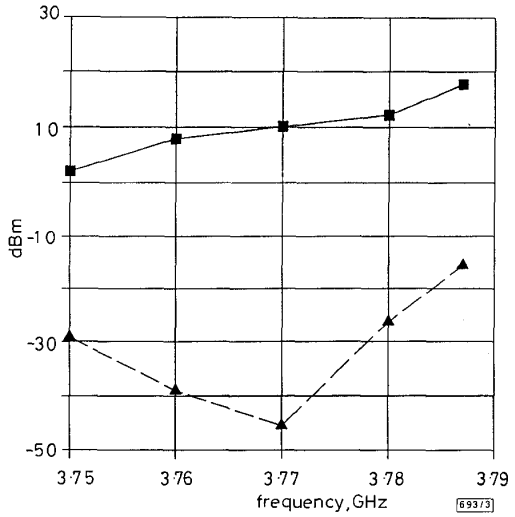

Fig. 3 *Array output power and transmit-recieve feedthrough signal*

■ array output power
▲ TX-RX feedthrough signal

oscillator output varies from 2.1dBm (1.62mW) at 3.75GHz to 17.7dBm (58.9mW) at 3.787GHz. The DC to RF efficiency varies from 1.5% at 3.75GHz to 21.4% at 3.787GHz. The isolation signal has a minimum at 3.77GHz of –45.5dBm, this is equivalent to 55.7dB isotation. The isolation is better than 30dB across the whole band and this could be improved by using broadband constant phase shift networks, such as Schiffman phase shifters.

Conclusion: A novel simultaneous transmit-receive active array has been described using dual linear polarisation and sequential rotation to achieve very high values of transmit-recieve isolation. The sequential rotation technique, while leading to increased isolation, has been found to require very repeatable active patches and this can be difficult to achieve in practice. A best case transmit-receive isolation of 55dB has been obtained with an array output power of 10dBm. These results show the possibility of using larger arrays of this type in the microwave or millimetric bands for short range communication or radar systems.

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5V, 8 bit, 100MS/s fully differential CMOS sample-and-hold amplifier

Chun-Chieh Chen and Hen-Wai Tsao

Indexing terms: Sample and hold circuits, CMOS integrated circuits, Amplifiers

A 5V, 100MS/s fully differential CMOS sample-and-hold amplifier (SHA) with 8 bit accuracy is proposed. Based on the stability limitations of closed-loop SHAs studied in a previous Letter (1995), the proposed SHA is implemented by an open-loop structure using the 'gain-enhanced unity-gain amplifier' to avoid the stability problem and achieve higher operation speed. Simulation results which agree well with experimental results have been obtained to demonstrate the accuracy of the proposed circuit.

Introduction: With the proliferation of digital signal processing, greater demands are placed on A/D converters. Meanwhile, the sample-and-hold amplifier (SHA), a circuit which often precedes A/D converters to reduce the distortion due to nonlinear junction capacitance and errors resulting from clock and input propagation delay mismatch, has also received more and more attention.

In the literature, monolithic sample-and-hold amplifiers have been demonstrated to operate up to 100MHz using either bipolar or BiCMOS technology [1, 2], but the sampling rate achievable with CMOS has been limited to 50MHz [3, 4]. Today, when CMOS is still the major part of semiconductor's production, it is our goal in this Letter to use the CMOS process to design a faster sample-and-hold amplifier.

In this Letter we design a fully differential CMOS SHA based on the fully differential 'gain-enhanced unity-gain amplifier'. The simulated and measured performance of the proposed circuit are also presented.

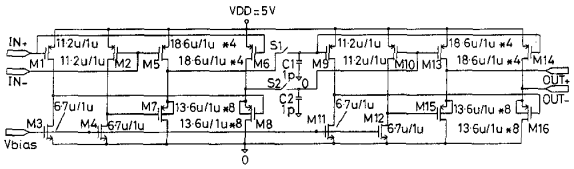

Fig. 1 *Gain enhanced unity gain amplifier based fully differential sample-and-hold amplifier circuit*

Fully differential CMOS sample/hold amplifier: Due to many limitations caused by the stability of a closed-loop SHA [5], we are urged to change our focus again to open-loop SHA. However to overcome the unavoidable clock-feedthrough problem in an open-loop SHA, we adopted the fully differential structure to eliminate the clock-feedthrough errors. At the same time, to keep the operation speed of the proposed SHA as high as possible, we employ the 'gain-enhanced unity-gain amplifier' to replace the conventional op-amp-based unity-gain buffer. The circuit we designed and the correspondmg device aspect ratios and multipliers are shown as Fig. 1, where M1 ~ M8, M9 ~ M16 construct the front-stage and the post-stage 'gain-enhanced unity-gain amplifier' without the need for common-mode feedback circuits. Using the small signal analysis, we can derive the differential-mode gain of the amplifier as:

$$A_d = -\frac{g_{mi} + A_{d(sub)} \bullet g_{ml}}{g_{ml} + g_{dl} + g_{di}} \qquad (1)$$

where $g_{ml}(g_{mi})$ is the transconductance of the load devices M7, M8, M15, M16 (input devices M5, M6, M13, M14) and $g_{dl}(g_{di})$ is the output conductance of the load (input) device. The term $A_{d(sub)} \bullet g_{ml}$ called the 'gain-enhancing' factor, is derived from the sub amplifier formed by M1 ~ M4 (M9 ~ M12) and $A_{d(sub)}$, the differential-mode gain of the sub amplifier, which can be expressed as follows:

$$A_{d(sub)} = \frac{g_{mi(sub)}}{g_{di(sub)} + g_{dl(sub)}} \qquad (2)$$

From the above equation, it is obvious that the differential-mode gain can be easily tuned to unity by adjusting the bias

voltage V_{bias}. That is the reason why we call it the 'gain-enhanced unity-gain amplifier'.

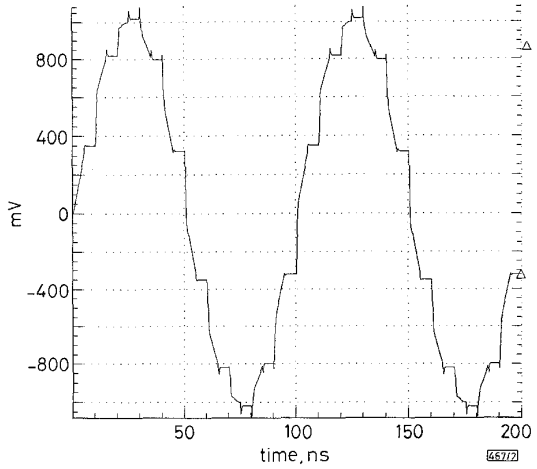

Fig. 2 *Simulated output waveform of SHA*

Table 1

Technology	0.8μm, *N*-well, DPDM
Power supply	5V
Overall bandwidth (C_H = 1pF)	304MHz
Gain error ($2V_{p-p}$, 10MHz input)	0.07%
THD ($2V_{p-p}$, 10MHz input)	0.22%
Tracking mode settling (0.1% of 1V step)	3.7ns
Hold mode settling (1mV within final value)	0.7ns
Pedestal ($2V_{p-p}$, 10MHz input, 100MHz clock rate)	<8mV
SNR ($2V_{p-p}$, 10MHz fully differential input, fully differential output, 100MHz clock rate)	50.2dB (>8bits)
SNR ($1V_{p-p}$, 10MHz input, 100MHz clock rate, single-ended)	27.44dB (simulated) 27.21dB (measured)
Droop rate	0.7mV/μs
Power consumption	53mW

Sample-and-hold amplifier performance results: To demonstrate the performance of our proposed circuit, the fully differential CMOS SHA shown in Fig. 1 is simulated by HSPICE using 0.8μm *N*-well, DPDM CMOS process parameters with a single 5V power supply. The bias voltage V_{bias} is 3.5V. The simulation results for a 10MHz sinusoidal input and 100MHz sampling clock rate are listed in Table 1 and the waveforms are shown in Fig. 2. The microphotograph of the proposed SHA circuit is shown in Fig. 3. The measured single-ended signal/noise ratio (SNR) for a 10MHz sinusoidal input and 100MHz sampling clock rate is 27.21dB, which agrees well with the simulated results (27.44dB).

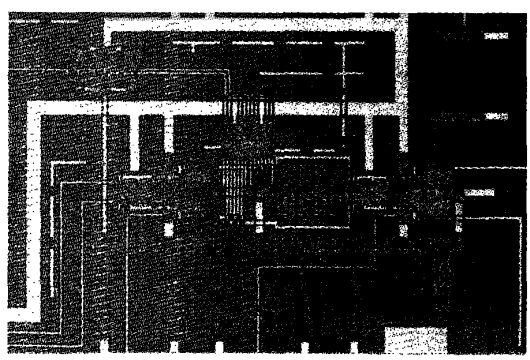

Fig. 3 *Microphotograph of SHA*

Conclusion: A 'gain-enhanced unity-gain amplifier'-based open-loop fully-differential CMOS sample-and-hold amplifier has been presented. It avoids the stability problem caused by the closed-loop structure and achieves a sampling rate and an accuracy of 100MS/s and 8bit, respectively. It is particularly useful in high-speed data acquisition systems implemented using the most popular CMOS process.

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Average modelling and simulation of series-parallel resonant converters by PSPICE compatible behavioural dependent sources

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Indexing terms: Resonant power converters, Modelling, Simulation, Power electronics

A new methodology for developing average models of resonant converters is presented and verified against cycle by cycle simulation, showing excellent agreement. The proposed modelling approach applies the concept of $R_{ac}(t)$, which represents the instantaneous effective load of the resonant network. The model can be used as it is to run steady-state (DC), large signal (transient) and small signal (AC) simulations.

Introduction: A prerequisite for a solid engineering design of resonant converters [1 – 3] is a good model that describes their operation in the time as well as in the frequency domain. Two basic approaches have been used hitherto to develop such models. One approach applies analytical relationships to derive the expressions that describe the behaviour of a given converter in the various domains [4]. A second approach developed by Steigerwald [5] uses the first harmonics approximation and the R_{ac} concept. By this, the converter is described as a simple resonant network with a load-dependent damping (or quality) factor which can then be examined by basic (steady-state) network equations. The limitation of the second approach is the difficulty of applying it to more than just the steady-state (DC) voltage ratio relationships. In this study we overcome this deficiency of the R_{ac} approach by extending the behavioural modelling methodology [6] to resonant converters. The advantage of the average models derived by the proposed high level presentation is their ability to emulate the DC, large signal and small signal responses of the corresponding switch mode or resonant system. Once derived, the models can be run as they are on practically any modern circuit simulation package to obtain open- or closed-loop responses in the time and/or frequency domain. The fundamental ideas of the proposed approach are exemplified by developing the behavioural model of a series-parallel resonant converter and verifying the validity of the model against cycle by cycle simulation.