A 10GBASE-LX4 RECEIVER FRONT END TRANSIMPEDANCE AMPLIFIER AND LIMITING AMPLIFIER

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ABSTRACT

A 10 Gbase-LX4 receiver front end including an inductor feedback transimpedance amplifier and a modified Cherry-Hooper cell limiting amplifier realized in a 0.18μm CMOS process is described. The receiver front end covers 34.8 dB input dynamic range and provides 66 dBΩ differential gain with 1.7 GHz bandwidth. All the building blocks achieve a high data rate with low power dissipation. The receiver front end can meet the BER requirement under all corner simulations with 113 ps(pp) data jitter at 3.125 Gb/s. The chip area is 1.1 x 2.2 mm^2 and consumes 54mW using 1.8 V supply voltage. The overall performance is verified by the measured results.

1. INTRODUCTION

The demand for large services and increased information, together with the trends of low power, low cost from the market, have accelerated the development of telecommunications which has resulted in the 10 Gigabit Ethernet standard for optical communication. Benefiting from the properties such as high integration, low cost and low power, the scaled CMOS technology is a potential solution for implementing high-speed communication systems that employ parallelism. Key building blocks in this high capacity network consist of a multiplexer (MUX), a retiming flip-flop, and a laser driver in the transmitter and a transimpedance amplifier, a limiting amplifier, a clock and data recovery and a demultiplexer as shown in the receiver. (Fig. 1.) At the receiving end, the signal current is converted into voltage by a low noise, high-speed transimpedance amplifier (TIA). Due to the large input capacitance from the photodiode, the transimpedance amplifier must deal with a wide dynamic input signal current and convert it to a voltage signal with a low contamination from self-noise. The limiting amplifier (LA) is essentially a high speed and high sensitivity hard limiter that quantizes the analog signal coming from the transimpedance amplifier. In general, the TIA is a linear circuit with its output carrying both the signal and noise of the detection subsystem.

Consequently, a decision circuit is therefore needed to regenerate a well-defined digital ones or zeros binary data stream. For a limiting amplifier, the signal is quantized and the output from the limiting amplifier is always at a well-defined level. When designing a transimpedance amplifier, the noise, group delay variation and bandwidth are always practical design issues. And as to the limiting amplifier, bandwidth, input sensitivity, and AM to PM noise also affect the overall system bit error rate (BER) and the data jitter which are associated with the clock and data recovery (CDR).

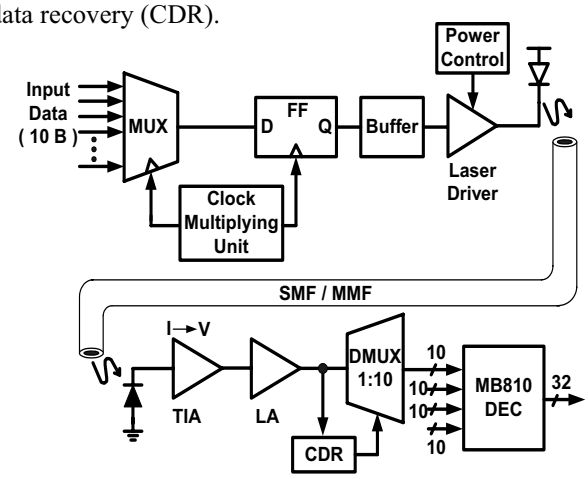

Fig. 1. Fibre optical transceiver

When designing the circuit near the limitation of the given technology, some circuit techniques such as active peaking [1] [2], zero peaking [3] Cherry-Hooper [4], and ft-doubler[5] can be used to enhance circuit performances. In addition to the circuit techniques, a huge power can also achieve a high data rate operation due to the property of maximum oscillation frequency (f_{MAX}) for a given technology. In this paper, we describe the design, and successful test of the front-end chip for 10GBase–LX4 receiver using CMOS 0.18μm process. This paper is organized as follows. In Section 2, the design of

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transimpedance amplifier is discussed. The proposed gain cell for the limiting amplifier is depicted in Section 3. Lastly, in Section 4, experimental results under on-wafer and board conditions are presented. Finally, a conclusion is drawn in Section 5.

2. CIRCUIT DESIGN OF TIA

The TIA in front of the receiver dominants the overall system noise performance and suffers from the large capacitance at the interface between electrical and optical signals. The inductor feedback architecture of the TIA is shown in Fig. 2(a). The equivalent small signal model of TIA is shown in Fig. 2(b), and we can derive the transfer function as:

$$Z_{TIA} \approx \frac{Gm(R+SL)}{S^3C_L CinL + S^2C_L CinR + S(C_L + Cin) + Gm} \quad (1)$$

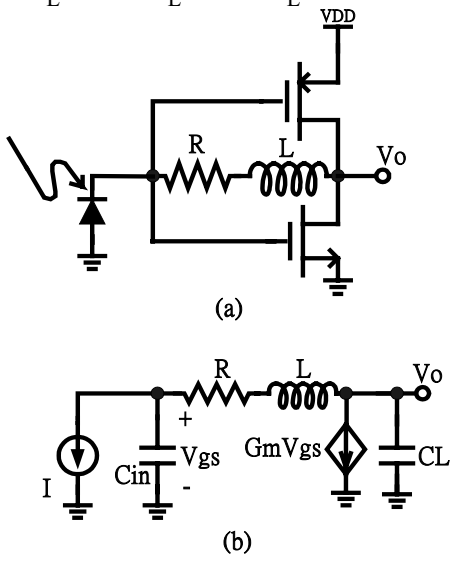

Fig. 2. (a) Transimpedance amplifier
(b) Small signal model

From equation 1, the added zero from the feedback inductor can reduce the parasitic effect between the TIA and limiting amplifier. The value of inductor is chosen such that it provides enough gain peaking and does not create a large phase distortion for the received data. The single ended output is converted to differential ones by a wide band buffer and the DC extracting RC network is implemented by the MOS in deep n-well. The RC network must maintain similar behavior under the system dynamic range. The transimpedance gain is 56 dBΩ under 0.5 pF photodiode capacitor, and bandwidth is about 0.7 times data rate. The overall power dissipation under 1.8 V power supply is 10 mW.

3. CIRCUIT DESIGN OF LIMITING AMPLIFIER

The limiting amplifier usually deals with the wide dynamic range signal and saturates it to a detectable level for the data recovery. The sensitivity of the LA is nearly twelve times the input rms noise voltage and has an influence on the system BER. When designing the limiting amplifier, the number of gain cells must be determined firstly. Assume that As and wp1 in Eq. (2) represent the gain and -3dB cut-off frequency of each gain cell respectively, and the second pole -3dB cut-off frequency, wp2, is added to model the transfer function as:

$$A_T(s) = \left[\frac{As}{(1+\frac{s}{wp1})(1+\frac{s}{wp2})}\right]^N \quad (2)$$

where N is the number of stage in LA. The overall gain can be expressed as：

$$A_t = (As)^N \quad (3)$$

and the bandwidth of the LA can be shown as：

$$\sqrt{(1+(\frac{f_{3dB}}{fp1})^2)(1+(\frac{f_{3dB}}{fp2})^2)} = 2^{\frac{1}{2N}} \quad (4)$$

Assume the second pole, fp2, is m times of the first pole, fp1, namely fp2 = m fp1, thus the fp1 can be found as：

$$fp1 = \frac{f_{3dB}}{\sqrt{\frac{\sqrt{m^4 + 2m^2(2^{\frac{N+1}{N}} - 1) + 1 - (1+m^2)}}{2}}} \quad (5)$$

The smaller the m, the larger the cell bandwidth is required to meet the overall bandwidth. Assume the required gain is 30 dB and the bandwidth is 2.5 GHz, the gain bandwidth product shows that the appropriate stage number is 5 and requirements for each stage are shown in Fig. 3. It shows that the bandwidth difference between m

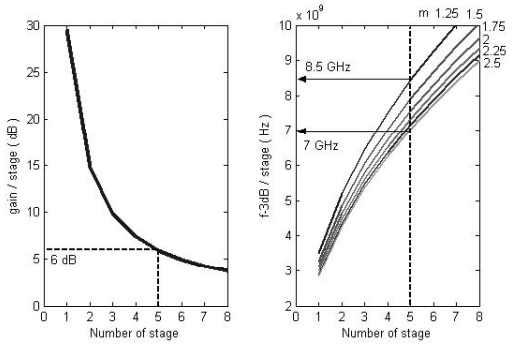

Fig. 3. Requirements of (a) gain and (b) bandwidth per stage

= 1.25 and m = 2.5 is 1.5 GHz, and under the worst case one must design a gain stage with 8.5G bandwidth. In order to achieve wideband amplification, the Cherry-Hooper typed wideband amplifier (Fig.4.) is adopted and

modified to enhance the bandwidth. The pole of the Cherry-Hooper amplifier is reduced to [6]

$$w_p = \frac{2gm_2}{C_2 + C_o + gm_2 R_2 C_{gd2}} \quad (6)$$

with respect to that without feedback. To avoid the gain-headroom trade-off in the Cherry-Hooper amplifier, the

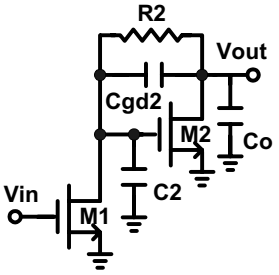

Fig. 4 Cherry-Hooper amplifier

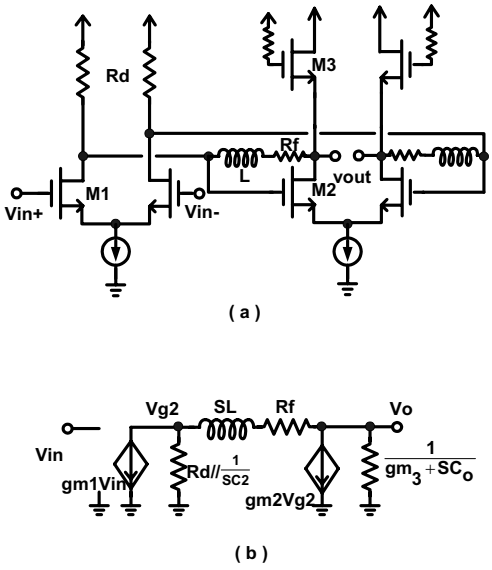

Fig. 5.(a) Gain cell for LA (b) Small signal model

additional load can be applied at the drain of transistor M1 and provides part of the bias current of the input differential pair. The modified Cherry-Hooper gain cell is shown in Fig. 5, and its small signal model including Co is shown. From the node equation, the relation between Vg2 and Vo can be found as:

$$V_{g2} = -V_o \frac{S^2 LC_o + S(C_o R_f + Lg_{m3}) + g_{m3} Rf}{g_{m2}(Rf + SL)} \quad (7)$$

If $LC_oC_dRd << 1$, then

$$\frac{V_o}{Vin} \approx \frac{g_{m1} g_{m2} Rd(Rf + SL)}{S^2(LC_o + C_oC_2RfRd + Lg_{m2}C_2R_d) + S(Lg_{m3} + C_oRf + g_{m3}RfC_2Rd) + g_{m3}Rf}$$

The equation shown above indicates an additional zero to cancel the high frequency pole and therefore the bandwidth is enlarged. In addition, it does not need a large tail current to make unity-gain frequency (ft) large. Thus the power can be smaller than conventional circuits in this band. Due to the cascaded structure, the peaking must be taken into consideration. Taking 30 dB gain with 1 dB peaking for example, the demanded quality factor per stage must be less than 0.8 corresponding to 0.7 dB peaking (Fig. 6). The differential mode stability of the limiting amplifier is verified with the stability condition parameters, k and $\triangle$. The common mode stability depends on the performance of the offset cancellation-loop, and this design is unconditionally stable and provides an offset cancellation-range ± 200mVpp. The stability of the overall front-end circuits is shown in Fig. 7.

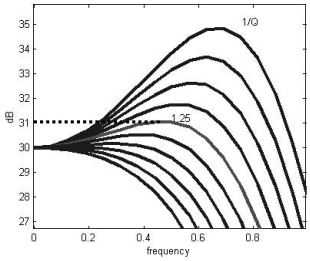

Fig. 6. Peaking of the LA

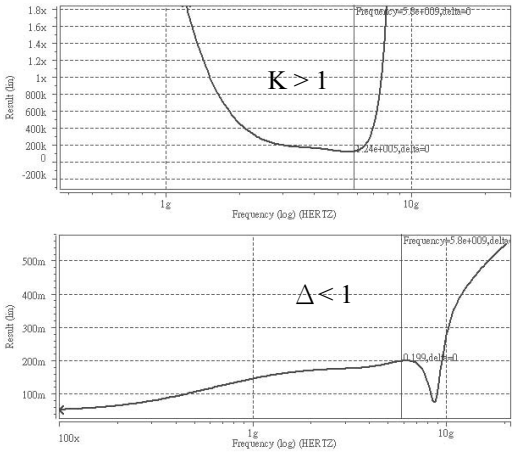

Fig. 7. Stability of the front-end circuits

4. EXPERIMENTAL RESULTS

The receiver chip is fabricated using 0.18 μm CMOS technology. The chip photo shown in Fig.8 covers an active area 1.9 x 0.9 mm^2. The external components in the testing board include a feedback cancellation capacitor, and some decoupling capacitors. The frequency response is under on-wafer testing and the eye diagram is on board testing. The sigle-ended transimpedance gain is 60 dBΩ with 1.72 GHz bandwidth which is sufficient for 10GBASE-LX4. (Fig. 9.) Since the random data generator can only provide a 250mVpp data sequence, which is not small enough for sensitivity testing, an additional 30 dB wideband attenuator is used to achieve the require-

ment. The testing random pattern with 2^{31} -1 pseudo-random bit sequence (PRBS) is applied to the chip input and the eye diagrams under the minimum and maximum inputs at the data rate from 1.25 Gb/s to 3.125 Gb/s are shown in Fig. 10 (a)(b)(c) respectively. An important parameter of the receiver is the data jitter. The data jitters for 1.25 Gb/s, 2.5 Gb/s and 3.125 Gb/s under 2^9 -1 PRBS are 42 ps (pp), 108 ps, and 113 ps respectively. The large jitter under -18 dBm input signal is due to the random jitter resulting from thermal noise, variation of the supply voltage and the finite chip bandwidth. The performance is summarized in TABLE1.

5. CONCLUSION

The receiver front end including transimpedance amplifier and fully differential limiting amplifier for 10GBASE-LX4 is presented. The modified Cherry-Hooper gain cells are proposed to lower the power dissipation in the limiting amplifier. The sensitivity of the chip at 3.125Gb/s is -16dBm and delivers 250mVpp to the next stage. This receiver active size is 1.9 x 0.9 mm^2 and it consumes 54mW from a 1.8 V power supply.

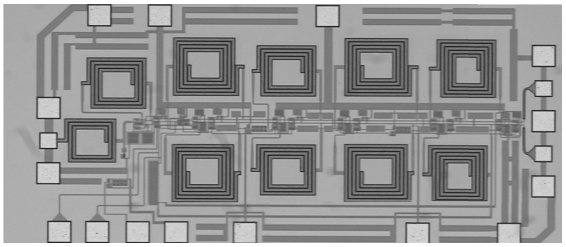

Fig. 8 Chip photo of the receiver front-end circuits

Technology	CMOS 0.18 μm , 1.8 V
Bandwidth	1.7 GHz
AC Gain	60 dBΩ
Rise / Fall Time (10 % - 90 %)	68 ps
Output swing	250 mVpp
Data jitter @ 3.125 Gb/s	113 ps (p-p)
Input sensitivity	-16 dBm
Input Return Loss	< -8 dB
Power Dissipation	54 mW

TABLE1 Performance summary of receiver front-end transimpedance amplifier and limiting amplifier

6. REFERENCES

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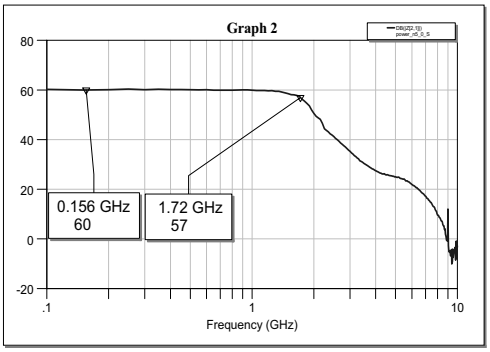

Fig. 9. Frequency response of the receiver front end

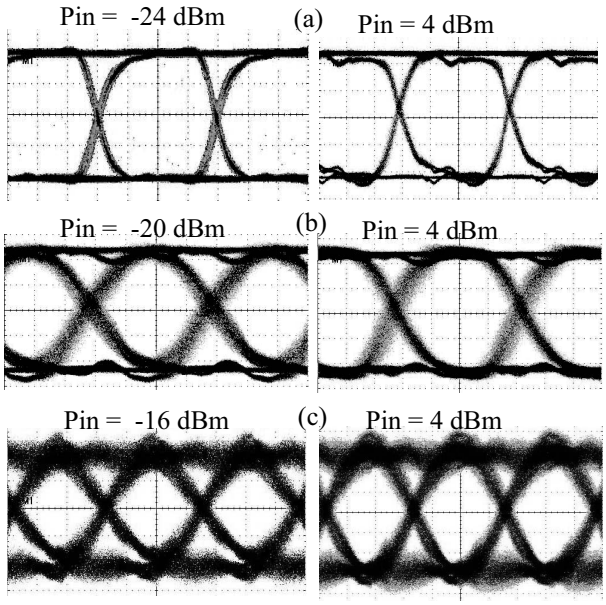

Fig. 10. Eye diagrams at (a) 1.25 Gb/s (b) 2.5 Gb/s (c) 3.125 Gb/s

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