An Analytical Back Gate Bias Dependent Threshold Voltage Model for SiGe-channel Ultra-thin SOI PMOS Devices

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Abstract

This paper reports an analytical threshold voltage model for SiGe-channel ultra-thin SOI PMOS devices. As confirmed by the PISCES simulation results, the analytical model provides a good prediction on the threshold voltage. According to the analytical formula, depending on the back gate bias, the SiGe-channel SOI PMOS device may have a conduction channel at the top or the bottom of the SiGe channel or at the top of the field oxide.

Summary

Recently, a high performance SiGe-channel PMOS device built on SOI structure using SIMOX technology has been reported [1]. For an SOI MOS device, its substrate bias effect on the threshold voltage is complicated [2]. Depending on the back gate bias, the ultra-thin SOI PMOS device may have a surface channel, or a buried channel and a surface inversion in the substrate depending on the substrate bias. This paper reports comparison of an SOI PMOS device with and without SiGe-channel in terms of internal hole distribution and back gate bias effects are described. In addition, an analytical back-gate-bias dependent threshold voltage model derived from Poisson's equation for SOI PMOS devices with a SiGe channel is described.

Fig. 1 shows the cross section of the SiGe-channel SOI PMOS device structure using a SIMOX process [3] under study. The ultra-thin SOI PMOS device using an $N+$ polysilicon gate, has a front gate oxide of $120\mathring{A}$ (t_{ox1}). Below the gate oxide, a silicon thin film of $1000\mathring{A}$ is sitting on a field oxide of $3500\mathring{A}$. In the thin film an undoped silicon cap of $60\mathring{A}$ below the gate oxide is placed atop the undoped SiGe-channel of $200\mathring{A}$, where the germanium density is 0.25. Below the SiGe-channel, an n-type thin film of $740\mathring{A}$ doped with $1 \times 10^{16} cm^{-3}$ is used. Below the field oxide, a p-type substrate region with a doping concentration of $1 \times 10^{15} cm^{-3}$ has been used in the study. Fig. 2 shows the internal carrier density distribution in the center of the SiGe-channel PMOS SOI device for various back gate biases and biased at a drain current of $I_D = 0.1\mu A/\mu m$ and $V_{DS} = -0.1V$. Depending on the back gate bias, classified by the carrier distributions there are four cases – Case I: a conduction channel at the top of the SiGe-channel and no inversion in the substrate, Case II: a conduction channel at the bottom of the SiGe-channel and no inversion in the substrate, Case III: a conduction channel at the bottom of the SiGe-channel and an inversion in the substrate, Case IV: a conduction channel at the top of the field oxide and an inversion in the substrate.

Owing to the existence of SiGe quantum well, a conduction channel is always present first in the SiGe region and the charge in the silicon cap can be neglected. Considering the depletion region under the insulator, Poisson's equation and Gauss's law have been used to solve for the internal potential distribution in the SiGe-channel SOI PMOS device biased at a various back-gate voltage. Solving these equations, the threshold voltage,V_{TH} has been derived for the above four cases. In order to show the effectiveness of the analytical model, the analytical model results have been compared with simulation results using PISCES, where germanium-induced bandgap narrowing phenomenon has been included [4]. Fig. 3 shows the internal potential distribution in the substrate direction in the SOI PMOS devices with SiGe-channel biased at a front gate voltage of $V_G = -0.5V$ and $V_{DS} = -0.1V$ for a back gate bias from $0V$ to $-5V$ in the center of the device in the substrate direction using the analytical model and PISCES results. As shown in the figure, the analytical model results show a good match with the PISCES results. Fig. 4 shows the threshold voltage vs. back-gate bias voltage curves for the SOI PMOS device using the analytical model and PISCES results. As shown in the figure, four cases – Case I, II,III,IV can be identified. In each case, the subthreshold slope with respect to the back gate bias is different. A good match between the PISCES and the analytical model results can be found. Fig. 5 shows the threshold voltages of the SOI PMOS device with and without SiGe-channel. As shown in the figure, as V_B is smaller than $-4.2V$, little difference exists in the threshold voltages of the SOI PMOS device with and without SiGe channel. As the back gate bias shifts toward the positive direction, the difference between the two cases gets larger. From Fig. 5, as the back gate bias is more negative than V_{BT34}, little difference exists between the devices with and without SiGe-channel. This implies that if V_B is smaller than V_{BT34}, the attractiveness of the SiGe-channel used in the SOI PMOS device does not exist any more. The doping density below the SiGe-channel in the thin

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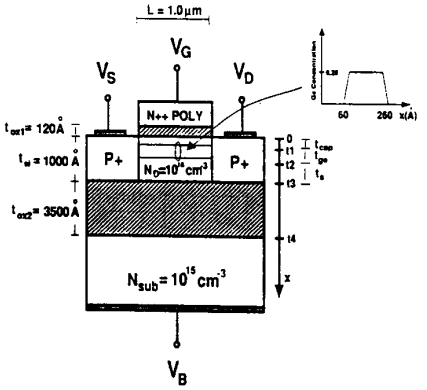
film also influences the back gate bias effect of the SiGe channel SOI PMOS device. Fig. 6 shows the threshold voltage vs. the doping density of the thin film below the SiGe channel. From this figure, for a lighter doped thin film, the back gate bias effect is more serious — a more difference between the $V_B = 0V$ and $V_B = -5V$ cases can be seen. In fact, this thin film doping density also affects the three transition voltages.

[1] D. K. Nayak, et al., *IEDM*, pp.777-780, 12/1992
[2] J. H. Sim and J. B. Kuo, *IEEE TED*, 4/1993
[3] T. W. MacElwee, et al.,*IEEE TED*, pp.1444-51, 6/1990
[4] J. B. Kuo, et al., VPAD, Nara, Japan, 5/1993



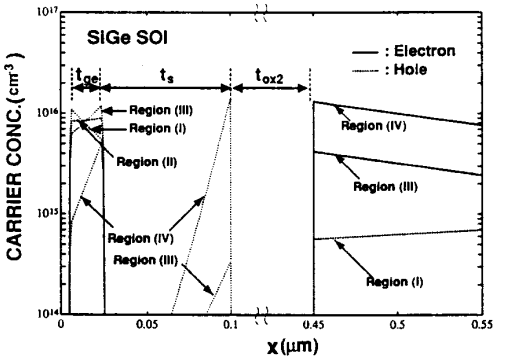
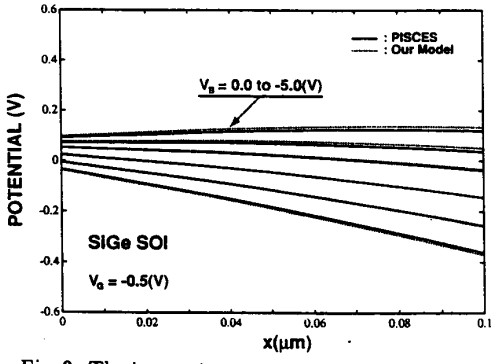


Fig. 1. Cross section of the SiGe-channel SOI PMOS device under study.
Fig. 2. The internal carrier density distribution in the center of the SOI device biased at various back gate biases and a drain current of $10^{-7}A/\mu m$ with SiGe-channel



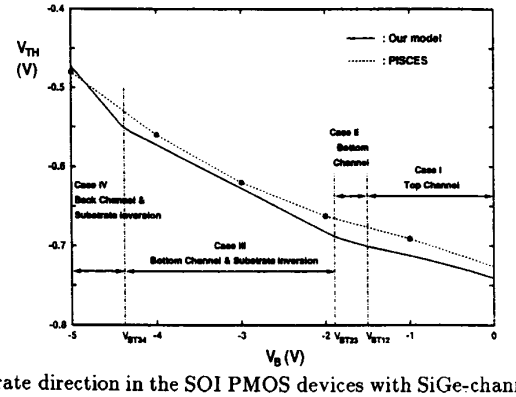
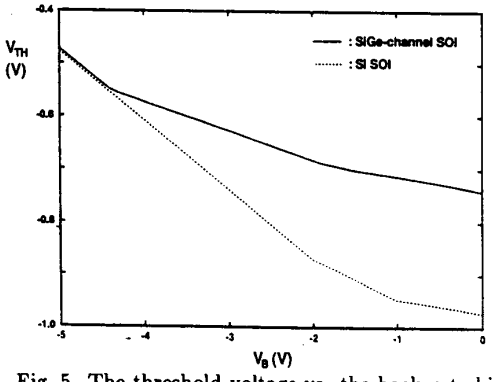


Fig. 3. The internal potential distribution in the substrate direction in the SOI PMOS devices with SiGe-channel biased at a front gate voltage of $V_G = -0.5V$ and $V_{DS} = -0.1V$ in the center of the device in the substrate direction using the analytical model and PISCES results.
Fig. 4. The threshold voltage vs. back-gate bias voltage curves for the SiGe-channel SOI PMOS device using the analytical model and PISCES results.



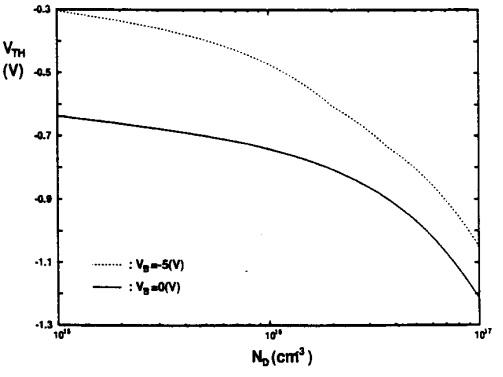


Fig. 5. The threshold voltage vs. the back gate bias curves of the SOI PMOS devices without and with SiGe-channel.
Fig. 6. The threshold voltage vs. the doping density of the thin film below the SiGe channel of the SOI PMOS device biased at $V_B = 0V$ and $-5V$.