Accumulation-type vs. Inversion-type: Narrow Channel Effect in VLSI Mesa-Isolated Fully-Depleted Ultra-thin SOI PMOS Devices

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Abstract

The paper reports the sidewall-related narrow channel effect in mesa-isolated fully-depleted ultra-thin SOI inversion-type and accumulation-type PMOS devices. Based on the study, contrary to inversion-type devices, the threshold voltage of mesa-isolated ultra-thin SOI accumulation-type PMOS devices shrinks as the channel width scales down as a result of the buried-channel effect influenced by the sidewall via the buried oxide.

Summary

Short channel effects in ultra-thin SOI MOS devices have been reported [1]-[3]. Mesa isolation technology has been used for fully-depleted ultra-thin SOI MOS devices [1]. Recently, sidewall-related narrow channel effect in mesa-isolated fully-depleted ultra-thin SOI inversion-type MOS devices has been reported [5]. For ultrathin SOI MOS technology, accumulation-type devices are also feasible [6]. In this paper, sidewall-related narrow channel effect in mesa-isolated fully-depleted ultra-thin SOI inversion-type and accumulation-type PMOS devices is reported.

Fig. 1 shows the cross section of the mesa-isolated fully-depleted ultra-thin SOI PMOS device with the sidewall structure. The mesa-isolated fully-depleted ultra-thin SOI PMOS device using an N^+ polysilicon gate has a thin film of 1000Å doped with an acceptor(accumulation-type)/ donor(inversion-type) density of $10^{17}cm^{-3}$ above a buried oxide. Owing to the mesa-isolation structure, an oxide sidewall of 150Å to the right of the thin film region and a front gate oxide of 100Å have been included. PISCES simulation has been used to obtain the results.

Fig. 2 shows threshold voltage vs. channel width of the mesa-isolated fully-depleted ultra-thin SOI PMOS device as shown in Fig. 1 with a buried oxide of 1000Å, 2000Å and 4000Å. As shown in Fig. 2, when the channel width is smaller than $0.6\mu m$, its threshold voltage is sensitive to the channel width. In the mesa-isolated ultra-thin SOI inversion-type PMOS device, a narrower channel leads to a larger threshold voltage as a result of the sidewall edge effect. In addition, the narrow channel effect of mesa-isolated ultra-thin SOI inversion-type PMOS device is insensitive to the thickness of the buried oxide. On the contrary, for the accumulation-type PMOS device, a narrower channel leads to a smaller threshold voltage. Furthermore, the narrow channe effect of accumulation-type devices is sensitive to the thickness of the buried oxide. Fig. 3 shows the 2D electrostatic potential contours at an interval of $0.05V$ in the ultrathin fully-depleted SOI (a) inversion-type and (b) accumulation-type PMOS devices as shown in Fig. 1, with a channel width of $0.4\mu m$, biased at their threshold voltages. As shown in the figures, in the inversion-type device, the sidewall structure has a direct impact on the thin film region near the sidewall. In the accumulation-type device, the influence of the sidewall is overwhelmed by the buried channel above the buried oxide. Fig. 4 shows the electrostatic potential in the horizontal direction at one half of thin film thickness in the thin film of the ultrathin fully-depleted SOI inversion-type and accumulation-type PMOS devices with a channel width of $0.4\mu m$ and $1.2\mu m$, biased at their threshold voltages. As shown in the figure, in the inversion-type device, the lateral electrostatic potential distribution is location-dependent— the sidewall has a direct impact on the potential distribution. On the other hand, in the accumulation-type device, the lateral electrostatic potential distribution is much less location-dependent, especially near the center region. Fig. 5 shows the electrostatic potential in the vertical direction in the center of the thin film in the ultrathin fully-depleted SOI inversion-type PMOS device with a channel width of $0.2\mu m$, $0.4\mu m$ and $1.2\mu m$, biased at its threshold voltage. In the inversion-type device, it has a surface inversion channel. As the channel width shrinks, all of the region in the thin film except the surface channel is affected. On the contrary, as shown in Fig. 6, in the accumulation-type device, it has a buried channel above the buried oxide. As the channel width shrinks, the buried channel moves toward the surface as influenced by the sidewall structure via the buried oxide.

References

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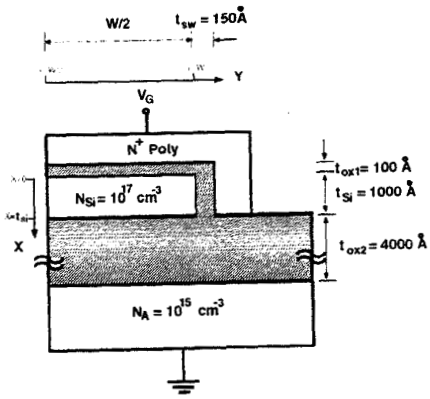


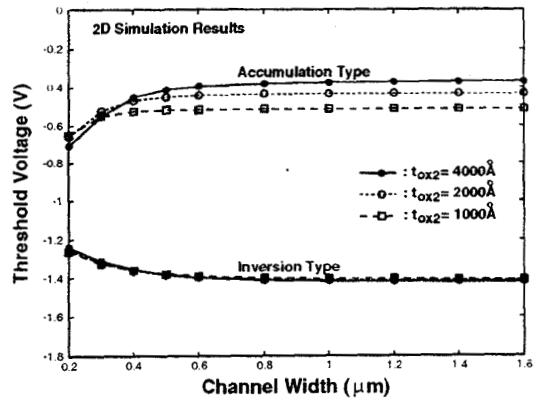
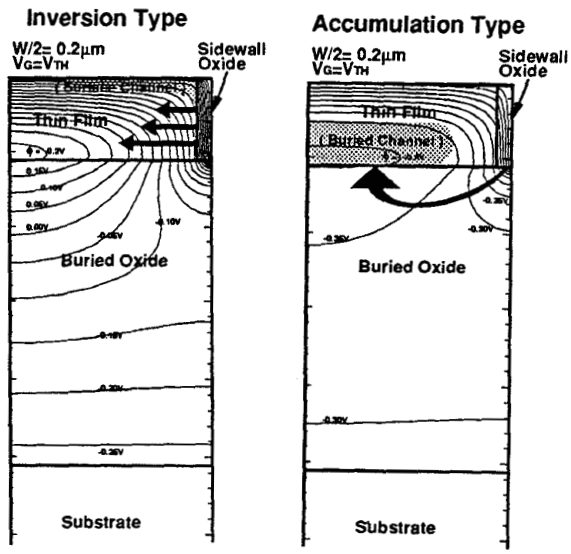


Fig. 1. Cross section of the mesa-isolated fully-depleted ultra-thin SOI PMOS device with oxide sidewall.
Fig. 2. Threshold voltage vs. channel width of the mesa-isolated fully-depleted ultra-thin SOI PMOS device.



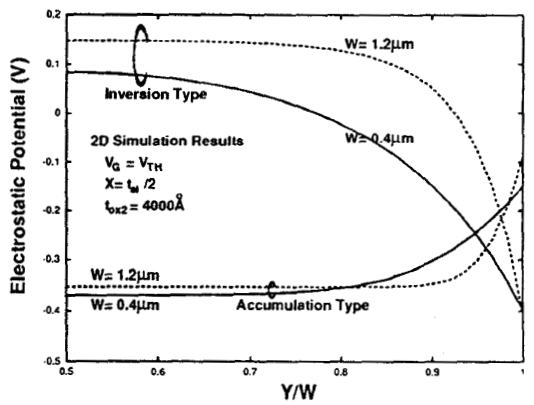
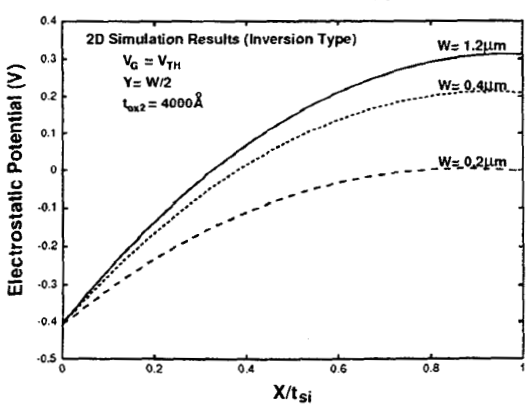


Fig. 3. The 2D electrostatic potential contours in the ultrathin fully-depleted SOI (a) inversion-type and (b) accumulation-type PMOS devices as shown in Fig. 1.
Fig. 4. The electrostatic potential in the horizontal direction at one half of thin film thickness in the thin film of the ultrathin fully-depleted SOI inversion-type and accumulation-type PMOS devices.



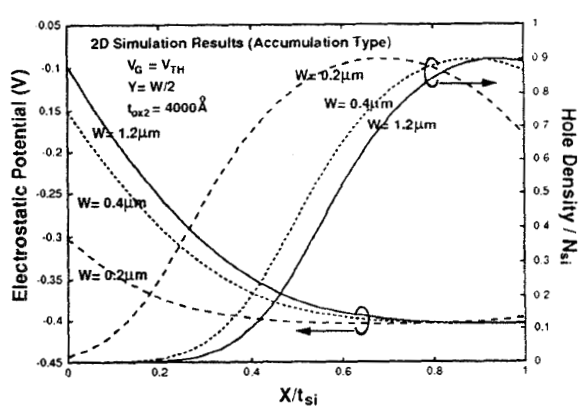


Fig. 5. The electrostatic potential in the vertical direction in the center of the thin film in the ultrathin fully-depleted SOI inversion-type PMOS device.
Fig. 6. The electrostatic potential and the hole density in the vertical direction in the center of the thin film in the ultrathin fully-depleted SOI accumulation-type PMOS device.