A New High-Performance AC-to-AC Conversion System

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Abstract - A new high-performance variable-voltage variable-frequency (VVVF) AC-to-AC conversion system is proposed. This system consists of an AC/DC SCR rectifier, an LC DC-link, and a three-phase DC/AC PWM inverter. The rectifier is operated under cosine-mode feedback which linearizes the closed-loop control characteristics. The PWM inverter receives gating signals from a ROM-based modulator with off-line computed PWM patterns. In this way, the inverter output frequency varies with the controlled clock frequency and the magnitude of the AC output voltage is regulated by the SCR rectifier. Without on-line microprocessor computations or discrete circuit implementation, this system features quick output response and low control complexity. Laboratory experiments have been performed to verify this idea and satisfactory results have been recorded.

INTRODUCTION

An AC-to-AC system formed by the rectifier, DC link and the inverter is widely used in AC drive applications. To reduce the total harmonic distortion and audible noise, the pulse-width modulated voltage source inverter (PWM-VSI), shown conceptually in Fig. 1, has replaced the so-called six-step inverter at all but the highest power levels [1]. Conventionally, control signals fed to PWM inverters are produced by discrete circuit or microprocessors [2-4]. The cost and complexity of hardware implementation are considerable and on-line microprocessor computation is memory-intensive and time-comsuming. Also, software development are required.

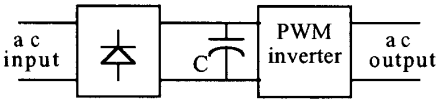

Fig. 1 Diode rectifier/PWM inverter system

Recently, a ROM-based PWM modulator proposed by R. Simard, etc. [5] partly solves the problems mentioned above. It combines the advantages of fast response of the analogue technique and simple hardware of the microcomputer approach, but provides output patterns at several discrete amplitude ratios and frequencies only. Also, the small values of amplitude modulation ratio m_a [6] for low output voltages results in larger total harmonic distortion (THD) [7] at the output stage.

A ROM-based PWM technique is presented in this paper for producing the inverter gating signals. Three-phase PWM control signals are computed off-line. To program this PWM signal pattern into a ROM, each pulse is composed of several consecutive '1's to represent its width. The duration between pulses are represented by consecutive '0's. This digitized PWM pattern can then be retrieved sequentially by incrementing the address counter. Also by varying the rate of counting, the stored PWM pattern is outputed in varying speed. In this way, the AC output frequency can be continuously varied when a voltage-controlled oscillator (VCO) is utilized. With this new ROM-based PWM technique, various PWM control schemes, such as sine-triangle PWM (SPWM), regular-sampled PWM, harmonic injection PWM (HIPWM) and space vector PWM, can be easily applied. Yet with ROM-based PWM, the amplitude modulation ratio m_a is fixed. Although the THD can be reduced when m_a is set large , the DC/AC inverter controls the output frequency only and fails to regulate the output voltage magnitude.

In this paper, a new variable-voltage variable-frequency (VVVF) AC-to-AC drive system, shown in Fig. 2, is proposed. A front-end controlled rectifier generates a controllable intermediate DC voltage, an inverter with ROM-based PWM control converts the DC voltage to AC outputs. The rectifier is operated under an improved cosine-mode feedback control scheme which simplifies the control complexity and linearizes the transfer characteristic of firing angles vs. DC output voltages. A VCO with counters counts through the addresses of the ROM to retrieve the stored PWM gating signals. The amplitudes and the frequencies of the output voltages can be independently controlled by firing angles of the rectifier part and the VCO rates of the inverter part.

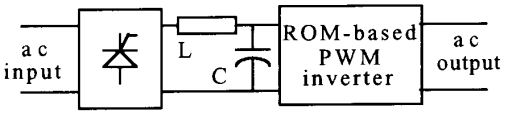

Fig. 2 Proposed AC-to-AC system

Both VVVF and constant flux (V/f) operations in AC drive applications [8] can be easily achieved in the proposed system. This new system features the advantages of low cost, low THD, fast response, simple control and easy implementation.

CONTROLLED RECTIFIER

The DC output voltage of the semi-bridge controlled rectifier, as shown in Fig. 3, is related to the AC input voltage as :

$$\langle V_o \rangle = \frac{Vs}{\pi} (\cos\alpha + 1)$$

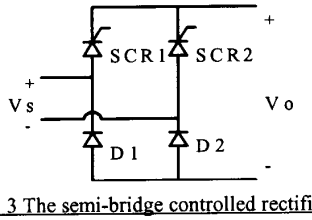

Fig. 3 The semi-bridge controlled rectifier

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where Vs is the amplitude of the AC input and α is the firing angle. There is a nonlinear transfer characteristic between control variable α and output voltage, resulting in a somewhat complicated control. An indirect control method (cosine control) [9] is used to linearize the control characteristic. A new control variable v_α is defined as :

$$v_\alpha = \cos\alpha + 1 ,$$

thus ,

$$\langle V_o \rangle = \frac{Vs}{\pi}(v_\alpha)$$

The cosine firing scheme provides a linear transfer characteristic between the output voltage and the control voltage v_α. The basic control scheme is shown in Fig. 4.

A scaled voltage, v_1 , of the ac input is first integrated to a cosine signal v_2 . Through a peak detector and an inverter, two signals , v_3 ($=1+v_2$) and v_4 ($=1-v_2$) are produced. These voltages are then compared to the new controlling variable v_α to produce v_5 and v_6, which are two trains of pulses commencing at $\omega t = \alpha$, and $\omega t = \pi + \alpha$ in a fundamental period, respectively. A zero-crossing detector produces v_7 to determine which SCR of the semi- bridge is going to be turnde on.

The pulses of v_5 and v_6 start when $v_\alpha = \cos\alpha + 1$ and $\cos(\pi+\alpha) + 1$. If $v_7 = 1$, the operating device should be SCR1, while SCR2 operates when $v_7 = 0$, that is, when the input voltage is in its negative half cycle. A pulse train produced by anding with a high frequency oscillator (10kHz-30kHz) ensures effective triggering. The signal amplifier of totem-pole type amplifies the pulse current to turn on the SCRs. Also the volume of the isolation pulse-transformer is reduced because of high frequency operation. A timing diagram is shown in Fig. 5.

Conventionally, the control circuit of a SCR rectifier utilizes monostables to detect the rising edge of triggering pulses[9]. Because of the high frequency noises, there are more than one triggering pulses at the intersections of the two input signals. Thus the triggerings would be mistaken if not properly solving the inevitable "bouncing" problem of the output of an op amp, as shown in Fig. 6. In Fig. 5. SCR1 and SCR2 should be ON at t1 and t3, respectively, if the monostable circuits can correctly detect the rising edges of the triggering pulses. Chances are the monostables may detect a rising signal at a falling edge, say, at t2, because of the bouncing problem of the comparators. This results in the false "ON" signal for SCR2, which should not start conducting at t2. Here we substitute a zero-crossing detector and TTL "AND" circuits for the monostables. It works well and produces no mistaken triggering signals.

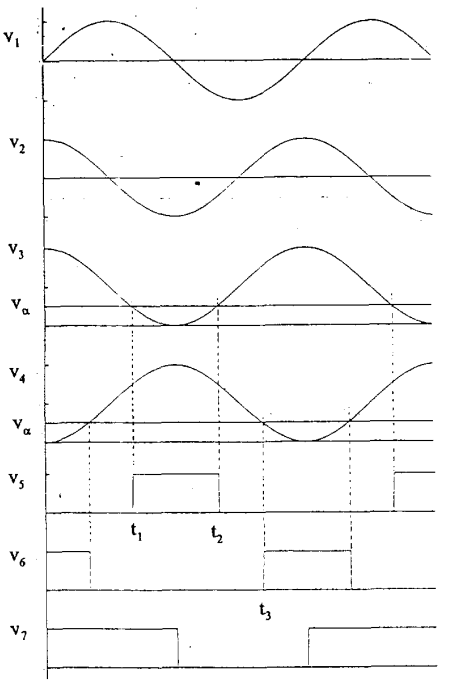

Fig. 5 Timing diagram

Fig. 6 The bouncing problem

INVERTER

A sine-triangle PWM pattern is produced by comparing a sinusoidal reference signal of the desired frequency and a triangular carrier signal. The switching instants, and therefore the time duration of pulses are determined by the intersections of the reference signal and carrier signal. In this paper, the PWM control signals are pre-calculated by computing the intersections of a fundamental sinusoidal wave and a triangular carrier wave with numerical approach. Then the analogue PWM signals are digitized, that is ,"1" represents "high" and "0" represents "low". This pattern is stored in an EPROM. The flow chart is shown in Fig. 7.

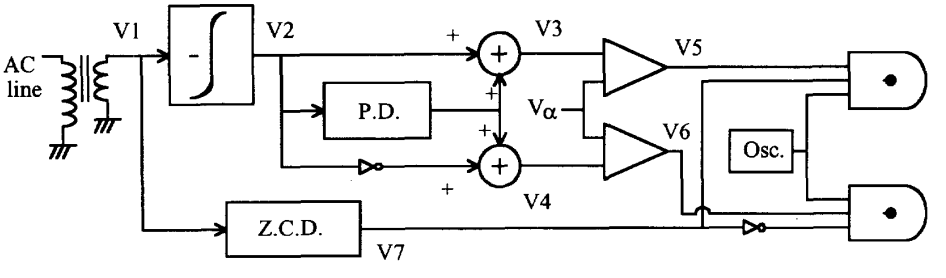

Fig. 4 Functional block of cosine control scheme.

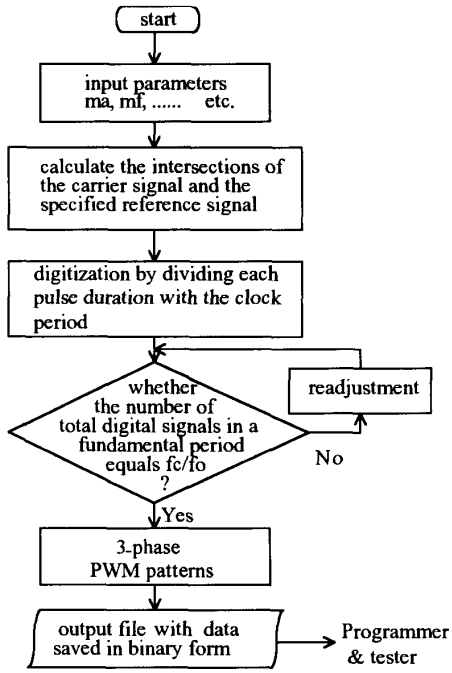

Fig. 7 Flowchart of designing a ROM-based PWM modulator

First we define some parameters of the reference signal and set proper values to them. Then the intersections of the triangular carrier signal and the specified reference signal (a pure sinewave or a harmonic-injected sinewave) are calculated by numerical method. The two consecutive intersections define a time duration of turn-on or turn-off, depending on the instantaneous amplitudes of these two signals. We translate the computed analogue PWM pulses into a series of digital signals by dividing each time duration with the clock period. The length of consecutive " 1 " or " 0 " signals is determined by the corresponding pulse width. In handling the remainder less than a clock period, a round-off algorithm is used. To make sure that the desired fundamental frequency of the PWM patterns is produced by the EPROM, it is necessary to check whether the number of the total digital signals in a fundamental period equals the value of (clock frequency / fundamental frequency), fc/fo . To generate the 3-ϕ patterns, just delay the original one by 120^0 and 240^0 , that is, by saving the original digital data starting at 1/3 length and 2/3 length , respectively, to the output files. Then the digital PWM patterns are programmed into an EPROM.

A clock counts through the addresses to retrieve the stored PWM control patterns. Thus, the frequency of the fundamental AC output varies with the speed of the clock. A VCO featuring a linear transfer characteristic between the input control voltage and the output frequency is used to vary the counting speed. A " CLEAR" signal is sent by the EPROM to ensure that after counting through the entire addresses of a period, another period can start from the beginning of the stored pattern.

For a bridge type of inverter, the dead time is needed to prevent the cross conduction of switches. Here we use the one-shot ICs to detect the rising edge of the PWM pulses and produce a programmable time duration. Anding these short pulses with the original PWM pattern, a PWM control signal with dead time programmed is produced. The functional blocks of the ROM-based PWM moculator is shown in Fig. 8.

IMPLEMENTATION

In the control circuit for the SCR rectifier, there are integrator, zero-crossing detector, peak detector, summing circuits and comparators. The oscillator is a 555 timer with 20kHz frequency. The gate drive consists of totem-pole current amplifier, isolation pulse transformer and gate protection circuit. To protect against dv/dt false turn-on of an SCR, a series R-C snubber circuit is placed across the thyristor.

For the inverter part, the VCO features a frequency range over 1 : 5 (from 240kHz to 1.2MHz), and a linear transfer characteristic between input voltage and output frequency. As for the EPROM, we record the SPWM pattern with $m_f = 249$, $m_a = 0.9$. Also a HIPWM (Harmonic Injection PWM Method) pattern with the 3rd harmonic injected is stored for comparison. In the experiments, the frequency range is defined from 40Hz to 200Hz. So , it needs 6k (240k/40, or 1.2M/200) bits to store a complete period of a PWM pattern. For a 3-ϕ pattern, a 2764 (8k×8) EPROM is enough. A "CLEAR" signal is sent by the 7th output of the EPROM to reset the 74393 counters. A synchronous D-FF 74374 is used to hold the outputs of the EPROM stable. The monostables 74123s detect the rising edges of the PWM pulses and produce the programmable dead time. The PWM patterns with the dead time are then amplified and fed to the opto isolators.

EXPERIMENTS

Illustrated in Fig. 9 is the linear transfer characteristic of the control voltage v_{cl} and the output DC voltage, V_{out} , of the SCR rectifier. The first order fitting polynomial is :

$$V_{out} = 15.1457\, v_{cl} + 0.5581$$

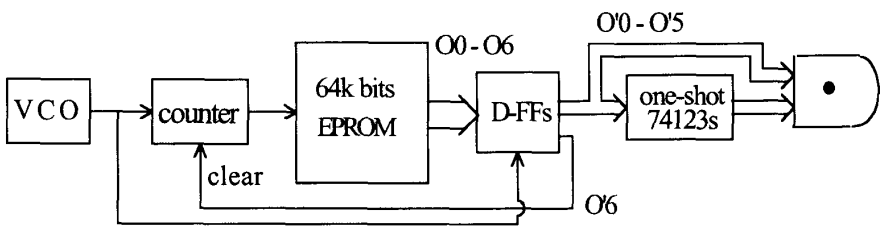

Fig. 8 Functional blocks of ROM-based PWM modulator.

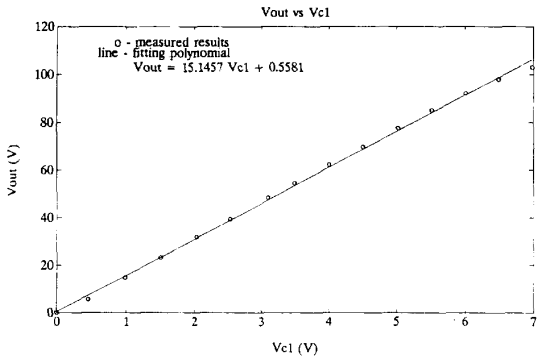

Fig. 9 Vout vs. Vc1

Fig. 10 shows the linear transfer characteristic between the control voltage v_{c2} and fundamental output frequency of the PWM pattern. The first order fitting polynomial is :

$$freq = 273\ v_{c2} - 445.56$$

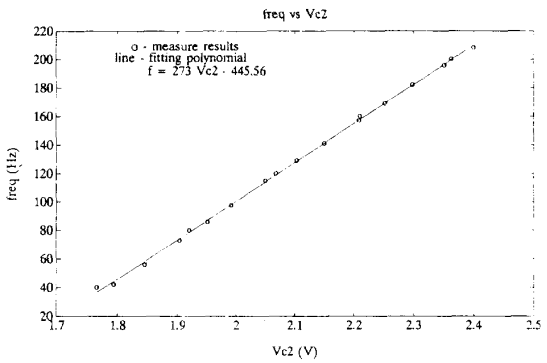

Fig. 10 freq vs.Vc2

The output voltage of the rectifier and the output frequency of the inverter can be controlled independently, if v_{c1} and v_{c2} are varied independently.

For a control under fixed V/f ratio, the control algorithm is listed in the following steps :

Step1 : Set fixed V/f ratio, r.

Step2 : $V_{out} = a \cdot v_{c1} + b$ and $freq = c \cdot v_{c2} + d$, a, b, c and d are constants acquired from experiments.

Step3 : Let

$$\frac{V_{out}}{freq} = \frac{a \cdot v_{c1} + b}{c \cdot v_{c2} + d} = r ;$$

Step 4 : Choose one control variable as the independent one, say, v_{c2}, then :

$$v_{c1} = \frac{r \cdot c \cdot v_{c2} + r \cdot d - b}{a}$$

To test the function of the fixed V/f ratio featured by this control circuit, we assume that the V/f ratio is 0.45 v/Hz (V: 18 ~ 90 v, f : 40 ~ 200 Hz).

$$\frac{V}{f} = \frac{15.1457 \cdot v_{c1} + 0.55}{273 \cdot v_{c2} - 445.56} = 0.45 ;$$

$$v_{c1} = \frac{122.8575 v_{c2} - 206.31}{15.1457}$$

We choose v_{c2} as the independent control variable and v_{c1} the dependent variable. Once v_{c2} is decided, so is v_{c1}. From Fig. 11, we see clearly that the V/f ratio is almost constant (0.4531) in the experimental frequency range (40 ~200 Hz).

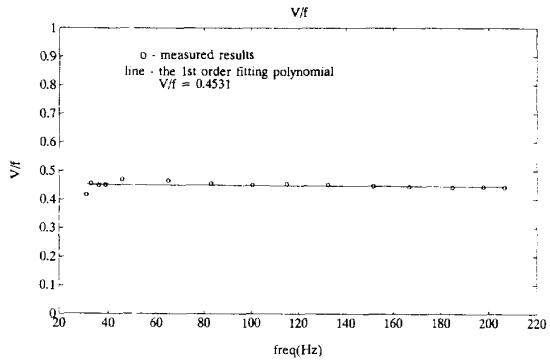

Fig. 11 V/f vs. freq

Shown in Fig. 12 and Fig. 13 are the SPWM patterns of 86.5Hz and 184.8Hz with two different phases plotted together. Fig. 14 and Fig. 15 depict the HIPWM patterns of 74.5Hz and 184.8Hz , respectively. We see clearly that because of fewer switchings at the peaks of the fundamental sine wave, the HIPWM produces more amplitude of fundamental voltage than SPWM does.

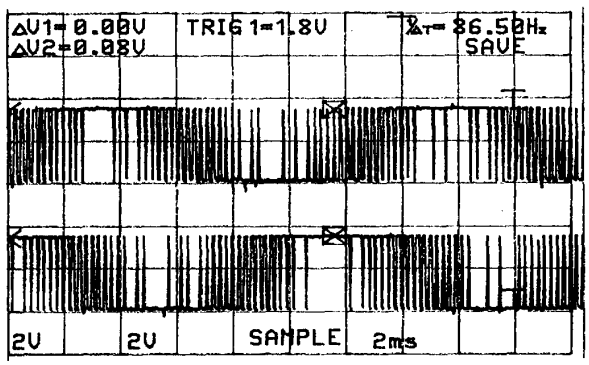

Fig. 12 Two phases of 86.5 Hz SPWM pattern

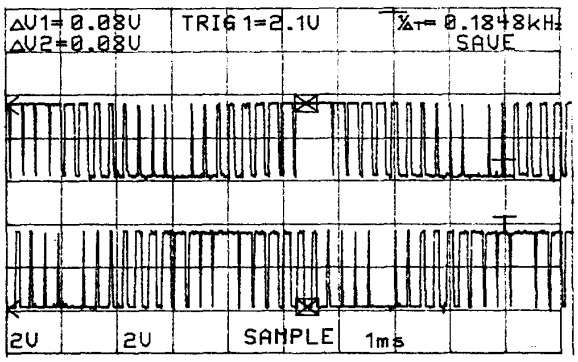

Fig. 13 Two phases of 184.8 Hz SPWM pattern

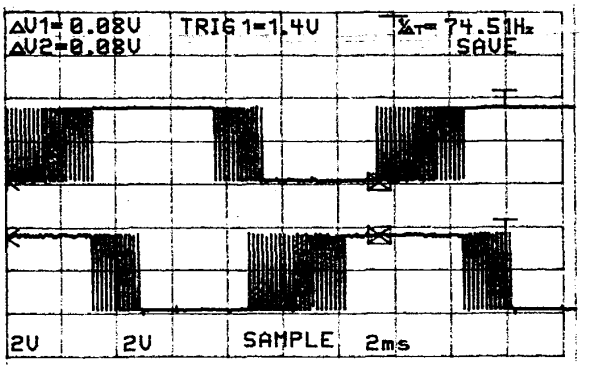

Fig. 14 Two phases of 74.5 Hz HIPWM pattern

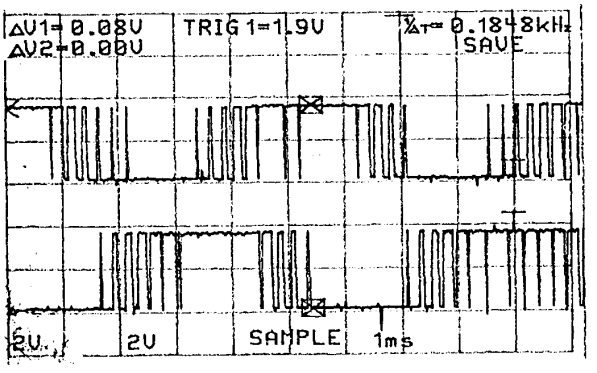

Fig. 15 Two phases of 184.8 Hz HIPWM pattern

In Fig. 16, the upper part is the ideal local PWM pattern, and the lower part is the same pattern with 10 ms dead times programmed at each rising edge . A pair of refined PWM control signals fed to the two switches of one switching leg are shown in Fig. 17, where each turn-on has been delayed 10 ms. Also shown in Fig. 18 and Fig. 19 are the voltage waveforms and their dc values of the rectifier's output when $\alpha = 60°$ and $\alpha = 130°$, respectively.

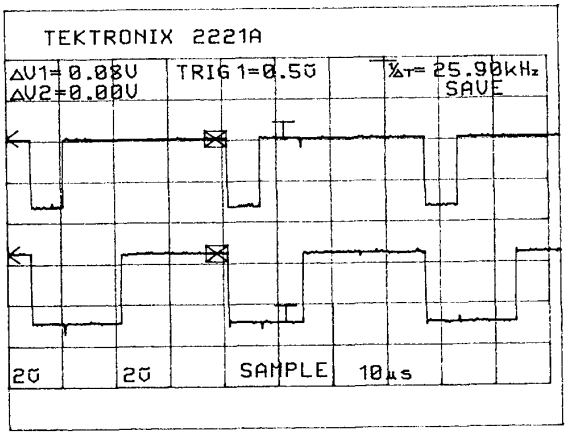

Fig. 16 The local PWM patterns without and with dead times.

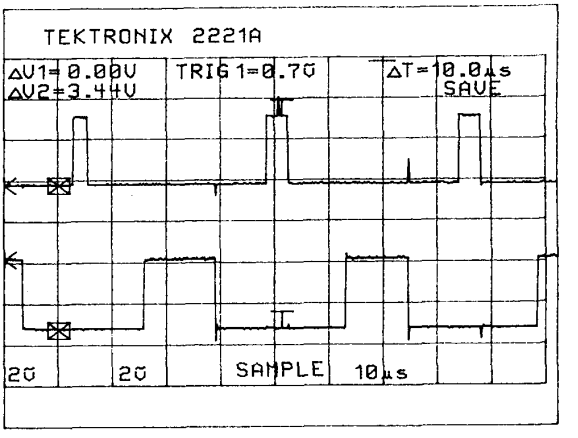

Fig. 17 A pair of local PWM patterns with dead times.

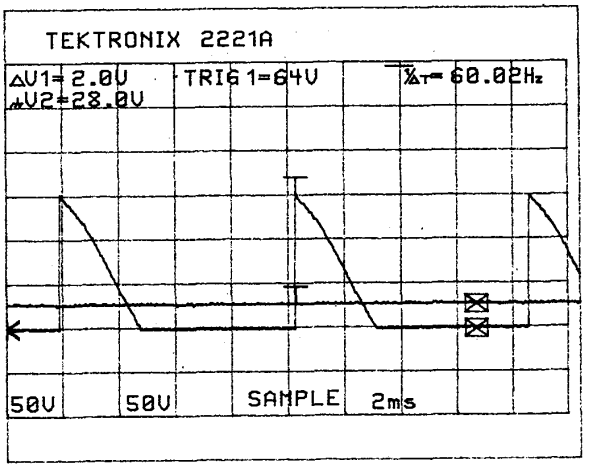

Fig. 18 Rectifier's output at $\alpha = 60°$.

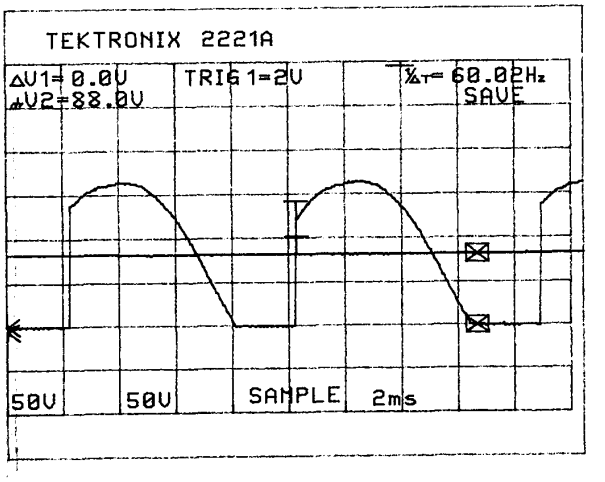

Fig. 19 Rectifier's output at $\alpha = 130°$.

CONCLUSIONS

The proposed scheme of AC-to-AC system consisting of a controlled SCR rectifier and a ROM-based PWM inverter features the fast response of analog circuits and simplicity of digital circuits. The improved cosine control of SCRs is used to obtain a linear control characteristic and to avoid the bouncing problem of op amps. The ROM-based PWM modulators provide an easy, fast and steady control for the inverter. The fixed PWM patterns such as SPWM, HIPWM are stored in 64k bits EPROMs. Combining the rectifier part and inverter part together, we can easily perform the command of VVVF control. Experiments have illustrated satisfactory results.

The studied system can be divided into two independent modules : the rectifer part and the inverter part. The SCR rectifier can be replaced by other AC-to-DC converters, such as switch-mode rectifiers[10-12]. In the inverter part, compensation for the inserted dead time [13,14] deserves more study to provide accurate and low harmonic AC power.

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