A 0.8 V Switched-opamp Bandpass ΔΣ Modulator Using a Two-path Architecture

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Abstract

In this paper, a very low-voltage fourth-order bandpass delta-sigma modulator with a two-path architecture is presented. Using the modified switched opamp technique enables the modulator to operate at only 0.8 V supply voltage without any voltage multiplier or bootstrapping switch. Realized in a 0.25-μm 1P5M standard CMOS process, the prototype modulator exhibits a signal-to-noise-plus-distortion ratio (SNDR) of 60.6 db and a dynamic range (DR) of 68 db in a 30 KHz signal bandwidth centered at 1.25 MHz while consuming 2.5 mW and occupying an active area of 2.11 mm^2.

Introduction

Increasing growth of wireless and portable communication leads to a request for low-voltage and high dynamic range bandpass A/D converters. The architectures of bandpass ΔΣ modulators [1] can be divided into three major categories: continuous-time, switched-current, and switched-capacitor types. Because the first two have common disadvantages: less accuracy and low dynamic range than the last one, they are not suitable for high resolution applications. A switched-capacitor bandpass ΔΣ modulator can be synthesized by Forward-Euler, Lossless-Discrete-Integrator, Pseudo-2-path, Two-delayed, and Two-path [2] filters. Using a two-path structure can relax the speed requirement of analog circuits and the advantage will become more significant in low-voltage operation environment [1]. Several solutions proposed in opening literatures [3]-[9] enable the ΔΣ modulator to operate at a very low supply voltage. Although voltage multipliers or bootstrapping switches can be applied easily and directly to conventional switched-capacitor circuits, the oxide breakdown issues will become more severe with continuously reduced channel length. Besides, due to the unavailable and expensive of low-Vt processes, the switched-opamp technique [3] can be selected to realize a truly low voltage ΔΣ modulator.

In this paper, the modified switched-opamp technique [7]-[9] is adopted to realize a very low-voltage switched-capacitor bandpass ΔΣ modulator. Since the allowable settling time is limited by the additional turn-on time of off-state opamps, a two-path architecture [2] can be used to relax the speed requirement of circuits by a factor of two. The architecture of the proposed modulator will be discussed in Section II and the circuit implementation will be described in Section III. Measurement results are shown in Section IV. Finally, the conclusions are given in Section V.

II. Architecture of proposed modulator

Because of the very low supply voltage operation environment, the settling requirement of the modulator will become more severe. The N-path architecture or the double sampling architecture can relax the problem, but the latter makes the designing of resonators more difficult. Besides, the required opamps often need high gain and high bandwidth and they are not easily available in low-voltage design. Thus, a two-path architecture [1, 2] is adopted to allow the

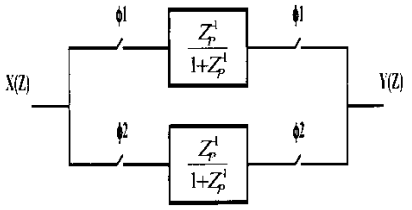

Figure 1 Two-path implementation of an fs/4 resonator

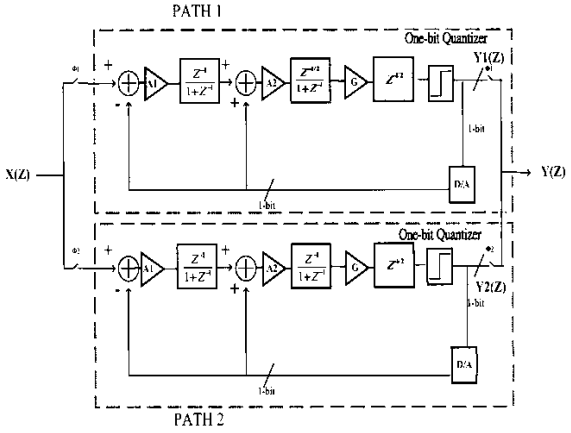

Figure 2 Low voltage two-path 4-th order bandpass modulator

modulator to operate at slower sampling rate than the overall throughput, which means the allowable settling time is doubled.
The fs/4 bandpass resonator can be partitioned into a two-path structure consisting of two identical highpass filters, as shown in Fig. 1, and the desired resonator transfer function, $H(Z)=AZ^{-2}/(1+Z^{-2})$, can be expressed as a function of Z_P in the following manner:

$$H(Z) = A\frac{Z^{-2}}{1+Z^{-2}} = A\frac{Z_P^{-1}}{1+Z_P^{-1}}\Big|_{Z_P=Z^2} \quad (1)$$

By using eqn. 1, a conventional bandpass ΔΣ modulator can be implemented by two identical paths which are controlled by two non-overlapping clocks. Since the low voltage comparator needs one-half clock cycle to completely process signals, the modulator is modified as shown in Fig. 2. The transfer function of the second highpass filter must be ahead one-half clock of the first one. Thus, the overall transfer function represented in z domain can be found

$$Y(Z)=\frac{A_1A_2GX(Z)(Z_P^{-1})^2+E(Z_P)(1+Z_P^{-1})^2}{1+(2-A_2G)Z_P^{-1}+(1+A_1A_2G-A_2G)Z_P^{-2}}\Big|_{Z_P=Z^2} \quad (2)$$

where G and E(Z) are the gain of comparator and quantization error, respectively.

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By setting the value of A_1, A_2, and G to be 0.5, 0.5, and 4, respectively, the transfer function can be approximated to

$$Y(Z) = Z^{-4}X(Z) + (1+Z^{-2})^2 E(Z) \qquad (3)$$

which is the same as that of conventional fourth-order, one-bit bandpass modulator. In this architecture, the proposed modulator can be implemented by highpass filters using switchable opamps, one-bit low voltage comparators, and DACs which are described in Section III. The modulator adopts a two-path architecture to relax the settling requirement and uses the modified switched opamp technique to eliminate all critical switches for very low supply voltage operation with any voltage multiplier.

III. Circuit Implementation

A. High pass filter

A traditional highpass filter requires the sampling phase (Φ1) to copy integrated charge form CF (CF') to CA (CA') and then transfers the charge to opposite input node of opamp during integrating phase (Φ2). Thus, it cannot be directly applied to the original switched-opamp technique. By adding the switchable opamp to process the signal during idle phase can solve the problem [8]. A low voltage version of the highpass filter using the technique is shown in Fig. 3. The transfer function of the highpass filter represented in z-domain can be

$$\frac{\tilde{v}_{out}^{+(1)} - \tilde{v}_{out}^{-(1)}}{\tilde{v}_{in}^{+(1)} - \tilde{v}_{in}^{-(1)}} = \frac{Z^{-1}}{1+Z^{-1}} \qquad (4)$$

and

$$\frac{\tilde{v}_{out}^{+(2)} - \tilde{v}_{out}^{-(2)}}{\tilde{v}_{in}^{+(1)} - \tilde{v}_{in}^{-(1)}} = \frac{Z^{-1/2}}{1+Z^{-1}} \qquad (5)$$

Because the modified switched opamp technique allows the output signals to be held during two clock phases, the two different highpass filters in Fig. 2 can be realized by eqns. 4 and 5, respectively.

B. Switchable opamp

In low-voltage design, stacked configurations must be avoided. Fig. 4 is the scheme of the switched opamp composed of four parts: input stage, level shifter, output stage, and the bias circuit. The input common mode voltage is set to ground and the two output pairs are controlled by two non-overlapped clock phases, respectively. The output common voltages are controlled by a modified common-mode feedback circuit. By choosing Cout1=Cout2=Cdc1=Cdc2, the common mode voltage of opamp can be controlled to Vdd/2. However, the turn-on time of the switched opamp limits the maximum operating frequency of the circuit. Here, four transistors, MA1~MA4, are added in two-output stages to reduce the opamp recovery time. The function of these transistors forces the drains of M10, M12, M14, and M16 to V_{DD} during the off phase. By doing so, the output stages are completely turned off and there is no current to discharge the compensation capacitors.

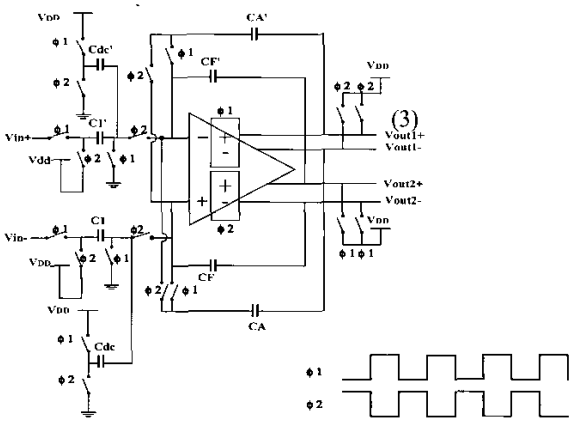
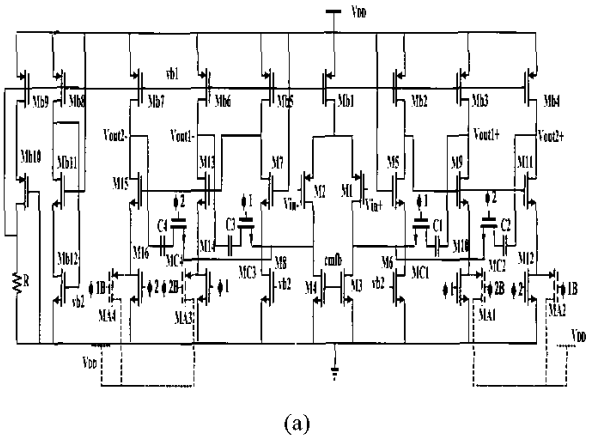


Figure 3 Low voltage highpass filter



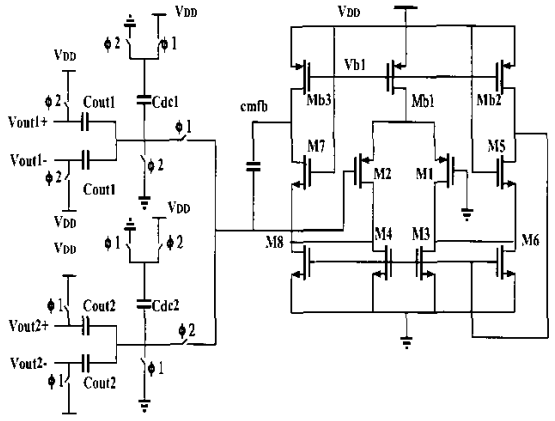


Figure 4 (a) Modified low voltage switchable opamp and (b) common-mode feedback circuit.

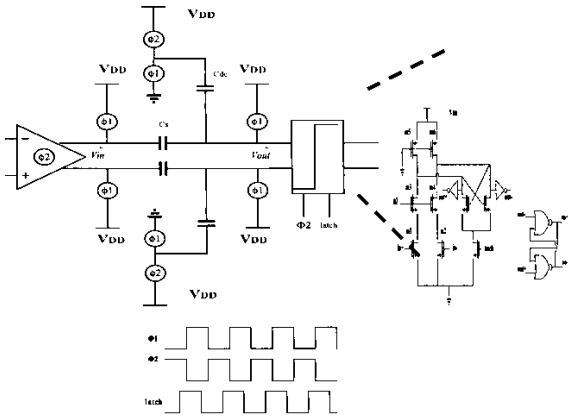


Figure 5 Low voltage comparator.

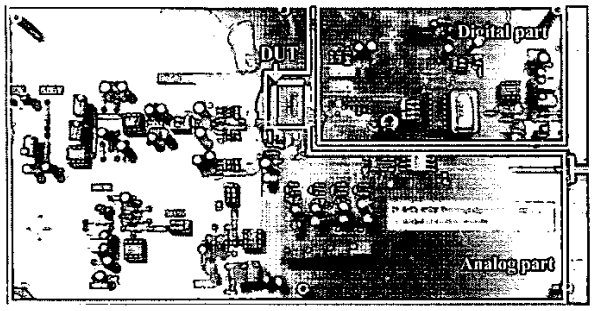


Figure 6 Photograph of the physical PCB.

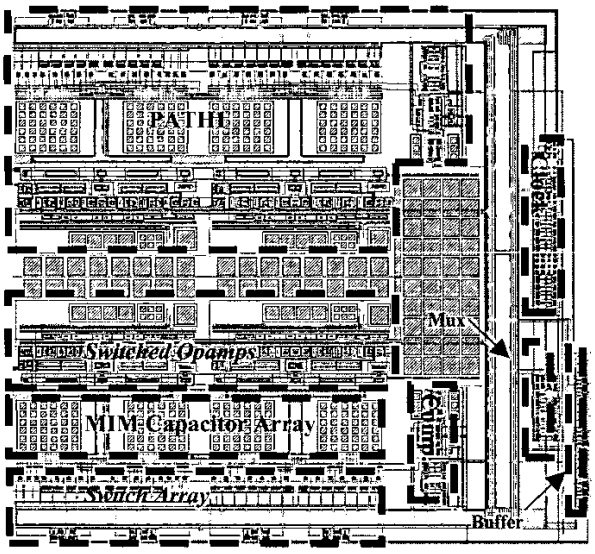


Figure 7 Layout of the prototype chip

C. Low voltage comparator

Since the output common mode voltage of the highpass filter is 0.4V, it is impossible to allow the conventional comparator to process signal at such low supply voltage without any additional circuits. A dynamic level shifter should be added in front of the latch comparator and the input common mode of comparator should be biased to V_{DD} or Gnd. Fig. 5 is a low voltage comparator [4]. During Φ1, the capacitor C_S is completely discharged while the capacitor Cdc is charged to V_{DD}. During Φ2, the output of the highpass filter is turned on while Cdc is completely discharged. From the law of charge conservation, the following relationships must hold in steady state.

$$Cs\{[(\frac{V_{DD}}{2}+\tilde{Vin})-(\tilde{Vout}+V_{DD})]-(V_{DD}-V_{DD})\}+ \quad (6)$$

$$Cdc\{[(V_{DD})-(\tilde{Vout}+V_{DD})]-(V_{DD}-V_{DD})\}=0$$

where $\tilde{Vin}$ and $\tilde{Vout}$ represent the small signal of input and output of level shifter, respectively. If Cs=2Cdc,

$$\tilde{Vout}=\frac{2}{3}\tilde{Vin} \quad (7)$$

Since the dynamic level shifter has a gain of 2/3, no inverse connection is needed between the level shifter and the comparator. The comparator is controlled by M3 and M4. During Φ2, the differential signals can be compared and then latched to the rails. At the end of Φ2, the compared signals are latched by a SR latch, which holds the data for a full clock cycle. The signal processing of the whole comparator requires one-half of clock cycle. Thus, the timing of the second highpass filter must be adjusted.

IV. Measurement Results

Fig. 6 shows the photograph of the physical PCB. The test board is separated into two parts, analog and digital, powered by different regulator circuits. Two separated grounds are connected by a bead inductor. The layout of the prototype chip is shown in Fig. 7, which is implemented with a 0.25-μm one-poly, five-metal standard CMOS process and occupies an active area of 2.1 mm^2. In typical case, the V_{TN} and V_{TP} of this process are 0.42 V and 0.48 V, respectively. The capacitors are realized by MIM capacitors and are arranged in a common-centroid structure to achieve matching. The modulator is operating at 0.8 V supply voltage and 5 MHz sampling rate. Applying –0.9 db input power relative to reference voltage, a peak SNDR of 60.6 db can be achieved. Fig. 8 is the measured dynamic range of the modulator. In comparison with the two results, although the performance of the modulator operating at 0.8 V supply voltage degrades a little performance but the power consumption is significantly decreased from 6.1 mW to 2.5 mW. A two-tone test is measured to determine the third inter-modulation (IM3) distortion. Fig. 9 shows an output spectrum with two frequency tones at 1.245 MHz and 1.255 MHz in which the resulting IM3 are 46 db below the amplitude of the two tones. Table 1 gives the performance summary.

V. Conclusions

A two-path fourth-order bandpass ΔΣ modulator operating at 0.8 V supply voltage has been proposed in this paper. Applying the

feature of two-path architecture relaxes the speed requirement of circuits by a factor of two. Meanwhile, the modified switched opamp technique is adopted to realize a truly low-voltage bandpass ΔΣ modulator without any voltage multiplier or bootstrapping switch. Due to no existing reliability problems, the proposed modulator is very suitable for the future advanced CMOS process and provides a great help for system integration.

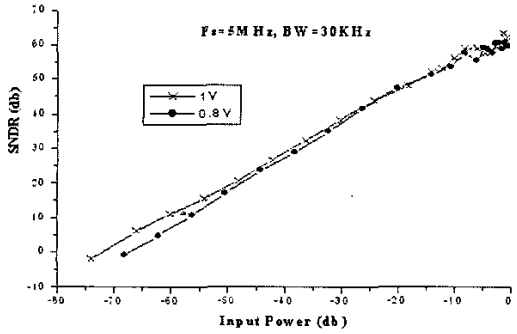


Figure 8 The measured SNDR

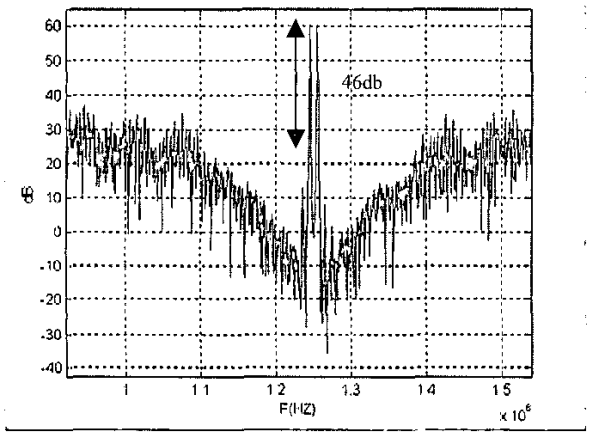


Figure 9 The two-tone test.

VI. References

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TABLE I: Performance summary of the proposed modulator

Architecture	Two-path architecture	
Order	4	
Sampling Frequency	5MHz	
OSR	83	
Signal Bandwidth	30KHz	
Input Range	0.5Vp-p	0.4Vp-p
Peak SNDR	63.5db	60.5db
Dynamic Range	72db	68db
Power dissipation	6.1mW	2.5mW
Power Supply	1.0V	0.8V
Active Area	2.1mm^2 (without pads)	
Technology	0.25μm CMOS, 1-poly 5-metal with MIM capacitors	