Boundary Scan for 5-GHz RF Pins Using LC Isolation Networks

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Abstract

The boundary-scan test provides a structural test solution for the densely packed digital electronics. For RF devices, the structural test also provides a good diagnostic resolution to the structural defects of RF circuits, especially for the high pin-count RF-SOCs. In this paper, the boundary-scan test is implemented on a 5-GHz RF pin using LC isolation networks to connect the RF lines and the boundary-scan cell, which isolates the RF circuitry from the digital boundary scan cell. This technique overcomes the parasitic loading problems and provides a minimum RF performance degradation to a RFIC. The measurement results show only 0.4-dB gain degradation in a 5-GHz amplifier with a boundary-scan cell and LC isolation networks.

1. Introduction

The boundary scan, IEEE standard 1149.1, is a design-for-testability standard to provide a test solution for the densely packed digital electronics [1]. Since the early 1990s, the extension of boundary-scan standard to cover microwave/RF devices has been discussed in many different publications [1]-[3]. In [2] and [3], the boundary-scan compliant digital signal processors (DSPs) in the baseband processor provide the means for the system controller to activate the functional test in RF sub-systems [2], or to activate the RF self-test [3]. The boundary-scan standard provides only an indirect testability to the RF devices in [2] and [3], which limits the resolution of RF diagnostics. To provide a structural test solution for RF circuits and increase the resolution of RF diagnostics, the boundary scan standard should be directly implemented on RF input and output ports.

There are many difficulties to perform boundary-scan tests on RF pins. The main reason is that adding additional test circuitry to the parasitic sensitive RF lines is not trivial and can easily degrade the RF performance of the RFICs [4]-[5]. Therefore, a RF isolation network is required to connect the RF lines and boundary-scan cell, which will overcome the previous parasitic loading problems and provide a minimum RF performance degradation to the RFIC.

The 5-GHz RF systems, like IEEE 802.11a, become popular in people's daily life. Due to the size reduction trend in wireless products, the RF designers have developed many highly integrated 5-GHz sytem-on-chip (SOC) [6], and system-on-package (SOP) [7] products. The test requirements of these 5-GHz RF-SOCs will include digital, analog, and RF tests all together. This paper utilizes a 5-GHz low-noise amplifier (LNA) [8] as an example to combine the boundary scan test with a 5-GHz RF input pin through an LC isolation network and demonstrates the feasibility of boundary scan for RF and analog pins. To the best of our knowledge, this is the first attempt to combine the boundary scan test with 5-GHz RF pins.

Most RF tests are placed within the functional tests or the parametric tests, which provide accurate RF performance tests, but have limited the resolution for RF diagnostics. The purpose of adding boundary-scan capabilities to the RF pins is to provide a fast structural test for the RF pins in an early manufacturing test stage. The boundary scan test for RF pins is like a complementary test to the RF functional test, which provides good diagnostic resolution to the structural defects of RF circuits. The RF boundary scan test can be implemented within the standard digital boundary scan test, and without any additional test procedures or expansive RF test equipment.

The module final test is a key contributor to the manufacturing cost for a packaged RFIC device [9]. Using boundary scan in RF pins can significantly increase the test coverage of RF circuits, and also improve the yield of the final functional test. The *test-earlier* strategy [10]-[11] is consistent with the proposed RF boundary scan in this paper, which can improve the final product yield and reduce production cost. Another concern with the RF boundary scan is that, adding additional test pins could significantly increase the die size or package size, which is not cost effective for most low-cost RFICs. Nevertheless, for the high pin-count RF-SOCs, like the 64-pin 5-GHz WLAN SOC [6], adding boundary scan pins will increase the total pin-count for less than 10%. In

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the future, many RF-SOCs will have more digital circuits inside, and the boundary scan pins can be used for both digital and RF boundary scan.

2. LC Isolation Networks

To overcome the parasitic loading problems and to minimize RF performance degradation to the 5-GHz LNA, an isolation network is required between the RF lines and the boundary scan cell (BSC). The most common isolation network in the microwave frequency is the RF choke, which is a large inductor. This inductor allows the boundary-scan low-frequency signal to pass, but blocks or isolates the RF signal from the BSC. Hence, for the 5-GHz in-band applications, no parasitics from BSC can affect the in-band RF performance. All the parasitics from BSC are isolated from the RF lines due to the LC isolation networks.

The LC isolation networks are implemented with a CMOS 0.35µm process. The spiral inductor with some parasitic capacitors and resistors needs an additional shunt capacitor to provide a better isolation. The RF isolation between the RF lines and the BSC is shown in Fig. 1. This simulation is based on 50 Ω input/output port impedance. For a real BSC cell using 0.35-µm CMOS, the port impedance will be much higher than 50 Ω. For higher impedance at BSC port, the isolation will be better than the isolation of 50 Ω port impedance. Hence the plot in Fig. 1 is the isolation of 50 Ω port impedance. For 5-GHz applications, the LC isolation networks consist of a 7.5-turn inductor and a 3.15 pF capacitor as the major parameters for the network.

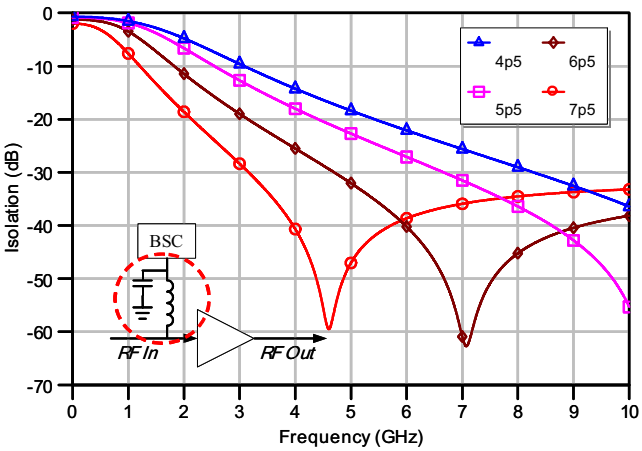


Fig. 1 The RF isolation between RF lines and boundary-scan cell (BSC) using LC isolation networks of a 3.15pF capacitor with different inductors of 4.5, 5.5, 6.5, and 7.5 turns. (assuming 50Ω input/output port impedance for the isolation study)

3. 5-GHz Amplifier Design

A 5-GHz amplifier [8] is used to demonstrate the feasibility of adding boundary-scan cell to 5- RF pins. This 0.35µm CMOS amplifier has two gain stages. Inductors are used as 5-GHz input/output matching networks. The LC networks are selected as a DC bias network, which allows only DC supply to pass the bias network. This bias network has a similar topology as our LC isolation networks, which provides a similar function to pass low-frequency boundary-scan signals only. Both networks block/isolate any RF noise from outside, and also keep the RF signal with minimal leakage to the outside.

The BSC cell design in the previous section can be used as a drop-in cell to the boundary-scan compliant amplifier design, as shown in Fig. 2. If the amplifier frequency is significantly different from the current design, then we need a different LC isolation network to cover a different frequency band.

The CMOS 0.35µm 5-GHz low-noise amplifier, in Fig. 2, is a two-stage design. The first stage is designed for noise performance, and the second stage is designed for gain. On-chip spiral inductors are used for matching, stability, and gain performance.

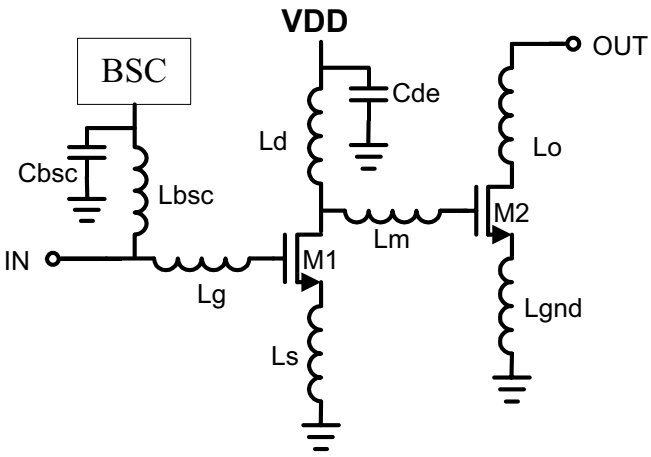
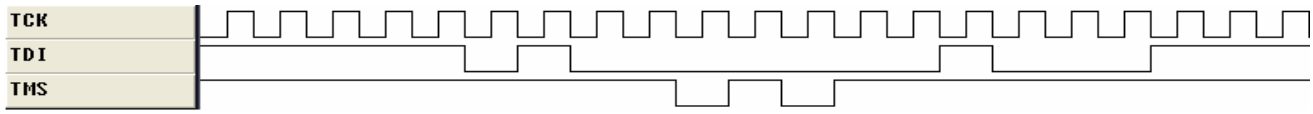


Fig. 2 Schematic of the boundary-scan compliant 5-GHz amplifier design.

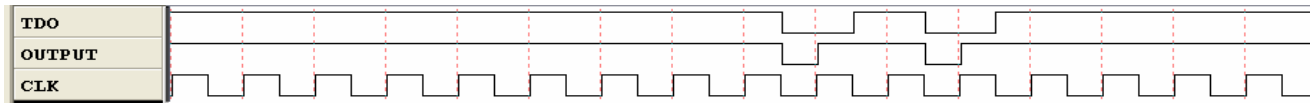
4. Digital Measurement

The 5-GHz boundary-scan compliant amplifier has two operation modes:

1) Test mode. The whole circuit in boundary scan test mode is for structural test only. During the test mode, the RF portion of the amplifier is off, and the BSC digital circuit block is powered on



(a)



(b)

Fig. 3 (a) Digital input pattern, clock rate is 50 kHz, (b) Digital output pattern, TDO (Test Data Out)
OUTPUT : BSC output pattern at RF pin when the amplifier is off and circuit is in test mode.

for receiving digital patterns and passing on patterns to next devices.

2) RF mode. The BSC digital circuit clock is powered off and no digital pattern is on the RF lines. The RF portion is powered on and the amplifier operates in its normal RF operational region. The LC isolation circuits will make the BSC 'invisible' (-40dB isolation) to the 5-GHz in-band signal.

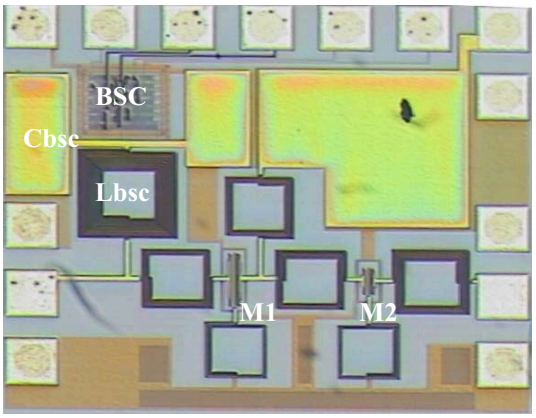


Fig. 4 Chip photo of the boundary-scan compliant 5-GHz amplifier design.

Fig. 3 shows the input digital pattern at TDI (Test Data In), TCK (Test Clock), and TMS (Test Mode Selection), and also the digital output pattern at TDO (Test Data Out), and the RF pin. The TDO signal has a similar output at the RF pin. This BSC test mode clock rate is 50 kHz.

Fig. 4 illustrates the chip-photo of the boundary-scan compliant 5-GHz amplifier. The physical size of this CMOS 0.35μm 5-GHz amplifier is 1.0 X 0.9 mm^2.

5. RF Measurement

Fig. 5 demonstrates the S-parameters of these two amplifiers, which have almost identical frequency responses between 5 and 6.5 GHz. At 5.8 GHz, the gain is not the highest peak, but it is the WLAN operation frequency with a low noise figure.

The RF performance of the boundary-scan compliant 5-GHz amplifier is measured and compared with the original 5-GHz amplifier without BSC, shown in Table I. The frequency is centered in the same 5.8 GHz. The gain has only 0.4-dB degradation, which is in the range of the process variations. It is noted that these two amplifiers are processed in different wafer lots. The return loss performance is also similar.

Table I. RF performance comparison between the 5-GHz amplifier with and without boundary-scan cell (BSC)/LC isolation networks

	Amplifier	Amplifier + BSC
Freq.	5.8 GHz	5.8 GHz
Gain	7.2 dB	6.8 dB
Input Return Loss	11 dB	11 dB
Output Return Loss	17 dB	16.7 dB

6. Conclusion

This paper demonstrates a boundary-scan compliant 5-GHz amplifier with 0.35µm CMOS technology. This amplifier implements the boundary-scan test on a 5-GHz RF pin using LC isolation networks to connect the RF lines and boundary-scan cell, which will isolate the RF circuitry from the digital boundary scan cell. This technique overcomes the parasitic loading problems and with minimum modification to the original circuits. The measurement results show only 0.4-dB gain degradation in a 5-GHz amplifier with a boundary-scan cell and LC isolation networks.

7. Acknowledgement

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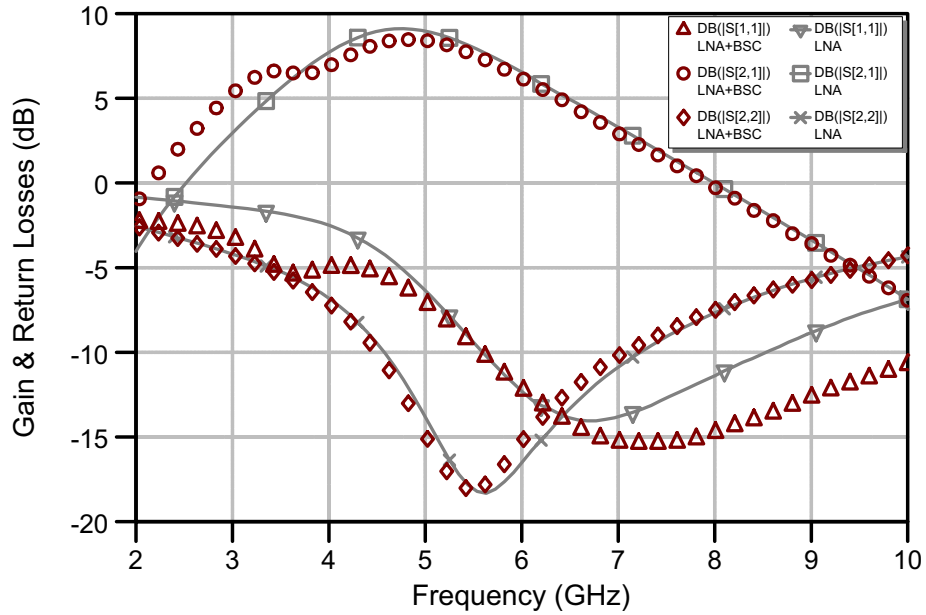

Fig. 5 RF measurements of the 5-GHz amplifier (LNA) with and without boundary-scan cell (BSC) and LC isolation networks.