Analysis of the Gate–Source/Drain Capacitance Behavior of a Narrow-Channel FD SOI NMOS Device Considering the 3-D Fringing Capacitances Using 3-D Simulation

Chien-Chung Chen, James B. Kuo, *Fellow, IEEE*, Ke-Wei Su, and Sally Liu

***Abstract*—This paper reports an analysis of the gate–source/drain capacitance behavior of a narrow-channel fully depleted (FD) silicon-on-insulator (SOI) NMOS device considering the three-dimensional (3-D) fringing capacitances. Based on the 3-D simulation results, when the width of the FD SOI NMOS device is scaled down to 0.05 μm, the inner-sidewall-oxide fringing capacitance (C_{FIS}), due to the fringing electric field at the edge of the mesa-isolated structure of the FD SOI NMOS device biased at $V_G = 0.3$ V and $V_D = 1$ V, is the second largest contributor to the gate–source capacitance (C_{GS}). Thus, when using nanometer CMOS devices with a channel width smaller than 0.1 μm, C_{FIS} cannot be overlooked for modeling gate–source/drain capacitance ($C_{\mathrm{GS}}/C_{\mathrm{GD}}$).**

***Index Terms*—Capacitance, CMOSFETs, modeling, silicon-on-insulator (SOI) technology, simulation.**

I. Introduction

SILICON-ON-INSULATOR (SOI) technology has been regarded as a major technology for integrating CMOS VLSI in the nanometer regime [1]. For small-geometry sub-100-nm SOI CMOS devices, narrow-channel effects are important in determining the performance [2], [3]. For analyzing the narrow-channel effects of a nanometer small-geometry device, three-dimensional (3-D) analysis is necessary, which is difficult to carry out. Compact modeling of the narrow-channel effects of the small-geometry fully depleted (FD) SOI CMOS devices in terms of the threshold voltage and the current conduction derived from 3-D analysis has been reported [4]–[6]. 3-D analysis of the source/drain capacitance of the small-geometry SOI CMOS devices has been done [7]. However, the gate–source/drain capacitance ($C_{\mathrm{GS}}/C_{\mathrm{GD}}$) behavior of a narrow-channel FD SOI NMOS device considering the 3-D fringing electric-field effects has not been reported. In fact, the 3-D fringing electric effects may bring impacts on the capacitance behavior substantially. In addition to the fringing electric field near the inner sidewall of the mesa-isolation structure in a narrow-channel FD SOI NMOS device, the fringing electric field in the source/drain sidewall is also important for affecting the device performance. In this paper, the $C_{\mathrm{GS}}/C_{\mathrm{GD}}$ behavior of a narrow-channel FD SOI NMOS device considering 3-D fringing electric-field effects is described. It will be shown that when the width of the FD SOI NMOS device is scaled down to below 0.1 μm, its gate–source/drain capacitance is substantially affected by the 3-D fringing electric-field-induced effects near the inner oxide sidewall and the source/drain sidewall. In the following sections, the capacitance behavior is described first, which is followed by discussion and conclusion.

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C.-C. Chen and J. B. Kuo are with the Department of Electrical Engineering, National Taiwan University, Taipei 106-17, Taiwan, R.O.C. (e-mail: jbkuo@cc.ee.ntu.edu.tw).

K.-W. Su and S. Liu are with the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu 300, Taiwan, R.O.C. (e-mail: s_liu@tsmc.com).

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II. Capacitance Behavior

Fig. 1 shows the 3-D cross section of the FD SOI NMOS device under study. It has a gate oxide of 5 nm, a thin film of 15 nm doped with a p-type doping density of 5×10^{17} cm^{-3}, a channel length of 0.18 μm, and a buried oxide of 400 nm. A mesa-isolation structure with the n$^+$ gate polysilicon covering a width-direction inner-sidewall oxide of 8 nm in thickness has been used. In order to facilitate analysis, next to the polysilicon gate, it is filled with oxide. A total of 17 640 grids have been generated for this device using a 3-D device simulator—Davinci [8]. Each set of the simulation for the $C_{\mathrm{GS}}/C_{\mathrm{GD}}$ of the device took about 190-min CPU time based on a 900MIPs workstation.

Fig. 2 shows the two-dimensional (2-D) electric-field contours in the $x - y$ and $y - z$ cross sections of the FD SOI NMOS device with a channel width of 0.1 μm biased at the drain voltage of $V_D = 1$ V and the gate voltage of $V_G = 1$ V. As shown in the $x - y$ cross section along the channel length direction (x-direction), the fringing electric field in the source and drain sidewalls is not negligible, which may affect $C_{\mathrm{GS}}/C_{\mathrm{GD}}$ substantially. In addition, in the $y - z$ cross section in the channel-width direction (z-direction) in the inner-sidewall oxide at the edge of the mesa-isolated structure, the fringing electric field is also not negligible, which may also affect $C_{\mathrm{GS}}/C_{\mathrm{GD}}$ to some extent. In the following analysis, an analysis in terms of the contributions from the fringing electric fields in the inner oxide sidewall and the source/drain sidewall to the

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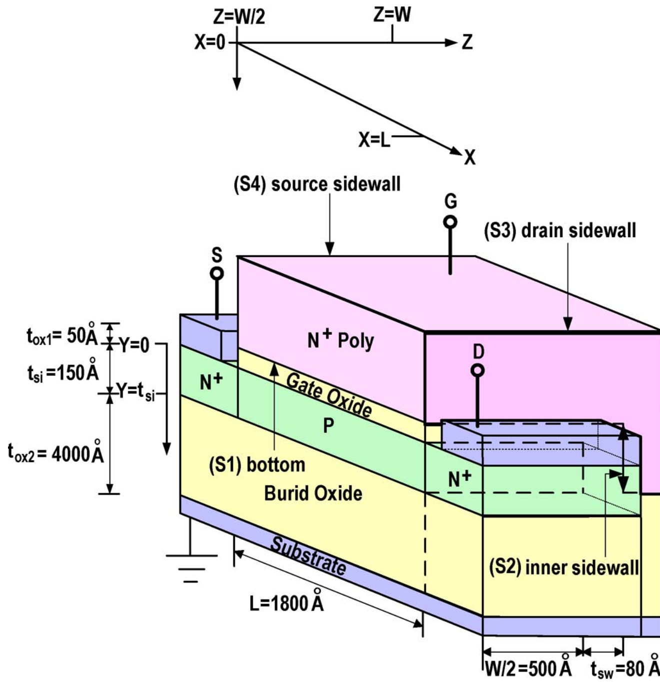


Fig. 1. Three-dimensional cross section of the mesa-isolated FD SOI NMOS device under study.

gate–source/drain capacitance of the narrow-channel FD SOI NMOS device is described.

As the $C_{\mathrm{GS}}/C_{\mathrm{GD}}$ is defined as the derivative of the gate charge with respect to the source/drain voltage $C_{\mathrm{GS}} = dQ_G/dV_S$, $C_{\mathrm{GD}} = dQ_G/dV_D$ [8], [9], where Q_G is the total gate charge. From Gauss' Law, the gate charge Q_G could be obtained by the surface integral of the displacement over the four surfaces of the poly gate—$(S1)$ is the bottom surface of the poly gate above the gate oxide, $(S2)$ is the inner surface next to the oxide sidewall, $(S3)$ is the right surface next to the drain sidewall, and $(S4)$ is the left surface next to the source sidewall as shown in Fig. 1. Thus, one obtains

$$Q_G = \iint_{S1} \epsilon_{\mathrm{ox}} E_y dx\, dz + \iint_{S2} \epsilon_{\mathrm{ox}} E_z dx\, dy + \iint_{S3} \epsilon_{\mathrm{ox}} E_x dy\, dz + \iint_{S4} \epsilon_{\mathrm{ox}} E_x dy\, dz \quad (1)$$

where x is in the lateral channel direction, y is in the substrate direction, and z is in the channel width direction. ϵ_{ox} is the oxide permittivity. E_y is the y-direction electric field at the bottom surface of the poly gate in the gate oxide $(S1)$. E_x is the x-direction electric field at right (drain) and the source (left) edge of the poly gate in the oxide side $(S3/S4)$. E_z is the z-direction electric field at the inner surface of the poly gate next to the oxide sidewall $(S2)$. From the above equation, the total gate charge Q_G can be expressed as the combination of the intrinsic gate charge (Q_I) in $S1$, the bottom of the poly gate, the inner-sidewall fringing gate charge (Q_{FIS}) in $S2$, the inner surface of the poly gate next to the oxide back sidewall, the drain-sidewall fringing gate charge (Q_{FDS}) in $S3$ and the source sidewall fringing gate charge (Q_{FSS}) in $S4$. Therefore, one obtains

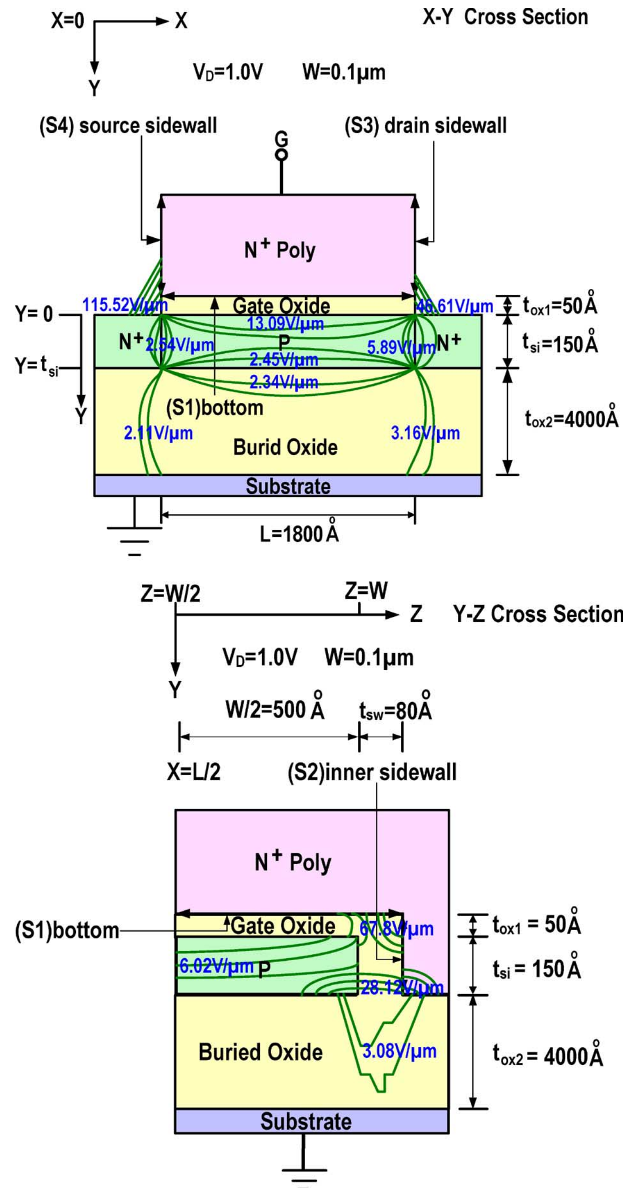
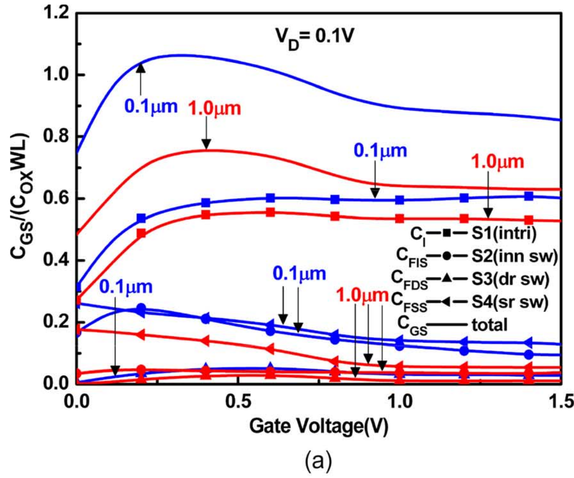


Fig. 2. 2-D electric-field contours in the $x-y$ and $y-z$ cross sections of the FD SOI NMOS device with a channel width of 0.1 μm, biased at $V_G = 1$ V and $V_D = 1$ V.

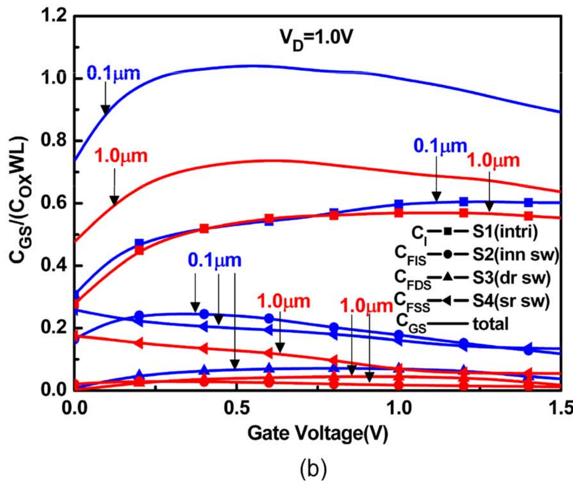
$$C_{\mathrm{GS}} = C_I + C_{\mathrm{FIS}} + C_{\mathrm{FDS}} + C_{\mathrm{FSS}} \quad (2)$$

where the intrinsic gate capacitance in $S1$ is defined as the derivative of the intrinsic gate charge with respect to the source voltage: $C_I = dQ_I/dV_S$. The inner oxide sidewall fringing capacitance in $S2$ is defined as: $C_{\mathrm{FIS}} = dQ_{\mathrm{FIS}}/dV_S$. The drain-sidewall fringing capacitance in $S3$ is defined as $C_{\mathrm{FDS}} = dQ_{\mathrm{FDS}}/dV_S$. The source sidewall fringing capacitance in $S4$ is defined as $C_{\mathrm{FSS}} = dQ_{\mathrm{FSS}}/dV_S$. By the same token, the gate-drain capacitance could be defined in a similar way as

$$C_{\mathrm{GD}} = C'_I + C'_{\mathrm{FIS}} + C'_{\mathrm{FDS}} + C'_{\mathrm{FSS}} \quad (3)$$

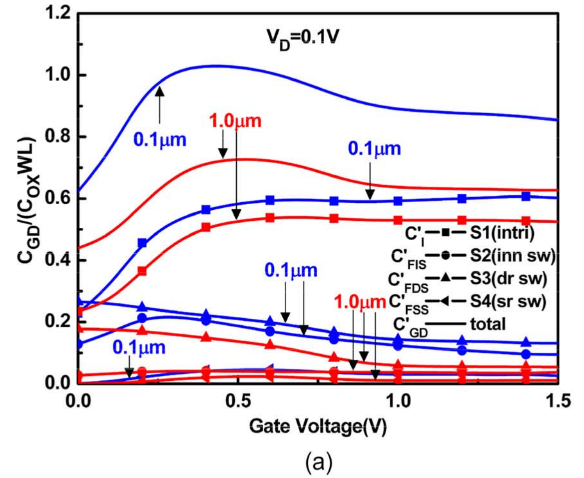


(a)

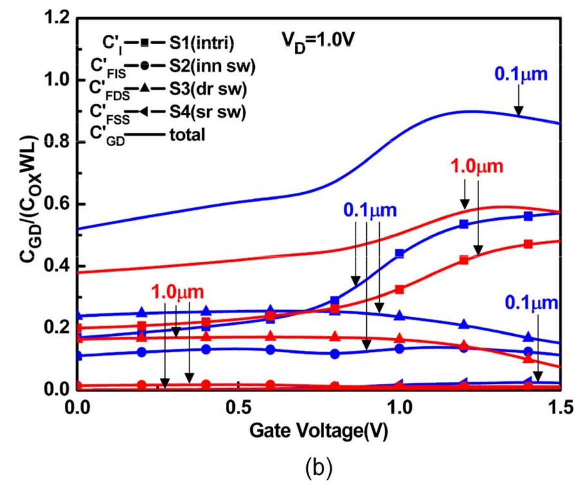


(b)

Fig. 3. Gate–source capacitance ($C_{\rm GS}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of (a) 0.1 V and (b) 1 V, considering the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C_{\rm FSS}$).



(a)



(b)

Fig. 4. Gate-drain capacitance ($C_{\rm GD}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of (a) 0.1 V and (b) 1 V, considering the contributions from $S1$—the intrinsic gate capacitance (C'_I), $S2$—the inner-sidewall fringing capacitance ($C'_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C'_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C'_{\rm FSS}$).

where $C'_I = dQ_I/dV_D$, $C'_{\rm FIS} = dQ_{\rm FIS}/dV_D$, $C'_{\rm FDS} = dQ_{\rm FDS}/dV_D$, and $C'_{\rm FSS} = dQ_{\rm FSS}/dV_D$. Thus, via carrying out the differentiation of the integral of the charge in four surfaces $(S1 - S4)$ of the poly gate at different biasing voltages based on the Davinci simulation results, the gate–source/drain capacitance of the device has been found.

Fig. 3 shows the gate–source capacitance $(C_{\rm GS})$ versus the gate voltage (V_G) of the mesa-isolated narrow-channel FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 0.1 V [Fig. 3(a)] and 1 V [Fig. 3(b)]. Note that $C_{\rm GS}$ has been normalized by the $WLC_{\rm ox}$ of the device, where W/L is the channel width/length and $C_{\rm ox}$ is the unit-area gate-oxide capacitance. As shown in the figures, the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance $(C_{\rm FIS})$, $S3$—the drain-sidewall fringing capacitance $(C_{\rm FDS})$, and $S4$—the source sidewall capacitance $(C_{\rm FSS})$ are also plotted. Fig. 4 shows the gate-drain capacitance $(C_{\rm GD})$ versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 0.1 V [Fig. 4(a)] and 1 V [Fig. 4(b)]. Note that various contributions–C'_I, $C'_{\rm FIS}$, $C'_{\rm FDS}$, and $C'_{\rm FSS}$–are also included. As shown in Fig. 3, with a narrower channel width (0.1 μm), the intrinsic gate capacitance (C_I) due to the electric field in $S1$ at the bottom of the poly gate becomes larger as compared to the 1-μm case due to the fringing electric field at the edges of the intrinsic gate region. With a narrower channel width (0.1 μm), the inner-sidewall fringing capacitance $(C_{\rm FIS})$ due to the electric field in $S2$, the inner back sidewall is also larger. A similar trend exists for the drain/source sidewall fringing capacitance $(C_{\rm FDS}/C_{\rm FSS})$ due to the electric field in $S3/4$—the drain/source sidewall. The source sidewall fringing capacitance $C_{\rm FSS}$ is greater than the drain-sidewall fringing capacitance $C_{\rm FDS}$. Considering the three fringing capacitances–$C_{\rm FIS}$, $C_{\rm FDS}$, $C_{\rm FSS}$–and the intrinsic gate capacitance (C_I), the total gate–source capacitance $C_{\rm GS}$ is larger for the case with a smaller channel width of 0.1 μm. As shown in Fig. 3, the intrinsic gate capacitance (C_I) is larger than the inner-sidewall fringing capacitance $(C_{\rm FIS})$. Among three fringing components, both the source sidewall fringing capacitance $(C_{\rm FSS})$ and the inner-sidewall capacitance $(C_{\rm FIS})$ are the dominant factors. As shown in Fig. 4, the contributions of the three fringing capacitances to $C_{\rm GD}$ are similar except

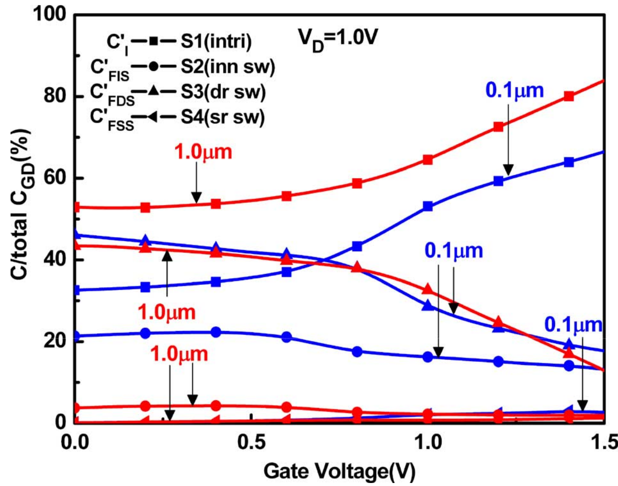


Fig. 5. Percentage contributions to the gate-drain capacitance ($C_{\rm GD}$) from $S1$—the intrinsic gate capacitance in the bottom of the poly gate (C'_I), $S2$—the inner-sidewall fringing capacitance ($C'_{\rm FIS}$), $S3$—the drain-sidewall capacitance ($C'_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C'_{\rm FSS}$) versus the gate voltage (V_G) of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 1 V.

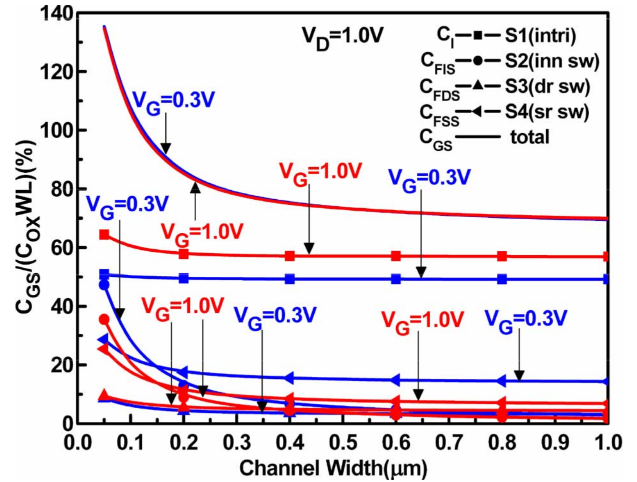


Fig. 6. Gate–source capacitance ($C_{\rm GS}$) versus channel width of the FD SOI NMOS device biased at $V_D = 1$ V and $V_G = 0.3$ V and 1 V, considering the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C_{\rm FSS}$).

that the source sidewall fringing capacitance ($C'_{\rm FSS}$) is smallest. From Figs. 3 and 4, the 3-D fringing electric-field effects are important while considering $C_{\rm GS}/C_{\rm GD}$ of a narrow-channel FD SOI NMOS device. From the 3-D simulation analysis, the importance of the 3-D fringing electric-field effects, especially the fringing electric-field effects in the source/drain sidewall as well as that in the inner oxide sidewall, has been observed. Note that the influence of $C_{\rm FSS}/C'_{\rm FSS}$ and $C_{\rm FDS}/C'_{\rm FDS}$ depends on the choice of the sidewall structure, which is determined by technology considerations.

III. Discussion

More insight into the relative importance of the fringing capacitances could be obtained by studying the percentage contributions to $C_{\rm GD}$ from $S1$—the intrinsic gate capacitance (C'_I), $S2$—inner-sidewall capacitance ($C'_{\rm FIS}$), $S3$—the drain-sidewall capacitance ($C'_{\rm FDS}$), and $S4$—the source sidewall capacitance ($C'_{\rm FSS}$) versus the gate voltage of the mesa-isolated FD SOI NMOS device with channel widths of 0.1 and 1 μm, biased at V_D of 1 V, as shown in Fig. 5. In general, the intrinsic gate capacitance (C'_I) always dominates the gate-drain capacitance ($C_{\rm GD}$). With a narrower channel width, the dominance of the intrinsic gate capacitance recesses, indicating the more influence of the fringing capacitances. When the gate voltage is smaller, C'_I from $S1$ becomes less important in contributing to $C_{\rm GD}$, and $C'_{\rm FDS}$ from $S3$ becomes more important. With a narrower channel width of 0.1 μm, the contribution of $C'_{\rm FDS}$ from $S3$ is even higher than that of C'_I in $S1$. At V_G of 0.3 V, $C'_{\rm FDS}$ occupies 43% of the total $C_{\rm GD}$ while C'_I does only 33%. In addition, $C'_{\rm FIS}$ from $S2$ rises to 22%. This implies that the fringing electric field in $S2$ (the inner-sidewall oxide at the edge of the mesa-isolated structure) and $S3$ (the drain sidewall) dominates $C_{\rm GD}$.

Fig. 6 shows $C_{\rm GS}$ versus channel width of the FD SOI NMOS device, biased at $V_D = 1$ V and $V_G = 1$ V and 0.3 V.

C_{GS}

Length 0.18μm	Width	C_I(S1)	C_{FIS}(S2)	C_{FDS}(S3)	C_{FSS}(S4)
V_D=0.1V V_G=0.5V	0.1μm	57.29%	18.24%	4.89%	19.58%
	0.18μm	64.82%	11.90%	4.50%	18.78%
	1.0μm	73.61%	5.55%	3.81%	17.03%

(a)

C_{GS}

Length 90nm	Width	C_I(S1)	C_{FIS}(S2)	C_{FDS}(S3)	C_{FSS}(S4)
V_D=0.1V V_G=0.5V	0.1μm	56.59%	16.65%	6.36%	20.40%
	1.0μm	74.23%	6.06%	4.98%	14.73%

(b)

Fig. 7. Contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall fringing capacitance ($C_{\rm FSS}$) to the gate–source capacitance ($C_{\rm GS}$) of the FD SOI NMOS device (a) with a channel length of 0.18 μm and channel widths of 0.1, 0.18, and 1 μm and (b) with a channel length of 90 nm and channel widths of 0.1, and 1 μm, biased at $V_D = 0.1$ V and $V_G = 0.5$ V.

As shown in the figure, when the channel width is greater than 0.4 μm, $C_{\rm GS}$ and all components–C_I, $C_{\rm FIS}$, $C_{\rm FDS}$, and $C_{\rm FSS}$–are almost constant, insensitive to variation in channel width. When the channel width is scaled down to below 0.1 μm, all contributing components–the inner-sidewall-oxide fringing capacitance ($C_{\rm FIS}$), the source sidewall fringing capacitance ($C_{\rm FSS}$), the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and the gate intrinsic capacitance (C_I)–increase due to the more fringing electric field. As a result, the total $C_{\rm GS}$ may exceed 100% of $WLC_{\rm ox}$. Specifically, with a channel width of 0.05 μm, the inner-sidewall-oxide fringing capacitance ($C_{\rm FIS}$) occupies 35% of the total $C_{\rm GS}$, only next to the gate intrinsic capacitance (C_I), which occupies 37.5%, followed by

the source sidewall fringing capacitance ($C_{\rm FSS}$) with 21.1%, and the drain-sidewall fringing capacitance ($C_{\rm FDS}$) with 6.4%. Therefore, the importance of the fringing electric field in the inner-sidewall at the edge of the mesa-isolated structure cannot be overlooked while using the nanometer CMOS devices with a channel width of smaller than 0.1 μm. Fig. 7 shows the contributions from $S1$—the intrinsic gate capacitance (C_I), $S2$—the inner-sidewall fringing capacitance ($C_{\rm FIS}$), $S3$—the drain-sidewall fringing capacitance ($C_{\rm FDS}$), and $S4$—the source sidewall fringing capacitance ($C_{\rm FSS}$) to the gate–source capacitance ($C_{\rm GS}$) of the FD SOI NMOS device, with a channel length of 0.18 μm and channel widths of 0.1, 0.18, and 1 μm [Fig. 7(a)] and with a channel length of 90 nm and channel widths of 0.1 and 1 μm, biased at $V_D = 0.1$ V and $V_G = 0.5$ V [Fig. 7(b)]. As shown in Fig. 7(a), when the channel width is scaled down, the contribution from $S2$–the inner-sidewall fringing capacitance ($C_{\rm FIS}$)–increases from 5.55% at $W = 1$ μm to 11.9% at $W = 0.18$ μm and 18.24% at $W = 0.1$ μm. As shown in Fig. 7(b), with a smaller channel length of 90 nm, $C_{\rm FIS}$ increases from 6.06% at $W = 1$ μm to 16.65% at $W = 0.1$ μm. Thus, a smaller channel width leads to a more contribution of the inner-sidewall fringing capacitance ($C_{\rm FIS}$) to the gate–source capacitance ($C_{\rm GS}$).

IV. Conclusion

In this paper, an analysis of the $C_{\rm GS}/C_{\rm GD}$ behavior of a narrow-channel FD SOI NMOS device considering the 3-D fringing capacitances has been reported. Based on the 3-D simulation results, when the width of the FD SOI NMOS device is scaled down to 0.05 μm, the $C_{\rm FIS}$, due to the fringing electric field at the edge of the mesa-isolated structure of the FD SOI NMOS device biased at $V_G = 0.3$ V and $V_D = 1$ V, is the second largest contributor to the $C_{\rm GS}$. Thus, when using nanometer CMOS devices with a channel width smaller than 0.1 μm, $C_{\rm FIS}$ cannot be overlooked for modeling $C_{\rm GS}/C_{\rm GD}$.

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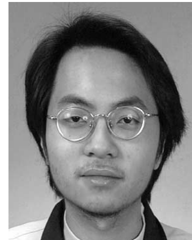


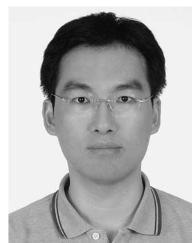
Chien-Chung Chen was born in Taoyuan, Taiwan, R.O.C., in June 19, 1981. He received the B.S.E.E. degree from National Cheng-Kung University, Tainan, Taiwan, R.O.C. in 2003 and the M.S.E.E. degree from National Taiwan University, Taipei, Taiwan, R.O.C. in 2006.

His research topic is in the simulation and modeling of CMOS VLSI devices.

James B. Kuo (M’85–SM’92–F’00) received the Ph.D.E.E. degree from Stanford University, Stanford, CA, in 1985.

From 1985 to 1987, he was a Research Associate with Integrated Circuit Lab, Stanford University. Since 1987, he has been with National Taiwan University, Taipei, Taiwan, R.O.C., where he is currently a Professor. Between 2000 and 2002, he was a Professor with the University of Waterloo, Waterloo, ON, Canada. Between 2004 and 2005, he was with the Simon Fraser University in Canada. His research expertise is in the field of low-voltage CMOS VLSI circuits and compact modeling of CMOS VLSI devices. He has published 300 technical papers and authored 8 textbooks on CMOS VLSI. He has graduated 80 graduate students specialized in CMOS VLSI working in leading microelectronics companies.

Dr. Kuo served as the Vice President of membership for the IEEE Electron Devices Society. He was awarded the Prestigious Canada Research Chair on Low-Voltage CMOS VLSI by NSERC.



Ke-Wei Su was born in Tainan, Taiwan, R.O.C., on February 23, 1973. He received the B.S. and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, Taiwan, R.O.C., in 1994 and 1998, respectively.

In 2001, he joined the SPICE group of the Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C. His current focus is on compact modeling of MOSFETs for both bulk and silicon-on-insulator technologies.

Sally Liu received the B.S. and M.S. degrees in physics and applied physics, respectively, from National Tsing-Hua University, Hsinchu, Taiwan, R.O.C., and the Ph.D. degree in electrical engineering and computer science from University of California, Berkeley.

Since 2004, he has been the Director of Advanced Technology Modeling Division with Taiwan Semiconductor Manufacturing Company (TSMC), Hsinchu, Taiwan, R.O.C. Prior to this, she spent 15 years with AT&T Bell Laboratories, 6 years with Conexant/Rockwell Semiconductors, and 2 years with RF Integrated Corporation. She has been engaged in the research and development of device modeling and simulation, circuit simulation and optimization, statistical modeling and design centering, circuit verification, IP characterization, and EDA framework.