Modelling and controller design of inductor-coupled multimodule DC–DC convertor with master–slave current-comparing scheme

R.-T. Chen and Y.-Y. Chen

Abstract: The paper proposes a novel multimodule parallel structure with coupled inductor and common filter. The design and implementation of a three-module parallel push–pull convertor system is presented. In parallel operation, a master–slave current-comparing scheme is proposed to compensate the mismatch in current-control characteristics of each parallel convertor. First, the small-signal equivalent circuit and transfer-function model of the multimodule convertor system are found. Then the model reduction is performed using the concept of dominant energy mode. Based on the reduced convertor model, a PI controller is quantitatively designed according to the prescribed regulating specifications. The performance of the convertor and the effectiveness of the proposed controller are demonstrated by some simulation and experimental results.

1 Introduction

Power requirements for large commercial and military systems such as large computer and electronic systems, ships and aircraft, telecommunications etc. are increasing and becoming more complex as systems compete for more data-computing and data-retrieval capability at higher speeds and lower costs. Power-supply systems must be increasingly reliable and efficient, and load power-density requirements are increasing as well. Present and future system power requirements are for five or more voltages, including new lower voltages as microprocessor (CPU) speed and power increase and operating voltages decrease to the 1–3 V level with higher currents and higher di/dt load steps, together with tighter voltage-regulation tolerances. Production of high currents with a single convertor raises problems such as heat dissipation, expensive high-power components and failure protection. A better method of meeting these demands is to employ several individual convertors that share the load requirements. Multimodule parallel DC–DC convertor systems [1, 2] are an interesting solution to the problem of providing a tightly regulated output voltage at high currents. Cascading of convertor stages reduces the conversion ratio of each stage, while paralleling allows sharing of the output current between modules. With such solutions, modularity of the power system is achieved by simply adding or removing power modules, depending on the power level.

Multimodule operation of convertors has the following advantages:

(i) The convertors can be designed in modular fashion, and thus the system power capacity can easily be enlarged by increasing the number of parallel convertors.

(ii) The system reliability is greatly increased.

(iii) With appropriate configuration arrangement and operation management, the overall power-conversion efficiency and the life of convertor can be increased.

(iv) With an appropriate phase shift among the switching sequence of convertor modules, the switching ripples of the individual convertor modules cancel each other, greatly reducing the input and output ripple. For a high-performance multimodule parallel convertor system, in addition to good current-sharing properties, good output-voltage-regulating performance is indispensable. During recent years, although research on the multimodule parallel operation for switching-type convertors has been carried out by some authors [2–7, 10–14], dynamic modelling, controller design and implementation for inductor-coupled parallel push–pull convertors with master–slave current-comparing scheme are still seldom performed.

To ensure uniform distribution of stresses, the total load current should be shared equally among the convertors. Many schemes can be used to achieve current sharing. Active current sharing ensures near-perfect current distribution without the disadvantages of the droop method such as degraded output-voltage regulation, requiring voltage references etc. [10]. The active current-sharing scheme of the 'master–slave' approach requires a 'current-sharing bus' to transfer/share certain common information [11, 12]. The objective of shared information among convertors is to determine the deviation of the individual output current from the desired value. In this paper, a novel master–slave current control of an instantaneous average-current-sharing scheme with a coupled inductor of output filter is presented. The output current of each slave module is compared with that of a master module; the regulated current-error signal is then used to modify the control signal of the respective slave module. If the current controllers in the inner loop are designed properly, each slave convertor current can closely track that of the master convertor in both the transient and static periods. In case the load current harmonics will be reduced, it is desirable to meet the stringent ripple and noise specifications. An efficient secondary LC filter can be

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The authors are with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.

E-mail: rtchen@ipmc.ee.ntu.edu.tw

designed to provide good attenuation of the switching ripple, while maintaining adequate stability margins under a wide range of capacitive loadings. The instantaneous current-sharing scheme has very good performance in both current sharing and voltage regulation. However, interconnections between the convertors are necessary. This limits the flexibility of the multimodule system and degrades the system's redundancy. Based on the proposed current-control technique, the outer-loop-voltage controller can be designed using an equivalent single-module model. Both the current convertor and the voltage controller are designed using the proposed systematic procedures according to the prescribed specifications. Although the multimodule parallel system analysed in this paper is a push–pull convertor, this control method is applicable to any other type of DC–DC convertor. The analytical study is validated for three parallel push–pull convertors. It can be augmented to n models. The simulated and measured results show that good current-sharing and output-voltage-regulating characteristics are obtained by the proposed convertor system.

2 Multimodule convertor with master–slave current-comparing system

The structures of multimodule parallel convertors have been treated just like two-port network connections in various papers [2, 5, 10–14]. The circuit characteristics will be limited by the primitive convertor. It causes the damage of circulation current between convertors because of the difference in the convertor parameters and control is then difficult. This paper presents a novel parallel structure with coupled inductors and a common filter. The proposed three-module paralleled push–pull convertor systems is shown in Fig. 1. The energy-storage elements are coupled together. The filter capacitor uses only one component for the three-convertor system. This is the main difference in the power circuit from therein other papers. Further, this paper presents another novel multimodule control scheme with two loops of inner current loop and outer voltage loop. This scheme has still seldom been proposed in other papers.

Figure 1 shows a schematic diagram of a three-module convertor system. The system consists of three push–pull convertor modules in parallel with a common coupled-inductor LC filter and an output-voltage-feedback circuit G_v. Each convertor module contains a power stage, a pulse-width-modulation (PWM) block, and two feedback circuits: GI, the current sensing network, for the inductor-current feedback and G_v for the capacitor-voltage feedback from the power stage. Each single module will reserve the original convertor characteristics in Fig. 1. The weight and volume of the parallel system will be reduced by the integrated magnetics and common filter. Another benefit is that the

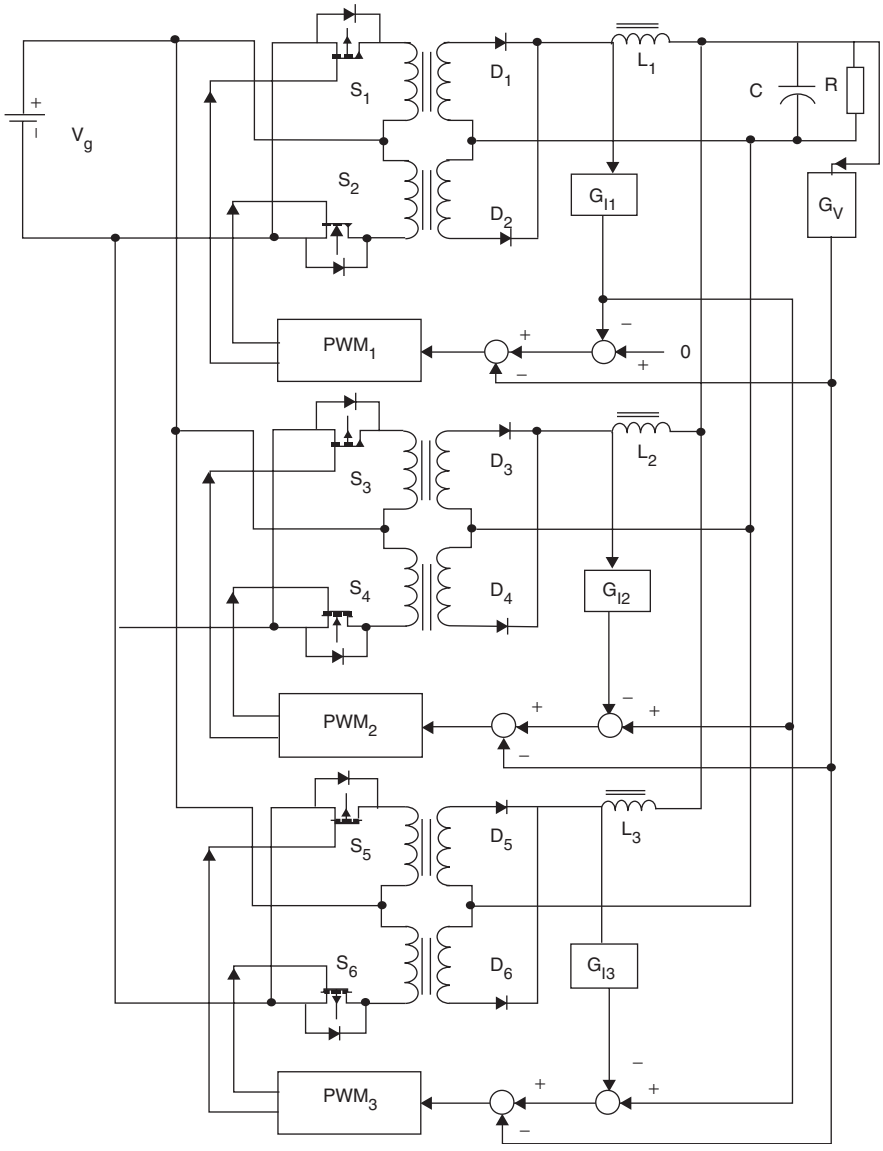


Fig. 1 *Three-module push–pull convertors with master–slave current-comparing control system*

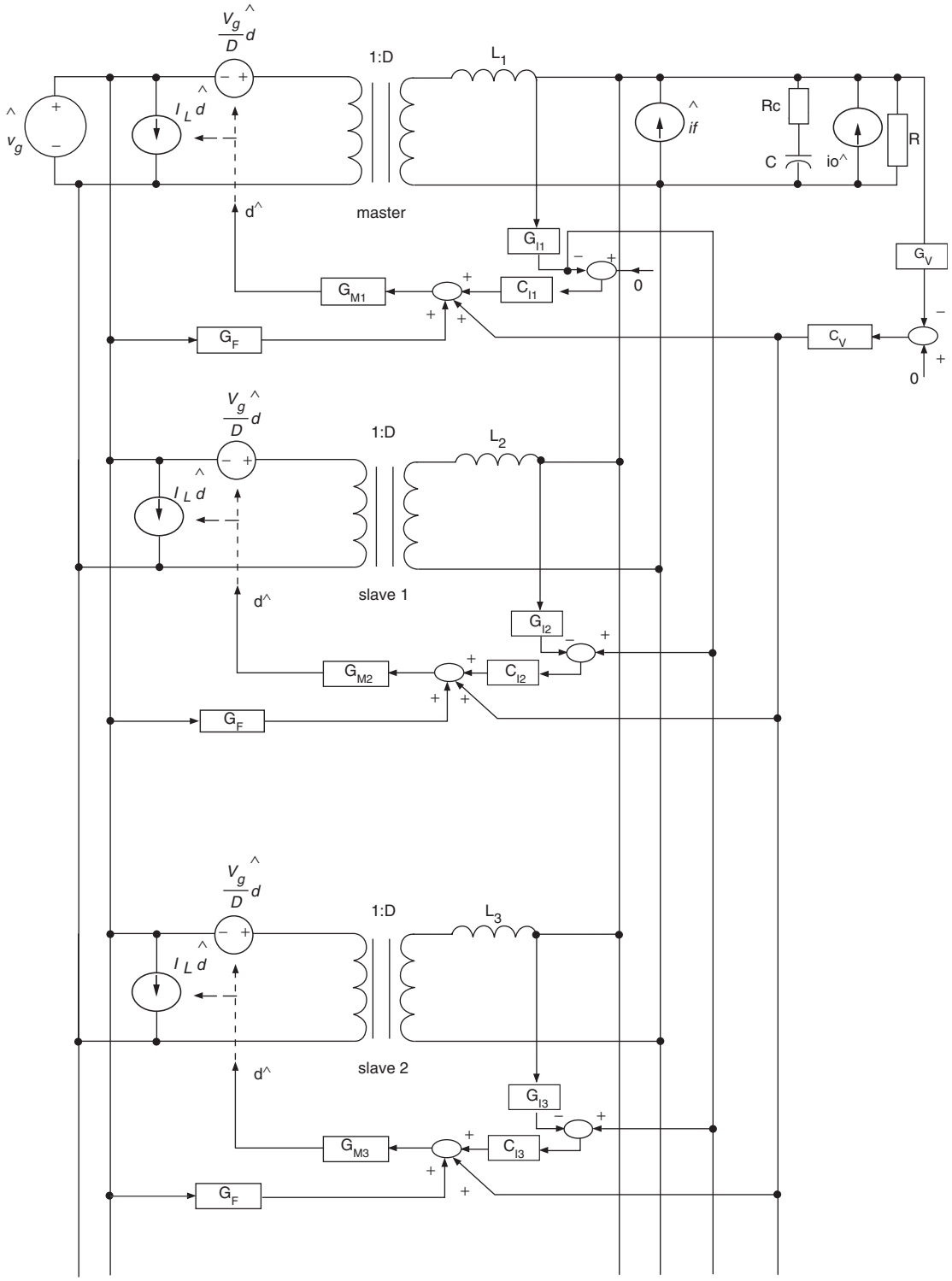


Fig. 2 *Equivalent small-signal models of the proposed system*

coupling circuits identify the parallel branch voltage and current in nature. The disadvantage is reduced flexibility and reliability.

The control structure proposed in Fig. 1 is a master–slave current-comparing scheme. It is different from the master–slave current-sharing scheme in [13]. Master–slave current-sharing circuits with a 'current share bus' are needed in that paper. In the absence of this bus, any imbalance in the convertor parameters will cause oscillation interaction and drop-out. The bus power dissipation and circuit complex are its defects. In Fig. 1 the master–slave current-comparing scheme is different from the master–slave current-sharing scheme because of the lack of current-sharing bus. The inner current loop is sensing from each module inductor and then comparing with each other. The scaling master-module inductor current is directly connected to the PWM control circuit for the inner-current control loop. The output current of each slave module is compared with that of a master module; the regulated-current error signal is then used to modify the control signal of the respective slave module. By designing properly the current controllers in inner loop, one can arrange that each slave convertor current can closely track that of the master convertor in both the transient and static periods.

In the proposed scheme, the outer loop is a voltage-regulation control loop. Generally, the response of the inner

current loop is faster than that of the outer voltage loop. For simplicity, the two compensation controllers will be designed separately in Section 3. When the master module breaks down, the slave module works independently with the current inner-loop control itself and the outer voltage-control loop still works normally. Thus, the current-averaging function will lose its effectiveness. This is the defect of the master–slave current-comparing scheme. Fortunately, the currents of the remaining slave modules are still determined by the proposed power circuit. It will maintain the averaging-shunt-current characteristics by way of the common coupled inductor. Another disadvantage of the proposed multimodule system is that the number of modules is limited by the integrated magnetics of the coupled inductors. This is acceptable in the trade off between power capacity and economy.

3 Dynamic modeling of proposed multimodule system

In this Section, a model of a three-parallel-push–pull-convertor system is proposed for the purpose of performance and controller design. The small-signal model for the three-module parallel-convertor system with master–slave current-comparing scheme is built in Section 3.1, which is used for the open-loop analysis in Section 3.2.

3.1 Small-signal model of the system

The small-signal equivalent circuit is derived using the technique proposed by [3, 4]. By replacing the convertor with the state-averaged PWM switch model and employing the sampled-data mechanism to describe the switching inductor current, we have the small-signal equivalent circuit shown in Fig. 2. The modulator gain (GM) of the PWM block is given by [4], and GF represents the feedforward gain from the input voltage. Then the current-sensing networks are replaced by a single gain block given by G_{Ii}, $i=1,2,3$. Finally the current and voltage controllers are represented by C_{Ii} and C_v, respectively.

The disturbance of the small-signal model will take into account:

(i) Input voltage variation $\hat{v}_g$: for current-mode-controlled convertors, the input voltage feedforward is automatically provided and thus the effect of $\hat{v}_g$ will be neglected in the current controller design.

(ii) Duty ratio variation $\hat{d}_k$: the control variable $\hat{d}_k$ is derived from the three feedback signals $\hat{v}_R$, $\hat{v}_L$, $\hat{i}_{Lk}$, $(k=1,2,3)$, which will be referred to as remote voltage, local voltage and inductor current, respectively.

(iii) Output-load current variation $\hat{i}_o$: for quantitatively specifying the dynamic response, it is typical to consider the output-voltage response due to a step load-current change.

(iv) Intermodule current variation $\hat{i}_f$: the effect of $\hat{i}_f$ on the output voltage response is quite similar to that of $\hat{i}_o$. It follows that $\hat{i}_f$ is also neglected in the controller design stage.

To characterise the module-failure response systematically, a transfer function called transimpedance is defined as $A_i = \hat{v}_R/\hat{i}_f$, representing the output-voltage response due to the current disturbance coming from the convertor modules. The other closed-loop performances include control-to-output transfer function: $A_c \equiv \hat{v}_R/\hat{d}$; line-to-output transfer function (audiosusceptibility): $A_g \equiv \hat{v}_R/\hat{v}_g$; and output-impedance function: $Z_o \equiv \hat{v}_R/\hat{i}_O$.

The principal variables used in this paper are defined in Table 1.

3.2 Open-loop analysis

From the small-signal equivalent circuit of Fig. 2, one can derive the transfer-function block diagram as shown in Fig. 3, i.e.

$$
\begin{aligned}
F_1(s) &= \frac{nD(1+sCR_c)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_2(s) &= \frac{sL(1+sCR_c)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_3(s) &= \frac{sL(1+sCR_c)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_4(s) &= \frac{nV_g(1+sCR_c)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_5(s) &= (\frac{nD}{R})\frac{(1+sC_R)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_6(s) &= \frac{-(1+sCR_c)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_7(s) &= \frac{-(1+sCR_c)}{s^2LC + s(\frac{L}{R}+CR_c)+1}\\
F_8(s) &= (\frac{nVg}{R})\frac{(1+sC_R)}{s^2LC + s(\frac{L}{R}+CR_c)+1}
\end{aligned}
\tag{1}
$$

where R_c is the equivalent series resistance (ESR) of the capacitor C and $L = L_1//L_2//L_3$.

Suppose that the multimodule convertor system consists of three single identical modules; we then find that

Table 1: Principal symbols used in the paper

V_g	steady-state input voltage	$\hat{i}_f$	intermodule current variation	R_c	equivalent series resistance (ESR) of the capacitor
$\hat{v}_g$	input-voltage variation	$\hat{v}_c$	control-current signal	f_s	switching frequency $T_s = 1/f_s$
$\hat{v}_R$	output-voltage variation	D	duty ratio	G_M	gain of the modulator $G_M = 1/(m_c\, S_n\, T_s)$
$\hat{i}_L$	inductor-current variation	n	turns ratio of the output transformer	S_n	sensed ramp $S_n = n^2\, k\, (1-D)\, V_g\, R_i/L$
$\hat{i}_o$	output-current variation	k	turns ratio of the current sensor	S_e	external stabilisation ramp
$\hat{d}$	duty-ratio variation	R_i	resistance used to translate the sensed current to voltage signal	m_c	degree of the slope compensation $m_c = 1 + S_e/S_n$

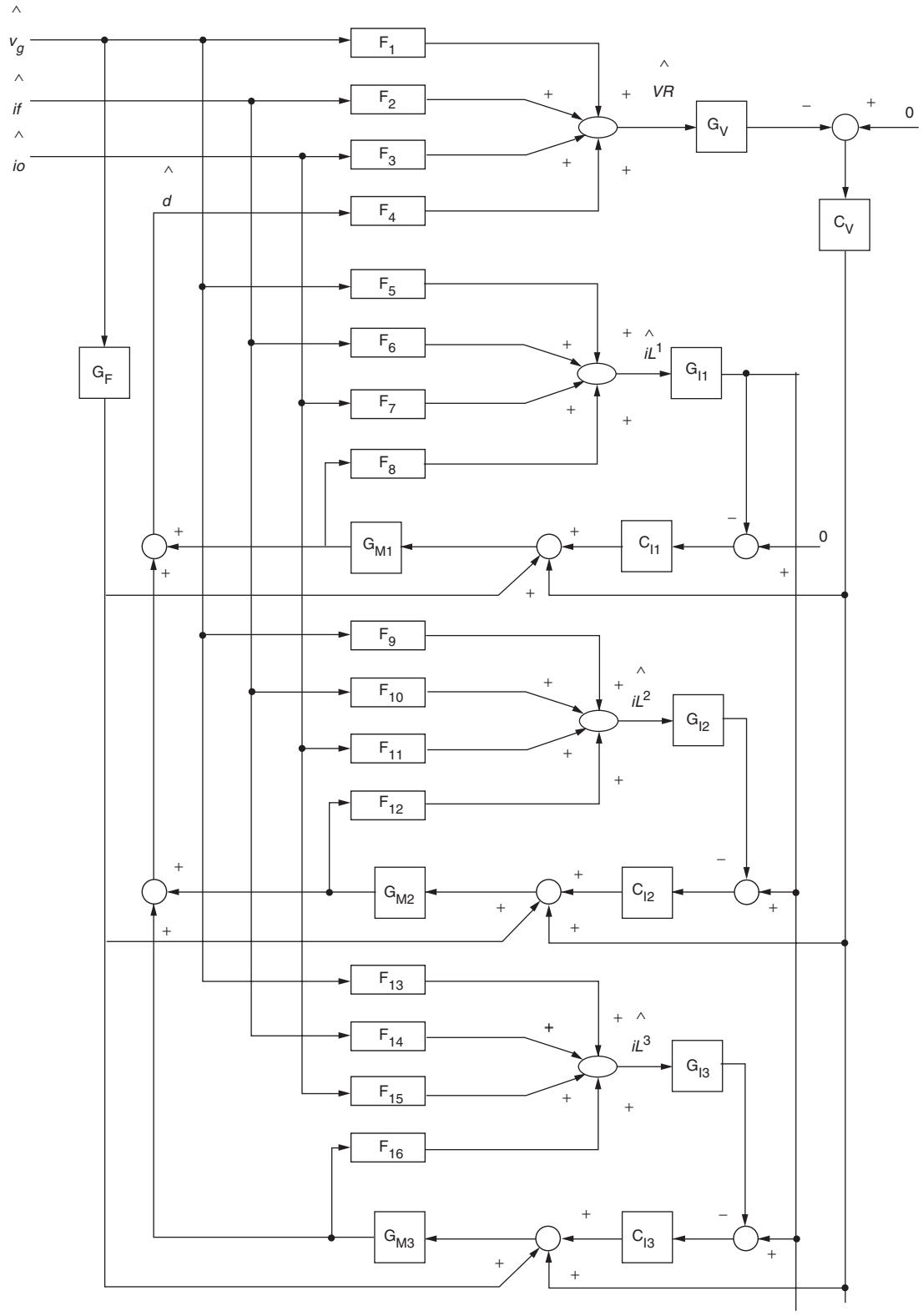


Fig. 3 *Small-signal block diagram of the proposed system*

$F_5 = F_9 = F_{13}$, $F_6 = F_{10} = F_{14}$, $F_7 = F_{11} = F_{15}$ and $F_8 = F_{12} = F_{16}$. For convenience in controller design, the interesting transfer function of the block diagram in Fig. 3 can be derived by Manson's formula. First, one can find eight loops in Fig. 3, i.e.

$$
\begin{aligned}
P_1 &= -F_4\, G_v\, C_v\, GM_1 \\
P_2 &= -F_4\, G_v\, C_v\, GM_2 \\
P_3 &= -F_4\, G_v\, C_v\, GM_3 \\
P_4 &= -F_8\, GI_1\, CI_1\, GM_1 \\
P_5 &= -F_{12}\, G_{I2}\, C_{I2}\, GM_2 \\
P_6 &= -F_{16}\, GI_3\, CI_3\, GM_3 \\
P_7 &= -F_4\, G_v\, C_v\, GM_1\, F_8\, GI_1\, CI_2\, GM_2 \\
P_8 &= -F_4\, G_v\, C_v\, GM_1\, F_8\, GI_1\, CI_3\, GM_3
\end{aligned}
\tag{2}
$$

Then, from Fig. 3, the relationship of loops may be defined by Manson's formula as the polynomials

$$X(S) \equiv 1 - \sum_{j=1}^{8} P_j + (P_1P_5 + P_1P_6 + P_2P_4 + P_2P_6 + P_3P_4 + P_3P_5 + P_4P_5 + P_4P_6 + P_5P_6 + P_5P_8 + P_6P_7) - (P_1P_5P_6 + P_2P_4P_6 + P_3P_4P_5 + P_4P_5P_6 + P_5P_6P_8) \quad (3)$$

$$Y(S) \equiv 1 - \sum_{j=4}^{6} P_j + (P_4P_5 + P_4P_6 + P_5P_6) - (P_4P_5P_6) \quad (4)$$

Thus, from the previous definition we can derive the transfer functions A_c, A_g, A_i and Z_o as follows:

$$A_c \equiv \frac{\hat{v}_R}{\hat{d}}\Big|(\hat{v}_g = \hat{i}_o = \hat{i}_f = 0) = \frac{F_4Y(S)}{X(S)} \quad (5)$$

$$A_g = \frac{\hat{v}_R}{\hat{v}_g}\Big|\left(\hat{d} = \hat{i}_o = \hat{i}_f = 0\right) = \frac{F_1Y(S)}{X(S)} \quad (6)$$

$$Z_o = \frac{\hat{v}_R}{\hat{i}_o}\Big|\left(\hat{v}_g = \hat{d} = \hat{i}_f = 0\right) = \frac{F_3Y(S)}{X(S)} \quad (7)$$

$$A_i = \frac{\hat{v}_R}{\hat{i}_f}\Big|\left(\hat{v}_g = \hat{i}_o = \hat{d} = 0\right) = \frac{F_2Y(S)}{X(S)} \quad (8)$$

4 Multimodule operation of proposed system

From previous analysis, A_c, A_g, A_i and Z_o are all sixth-order transfer functions. To simplify the controller design, model reduction is indispensable. It is known that the frequency-domain characteristics of PWM are dependent on the degree of slope compensation m_c, as indicated in Table 1 [3]. By selecting the value of m_c properly, one can much enhance the operating stability of the convertor system. In this paper, the concept of dominant energy mode proposed in [8] is used to determine the slope compensation and used to find the reduced models of the convertor. Detailed derivation of the model reduction by power decomposition can be referred to in [8]; only a brief description is included in the Appendix (Section 9). The results show that A_c, A_g, A_i and Z_o can be approximated by first-order models for the proper selection of m_c. The Bode plots of these transfer functions also confirm these characteristics at low frequencies.

In Section 4.1 and 4.2 a controller of reduced model without and with on inner-loop current loop is built. In Section 4.3, an input-voltage feedforward controller is discussed.

4.1 Module-parallel-without-inner-loop current control

The circuit configuration of the parallel-convertor system, which consists of N models, is shown in Fig. 2, where the control voltage v_e generated from a voltage controller is common for all modules. Since the effect of input-voltage variation $\hat{v}_g$ is much smaller than that of the output current $\hat{i}_o$, it is neglected in the controller design introduced here. Accordingly, a transfer-function block diagram is drawn in Fig. 4 from Fig. 3 where C_v is a voltage feedback controller. The current-sharing property is described as follows.

Suppose convertor 1 in Fig. 2 is regarded as the master convertor; the current ratio of the ith slave module to the master module can be found as

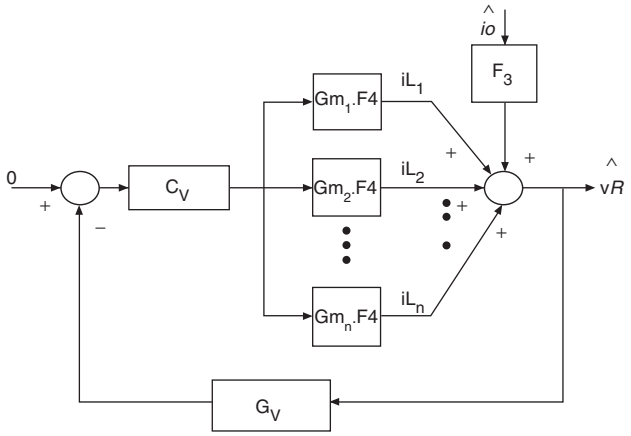


Fig. 4 *Closed-loop transfer-function block diagram for n parallel convertors without current control*

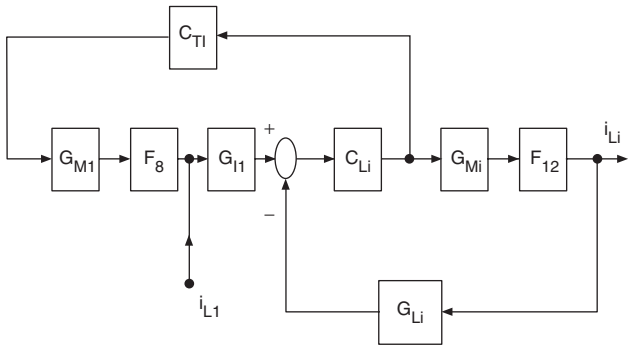


Fig. 5 *Closed-loop transfer-function block diagram for any $i = 2, 3, \ldots, n$ parallel-convertor system with current control*

$$\kappa_{\mathrm{Ii}} \equiv \frac{\hat{i}_{Li}}{\hat{i}_{L1}} = \frac{G_{m_i}}{G_{m_1}} = 1 - \frac{\Delta G_{m_i}}{G_{m_1}} \quad i = 2, 3, \ldots, N \quad (9)$$

where $G_{m_i} \equiv G_{m_1} + \Delta G_{m_i}$ is assumed and ΔG_{m_i} denotes the mismatch between G_{m_1} and G_{m_i}. The ratio of current-sharing mismatch between the ith slave module and the master module to the total current can further be found to be

$$\kappa_{Ti=} \frac{(\hat{i}_{Li} - \hat{i}_{L1})}{\sum_{i=1}^{N} i_{Li}} = \frac{\Delta G_{m_i}}{\sum_{i=1}^{N} G_{m_i}} \quad (10)$$

If only two modules are parallel and ΔG_{m_2} is within $\pm 10\%$ of G_{m_1} due to the variations of capacitor C, then from (10) the maximum value of κ_{T2} is 5.26%. In practice, this is in the acceptable range. The maximum value of κ_{Ti}, $i = 2, 3, \ldots, N$ will be decreased as the number of paralleled convertors is increased.

The controller C_v shown in Fig. 4 is the PI controller

$$C_v(s) = \frac{k_P s + k_I}{s}$$

The closed-loop transfer function of $\hat{v}_R$ to $\hat{i}_o$ is derived from Fig. 4 as

$$Z_c(s) \equiv \frac{\hat{v}_R}{\hat{i}_o} = \frac{F_3}{1 + G_vC_vF_4(G_{m1} + G_{m2} + \ldots + G_{mn})} \quad (11)$$

For evaluating the regulating performance, according to (11) and the prescribed specifications, the parameters k_p and k_I of the voltage controller C_v can be found by numerical computation.

4.2 Module-parallel-with-inner-loop current control

To achieve more accurate dynamic current-sharing characteristics, an average current-control technique is proposed in Fig. 5, where C_{Ii}, $i=2,3,\ldots,N$ are the current controllers for the ith slave module. The average current for each module is obtained by coupling the inductor current and filtering by the lowpass filter G_{Ii}. The error of average currents of the ith slave module and master module is regulated through the current controller C_{Ii}, and the resulted signal is augmented to the control signal $\hat{v}_c$, which is then sent to adjust the output current of the ith slave module. The effect of input-voltage variation $\hat{v}_g$ is also neglected here.

Since the response speed of the inner current loop is much faster than that of the outer voltage loop, the outer loop is neglected in the design stage of current controller C_{Ii}. The design of C_{Ii}, PI controller can be treated as the tracking problem. From Fig. 5 one can derive the ratio of these two currents as

$$\kappa_{1i} \equiv \frac{\hat{i}_{Li}}{\hat{i}_{L1}} \equiv \frac{C_{Ii}\, G_{Mi}\, G_{I1}\, F_8}{1 + C_{Ii}\, G_{Mi}\, G_{Ii}\, F_8} \quad i = 2, 3, \ldots, N \qquad (12)$$

where the transfer functions $F_8 = F_{12} = F_{16} = \ldots$ for each slave module.

By specifying the desired response

$$C_{\mathrm{Ii}}(s) = \frac{k_{pi}s + k_{Ii}}{s}$$

can be found, and then k_{pi} and k_{Ii} , $i=2,3,\ldots,N$ are all successfully designed.

4.3 Consideration of the input voltage feedforward controller

Generally, complete elimination of the effect of input-voltage variation under various operating conditions is impossible, although the effect of input-voltage variation on the output voltage is much smaller than that of load current and it is neglected in the design of feedback controllers. The feedforward controller GF shown in Fig. 3 can be augmented to reduce its effect. Since $G_{M1} \simeq G_{M2} \simeq \ldots \simeq G_{Mn}$, if all the inner-loop current controllers are properly designed, the controller G_F can be found [9] to be

$$G_F = M/G_{M1} \qquad (13)$$

where M is the convertor gain and G_{M1} is the master-modulator gain.

5 Design of proposed parallel convertor system

A prototype of the three-module parallel push–pull convertor has been built to verify the theoretical results. The power-circuit specifications are designed in Section 5.1. Then Section 5.2 proposes a reduced model with and without inner-loop current control. Based on the reduced model, a PI controller is designed quantitatively according to the prescribed regulating specifications.

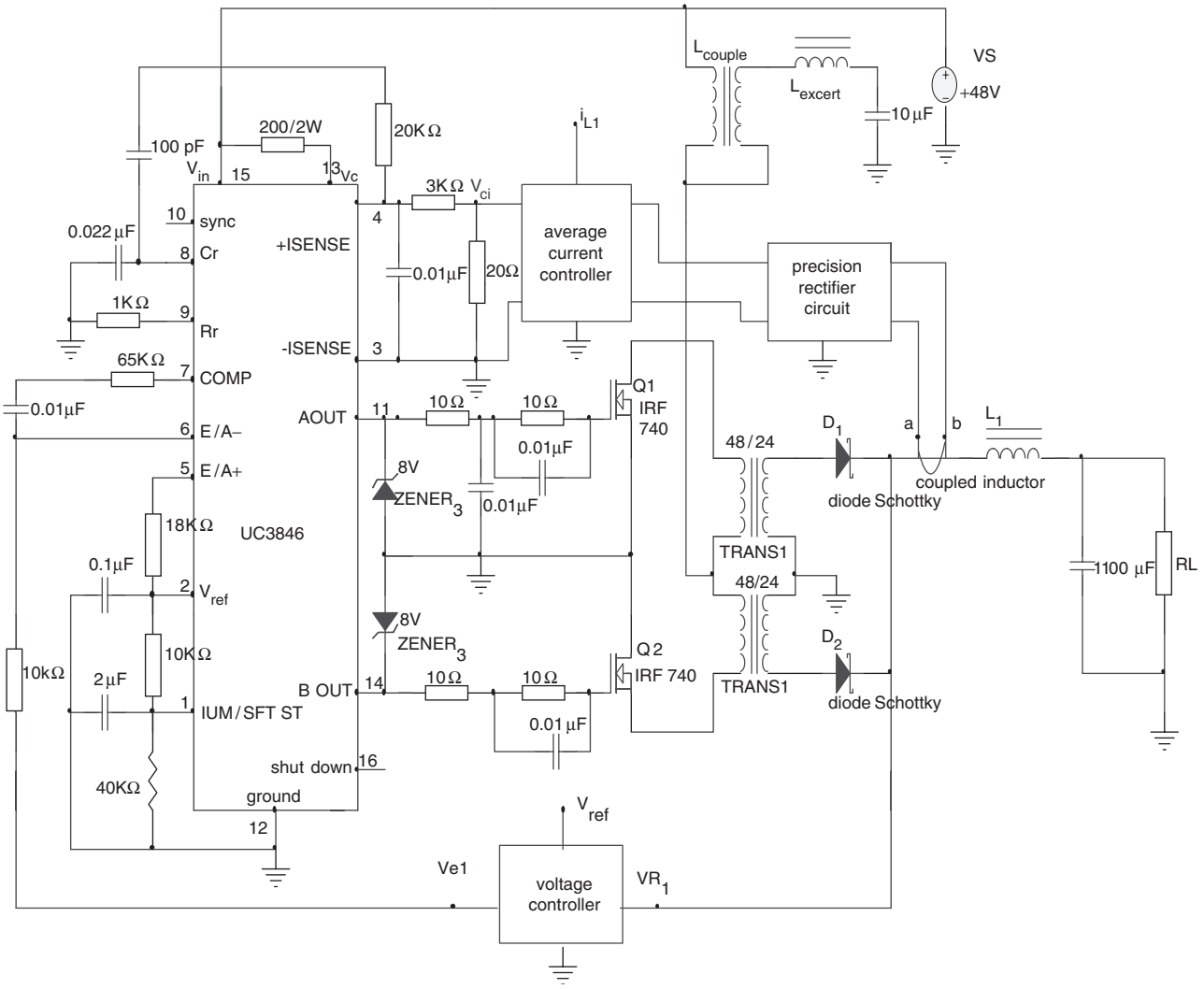


Fig. 6 *Configuration of the proposed single-module convertor*

Applying the model-reduction technique proposed in [8], the reduced models at the nominal case can be found. MATLAB Simulinks are used to verify the results. The simulated results indicate that the unit-step responses of the reduced models are very close to that of the actual sixth-order transfer functions.

5.1 Power circuit

The push–pull convertor is adopted in this paper to study the modelling and controller design of a multimodule parallel-convertor system, as shown in Fig. 1. The single-module circuit configuration of the proposed convertor is shown in Fig. 6. All the magnetic components are integrated in a single core, giving a smaller size, weight and lower core losses. This topology also provides a built-in input filter, and thus a smooth input current. The integrated circuit UC3846 is used for the PWM controller. The sensed inductor current is added with a stabilising current ramp for slope compensation. This compensated current is then compared with the regulated voltage-error signal to perform the master–slave current-comparing control.

The three-module push–pull convertor system was implemented as shown in Fig. 1, with one module output power $P_o = 80\,W$ and switching frequency $f_s = 120\,kHz$. The power stage consists of the following components; switches S_1–S_6: power MOSFET's IRF 740; parallel switch diodes: HFA08TB60; diodes D_1–D_6: HFA15TB40; coupling inductor $L_1 = L_2 = L_3 = 120\,\mu H$; core: TDK EI 35; each transformer $N_{p1} = N_{p2} = 48$ turns; $N_{s1} = N_{s2} = 24$ turns; $N_{L1} = N_{L2} = N_{L3} = 18$ turns; load R: $5\,\Omega$; and output capacitor C: $1100\,\mu F$. The other parameters of the experimental three-module parallel-convertor system are

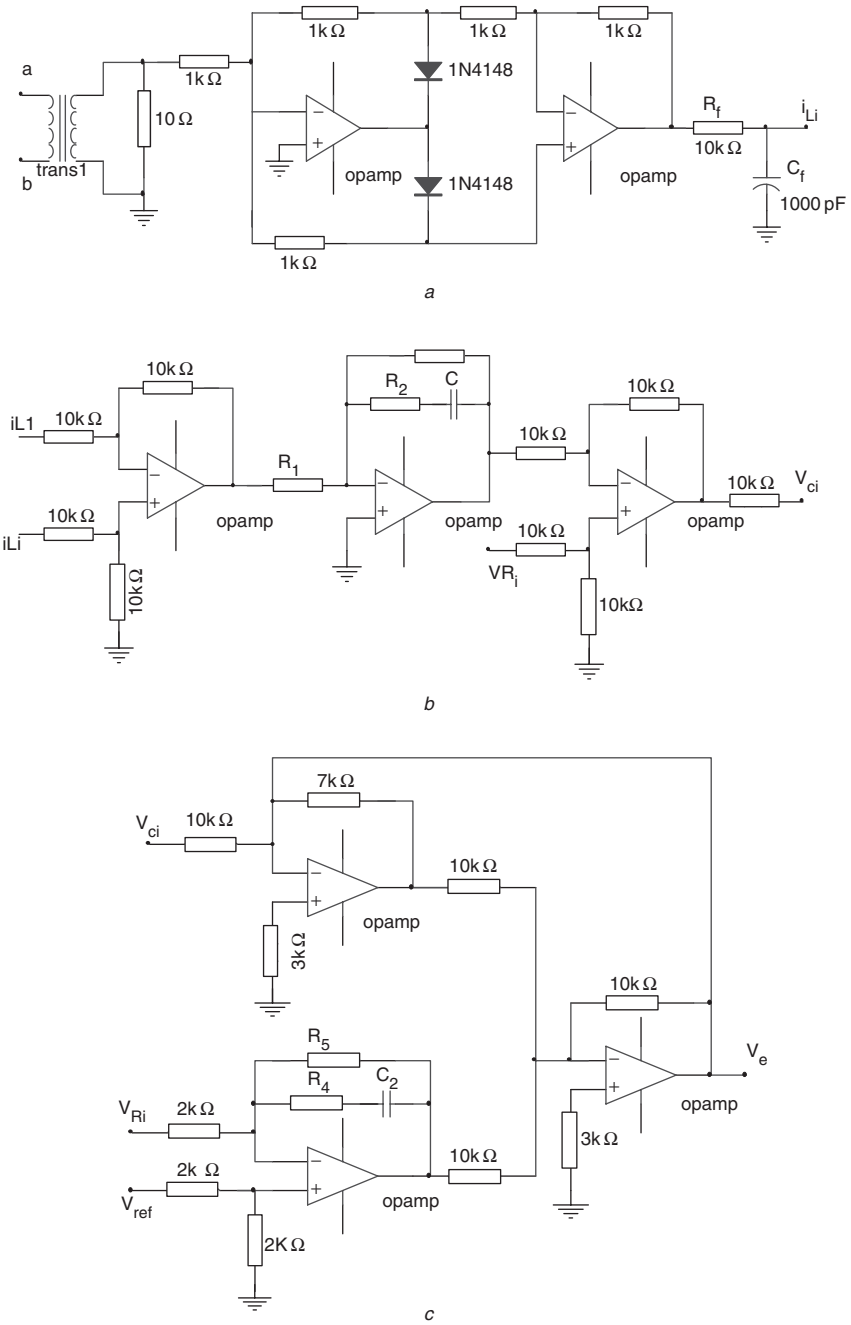


Fig. 7 *Implement circuits*
a Precision rectifier circuit
b Current controller
c Voltage controller

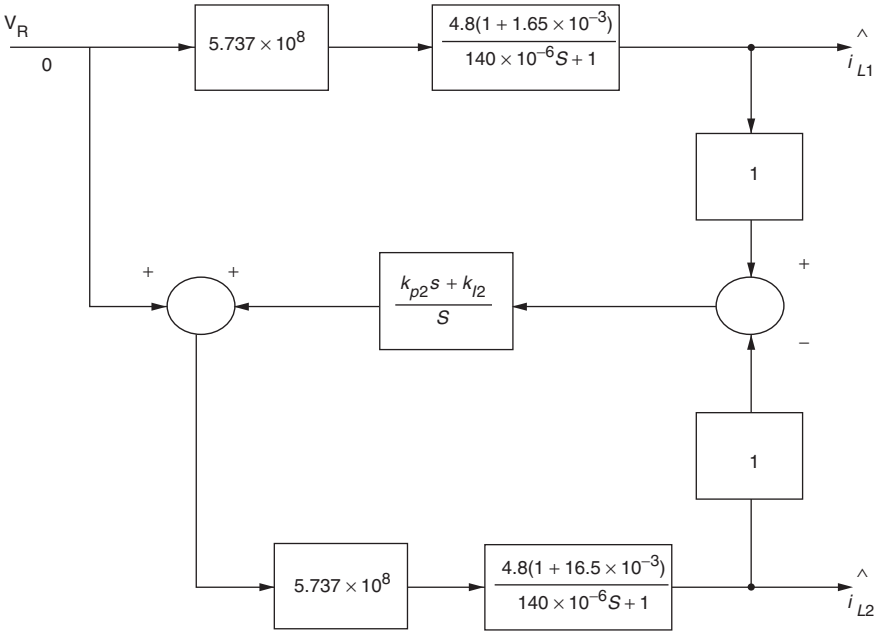


Fig. 8 *Two-module block diagram for implementing a reduced model with inner current loop*

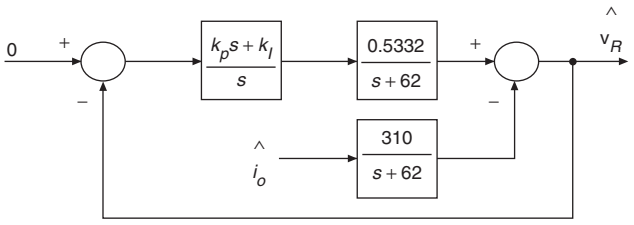


Fig. 9 *Block diagram for implementing a reduced model without inner current loop*

listed below for later analyses:

$$V_g = 48\,V,\ V_o = 5\,V,\ D = 0.3,\ m_c = 10,\ R_c = 0.12\,\Omega$$

Thus, from (1) we can derive that

$$\begin{aligned}
F_1 &= \frac{0.15(1 + 132 \times 10^{-6}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_2 &= \frac{40 \times 10^{-6}s(1 + 132 \times 10^{-6}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_3 &= \frac{40 \times 10^{-6}s(1 + 132 \times 10^{-6}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_4 &= \frac{24(1 + 132 \times 10^{-6}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_5 &= \frac{0.03(1 + 16.5 \times 10^{-3}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_6 &= \frac{-(1 + 132 \times 10^{-6}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_7 &= \frac{-(1 + 132 \times 10^{-6}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1} \\
F_8 &= \frac{4.8(1 + 16.5 \times 10^{-3}s)}{0.132 \times 10^{-6}s^2 + 140 \times 10^{-6}s + 1}
\end{aligned} \tag{14}$$

and the useful transfer functions (5)–(8) are as follows:

$$\begin{aligned}
A_c &= \frac{\begin{array}{c}(5.512 \times 10^{-17}s^5 + 3.8 \times 10^{-2}s^4 + 2.59 \times 10^{11}s^3 \\ +1.995 \times 10^{15}s^2 + 1.51 \times 10^{19}s + 9.01 \times 10^{20})\end{array}}{\begin{array}{c}(2.3 \times 10^{-21}s^6 + 2.93 \times 10^{-15}s^5 + 3.052 \times 10^{8}s^4 \\ +3.752 \times 10^{21}s^3 + 0.2886 \times 10^{26}s^2 \\ +3.459 \times 10^{27}s + 1.044 \times 10^{29})\end{array}} \\
A_g &= \frac{\begin{array}{c}(9.5 \times 10^{-7}s^5 + 4.36 \times 10^{7}s^4 + 1.5 \times 10^{20}s^3 \\ +2.282 \times 10^{24}s^2 + 8.75 \times 10^{27}s + 5.22 \times 10^{29})\end{array}}{\begin{array}{c}(2.3 \times 10^{-21}s^6 + 2.93 \times 10^{-15}s^5 + 3.052 \times 10^{8}s^4 \\ +3.752 \times 10^{21}s^3 + 0.2886 \times 10^{26}s^2 \\ +3.459 \times 10^{27}s + 1.044 \times 10^{29})\end{array}} \\
Z_o &= \frac{\begin{array}{c}(6.33 \times 10^{-8}s^5 + 4.307 \times 10^{5}s^4 - 3.646 \times 10^{10}s^3 \\ -6.631 \times 10^{14}s^2 - 2.54 \times 10^{18}s - 1.516 \times 10^{20})\end{array}}{\begin{array}{c}(2.3 \times 10^{-21}s^6 + 2.93 \times 10^{-15}s^5 + 3.052 \times 10^{8}s^4 \\ +3.752 \times 10^{21}s^3 + 0.2886 \times 10^{26}s^2 \\ +3.459 \times 10^{27}s + 1.044 \times 10^{29})\end{array}} \\
A_i &= \frac{\begin{array}{c}(6.33 \times 10^{-8}s^5 + 4.307 \times 10^{5}s^4 - 3.646 \times 10^{10}s^3 \\ -6.631 \times 10^{14}s^2 - 2.54 \times 10^{18}s - 1.516 \times 10^{20})\end{array}}{\begin{array}{c}(2.3 \times 10^{-21}s^6 + 2.93 \times 10^{-15}s^5 + 3.052 \times 10^{8}s^4 \\ +3.752 \times 10^{21}s^3 + 0.2886 \times 10^{26}s^2 \\ +3.459 \times 10^{27}s + 1.044 \times 10^{29})\end{array}}
\end{aligned} \tag{15}$$

5.2 Controller design

The implemented configuration of the controller is shown in Fig. 7. The load current of each module is sensed and scaled by a precision rectifier circuit, as shown in Fig. 7*a*. The average-current controller is sketched in Fig. 7*b*. The output current of each slave module is compared with that of a master module; the regulated current error signal is then used to modify the control signal of the respective slave module. The outer-loop voltage controller shown in Fig. 7*c* is used for achieving output-voltage-regulating characteristics.

The model reduction is performed using the concept of dominant energy mode. Based on the reduced convertor model, a PI controller is designed quantitatively according to the prescribed regulating specification. The two-module block diagrams of the reduced model with and without inner-loop current loop are shown in Figs. 8 and 9, respectively. It is assumed that the mismatch between the current-tracking responses is

$$\Delta G_m = \pm 0.1 G_{m1} \tag{16}$$

and the desired response time of the current-tracking response is $t_{re} = 0.1$ ms. Following the design method introduced in Section 4, the parameters of the current controller C_{I2} can be found as $k_{p2} = 1$, $k_{I2} = 5000$.

The current controller having been designed, the specifications of unit-step response for designing the voltage controller C_v are prescribed as response time $t_{re} = 0.4$ ms and maximum dip of output voltage $V_m = 0.022$ V. Following the design method described in Section 4, the parameters of the voltage controller C_v are obtained as $k_p = 68$, $k_I = 53\,720$.

5.3 Simulation results

The proposed system closed-loop characteristics are decided by the transfer function A_c, A_i, A_g and Z_o. Its Bode plots are shown in Fig. 10. At low frequencies, the remote loop is dominant, as seen previously. At high frequencies, the current loop is dominant, thus realising the full benefits of current-mode control.

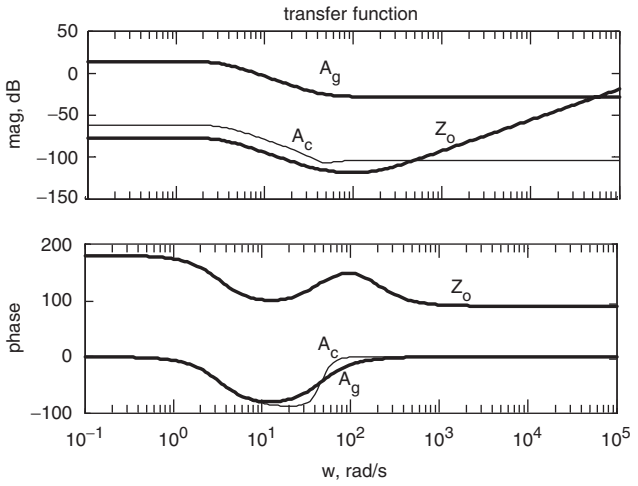


Fig. 10 *Bode plots of the transfer functions A_c, A_g and Z_o ($= A_i$) of the proposed system*

From Fig. 8, the simulated responses of $\hat{i}_{L2}/\hat{i}_{L1}$ shown in Fig. 12 indicate that the given tracking characteristics are exactly satisfied. The simulated responses due to step-load current change (1 A to 3 A) plotted in Figs. 11 and 12 show that good current tracking performance is obtained and the voltage-regulating response satisfies the prescribed specifications.

The nominal load resistance is used to design the controller G_F. When the convertor is operated at 90% rated load, the simulated output voltage and current responses without adding the feedforward controller due to the 10% input-voltage variation are shown in Fig. 13. The results show that the variations in the output-voltage and current-sharing characteristics are small. If further improvement is needed, the feedforward controller is designed to be $G_F = 0.302$. The simulated results shown in Fig. 14 indicate that significant improvements in the input-voltage-rejection characteristics have been achieved.

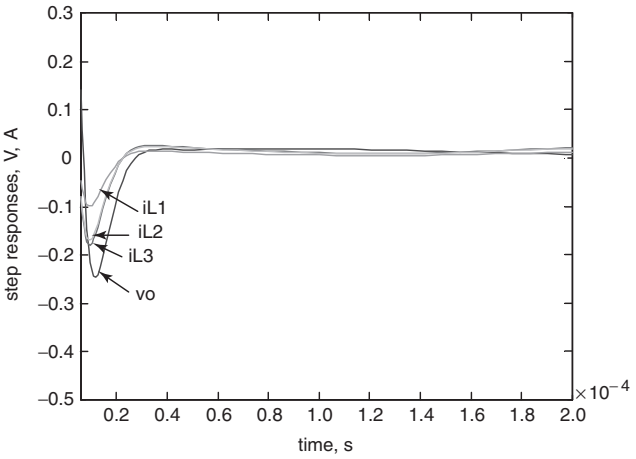


Fig. 11 *Simulated inductor currents and output-voltage-regulating characteristics*

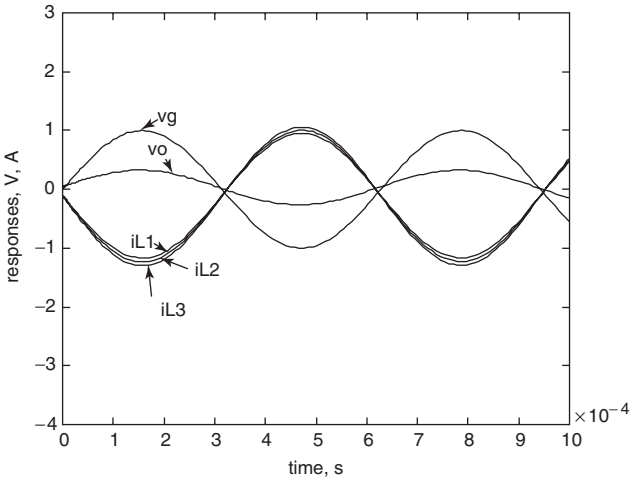


Fig. 12 *Simulated current- and voltage-tracking responses*

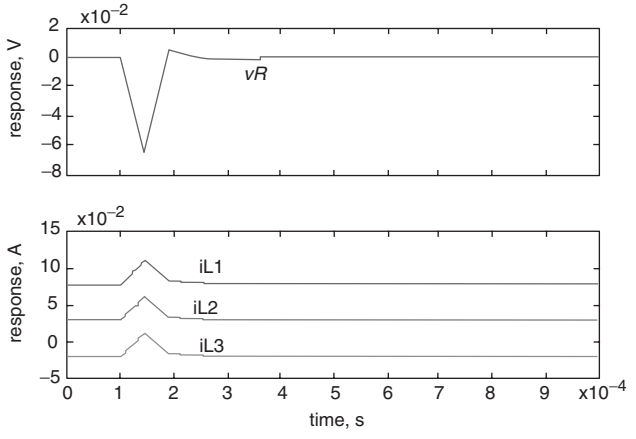


Fig. 13 *Simulated closed-loop responses without feedforward controller*

6 Experiment results

The three-module push–pull convertor system was implemented to verify the master–slave current-comparing scheme. Having confirmed the effectiveness of the proposed system, we implemented the circuit designed current and voltage controllers as shown in Fig. 6. The power-circuit operation under normal conditions and each gate-signal

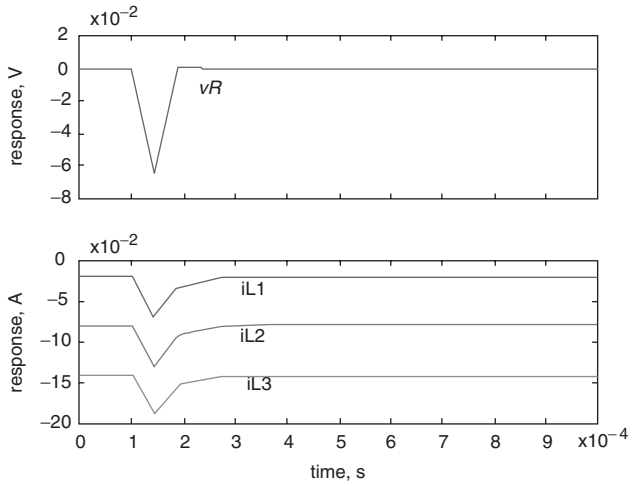


Fig. 14 *Simulated closed-loop responses with feedward controller*

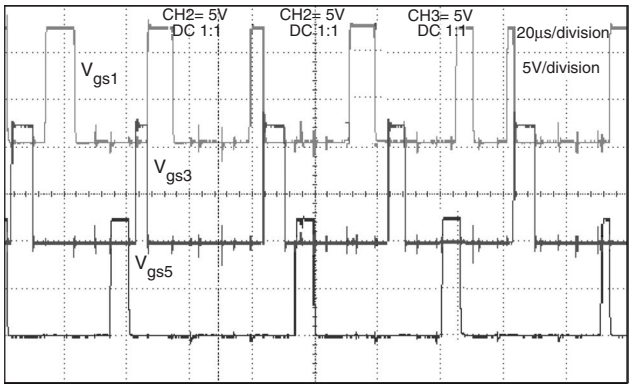


Fig. 15 *Experimental gate signals of the three-module system: master:* V_{gs1}; slave1;V_{gs3}; slave2:V_{gs5}

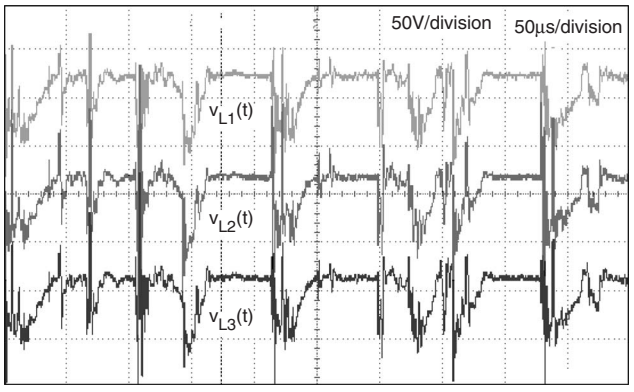


Fig. 16 *Experimental coupled inductor-voltage waveforms; master:* $V_{L1}(t)$; slave1:$V_{L2}(t)$; slave2:$V_{L3}(t)$

experimental waveforms are shown in Fig. 15. We can see that the three modules operated in different duty times while sharing the whole switching cycle. The three modules work together to share the average load current. The experimental inductor voltages of the three modules are shown in Fig. 16. The three voltage waveforms are almost the same because of the coupled circuit.

In Fig. 17, we assumed that the three parallel convertors were normally operated, and the dynamic responses of convertor currents and output voltage were due to the step load-current change (4 A to 6 A). The voltage response obtained is very close to the simulated results shown in

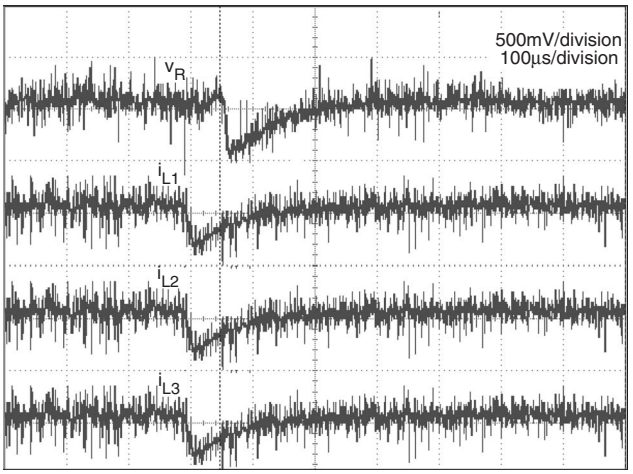
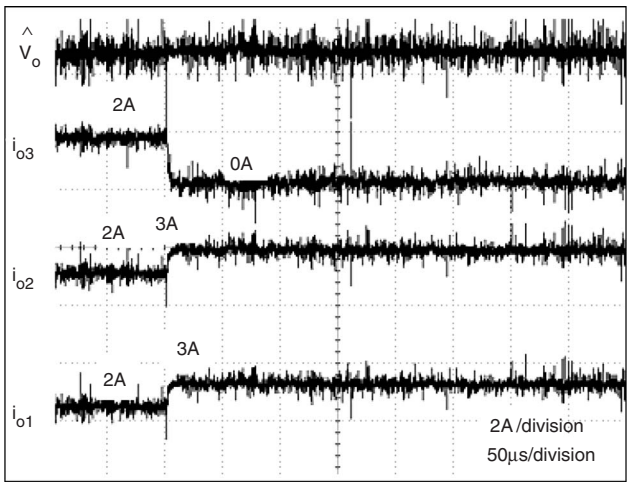
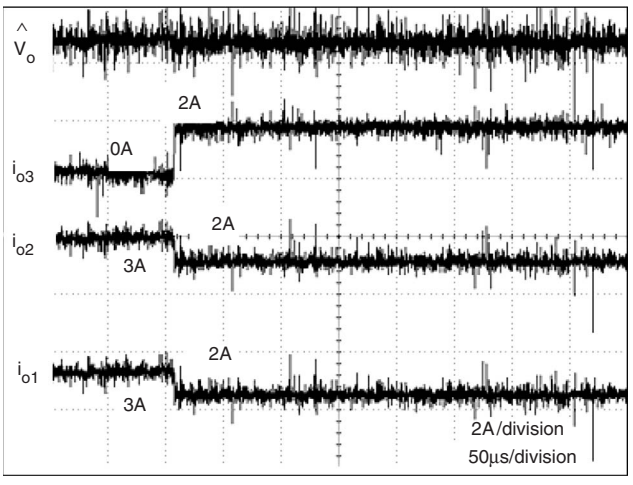


Fig. 17 *Measured dynamic-regulation response (step-load change 4 A to 6 A) of the output voltage* (v_R) *and inductor current* (i_{L1}, i_{L2}, i_{L3})



a



b

Fig. 18 *Measured dynamic responses of the convertor output currents and output voltage*
a Module 3 is suddenly terminated its operation
b Module 3 is suddenly restored

Fig. 11. The dynamic responses of convertor output currents and output voltage plotted in Fig. 18 occur when under steady-state conditions with $I_o = 6$ A: the operation

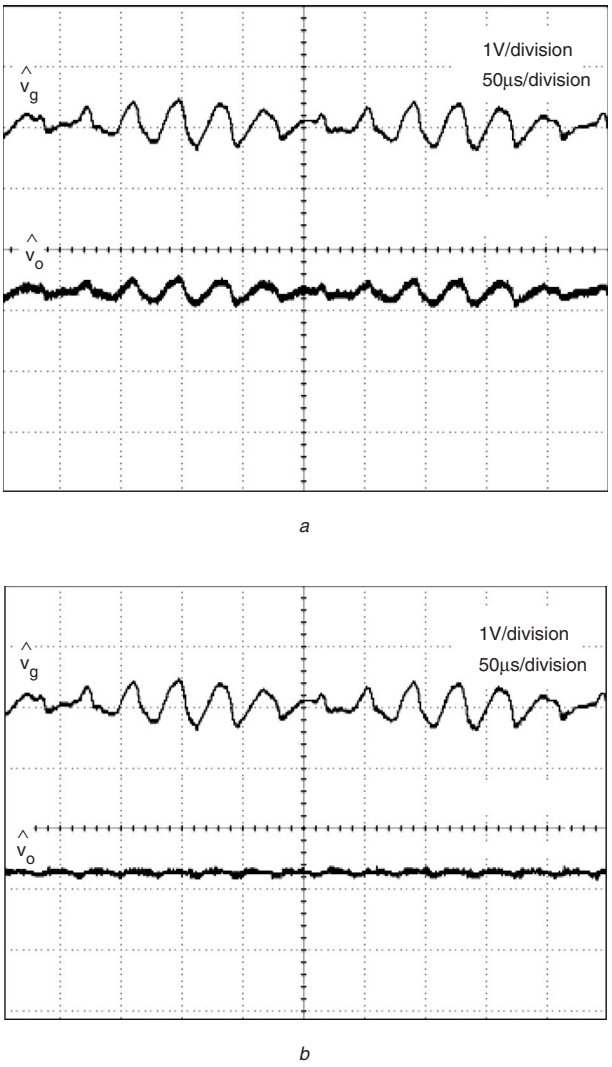


Fig. 19 *Measured output-voltage waveform due to varying input voltage*
a Without feedforward convertor
b With feedforward convertor

of one module is suddenly terminated and then restored. The good performances obtained using the proposed controller are verified by the results. The responses of output voltage due to input-voltage variation without and with feedforward compensator G_F are shown in Fig. 19. The effectiveness of augmenting the feedforward compensator is obvious from the results. It is clear that the controller gives good intermodule current-disturbance-rejection characteristics. In addition, the proposed current-average-sharing schemes of the system are also excellent.

7 Conclusions

The analysis, design and implementation of the three-module parallel push–pull convertor have been presented. A three-module control strategy for the multimodule convertor system with a secondary coupled-inductor output filter is developed. By properly selection of the degree of slope compensation of the current-mode control mechanism, the transfer functions of the convertor can be approximated very well by the first-order reduced models. The selection of slope compensation and the model simplification are carried out easily and intuitively by using the dominant-energy-mode-analysis approach. The reduced models having been found, a design technique has been developed to find the controller parameters. A novel master–slave current-comparing control technique is proposed to yield good dynamic and static current-sharing characteristics. The simulated and experimental results show that good current-sharing and output voltage-regulating performances are achieved by the parallel-convertor system controlled by the proposed controller.

8 References

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9 Appendix: Introduction to model reduction by power decomposition

By partial-fraction expansion, the plant of an nth-order transfer function $G(s)$ can be expressed as

$$G(s) = \frac{M(s)}{D(s)} = \frac{m_0 + m_1 s + \cdots + m_{n-1} s^{n-1}}{d_0 + d_1 s + \cdots + d_n s^n} = \sum_{i=1}^{n} \frac{b_i}{s + a_i} \tag{17}$$

For white-noise input with the variance σ_w^2, the covariance of the output can be found as [8]

$$\sigma(\tau) = \sigma_w^2 \sum_{j=1}^{n} e^{-a_j \tau} \left\{ \sum_{i=1}^{n} \frac{b_i b_j}{-(a_i + a_j)} \right\} \tag{18}$$

and let

$$\sigma_j = \sigma_w^2 \sum_{i=1}^{n} \frac{b_i b_j}{-(a_i + a_j)} \tag{19}$$

$$\sigma(\tau) = \sum_{j=1}^{n} \sigma_j \cdot e^{-a_j \tau} \tag{20}$$

The energy contribution corresponding to the pole $-a_j$ is defined as

$$e_j = \frac{\sigma_j}{\sigma(0)} \tag{21}$$

Then the dispersion e_j can be used as a measurement for the relative importance of each pole of the system. Thus, we can find the dominant pole of the system for model reduction.