Back Gate Bias Dependent Quasi-Saturation in a High-Voltage SOI MOSFET: 2D Analysis and Closed-form Analytical Model

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Abstract

This paper reports a simulation study on the back gate bias dependent quasi-saturation behavior in a high-voltage SOI MOSFET. A closed-form physical back-gate bias dependent quasi-saturation model for the high-voltage SOI MOS device has been derived. Based on the analysis, with a negative back gate bias, in contrast to the zero back gate bias case, the drain current at quasi-saturation is insensitive to the drain voltage since the depth of the conduction channel in the n- region is determined mainly by the back gate bias.

Summary

High-voltage integrated circuits (HVIC's) have been gaining a lot of attention owing to their applications in telecommunication, display drivers, and electrostatic printers[1]. SOI technology for high-voltage MOS devices has been reported for its advantages in speed performance [2]. For a bulk DMOS device, quasi-saturation behavior is important [3]. For an ultra-thin SOI MOS device, the back gate bias effect on its device performance is complicated [4]. In this paper, the back gate bias effect on the quasi-saturation behavior in a high-voltage SOI MOSFET is described. In addition, a closed-form physical back-gate bias dependent quasi-saturation model for the high-voltage SOI MOS device is derived.

Fig. 1 shows the cross section of the high-voltage SOI MOSFET device used in this study. The high-voltage SOI MOSFET has an n+ polysilicon gate and a front gate oxide of $500\mathring{A}$ and a $1\mu m$ thin film above an oxide insulator of $1.2\mu m$. Below the oxide insulator, the p type substrate is doped with $10^{16}cm^{-3}$. There is an n- region of $40\mu m$ with a doping density of $10^{16}cm^{-3}$. Fig. 2 shows the drain current (I_D) vs. the gate-to-source voltage (V_{GS}) characteristics of the high-voltage MOSFET biased at a back gate bias of $0V$ and $-40V$. When V_{GS} is greater than a certain value, the drain current stays almost unchanged regardless of V_{GS}. For a back gate bias of $0V$, as V_{DS} increases, the drain current at quasi-saturation increases. On the other hand, for a negative back gate bias of $-40V$, the drain current at quasi-saturation stays almost unchanged regardless of V_{DS}. Different from the bulk vertical DMOS device, the quasi-saturation behavior of the high-voltage SOI MOS device is also influenced by the back gate bias. Figs. 3 show the 2D electron concentration contours in the thin film region of the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 40V$, $V_{GS} = 20V$) $V_{BS} = 0V$ and $-40V$ from $10^{14}cm^{-3}$ to $10^{16}cm^{-3}$ at an interval of $10^{0.4}cm^{-3}$ As in the bulk vertical DMOS device, the drain current of a high-voltage SOI MOSFET biased at quasi-saturation is determined by the current conduction in the n- region. For a back gate bias of $0V$, most of the n- region is for current conduction. For a back gate bias of $-40V$, the depletion edge moves upward. A more negative back gate bias leads to a smaller channel depth in the n- region. For $V_{BS} = 0V$, the shape of the depletion edge is linear. For $V_{BS} = -40V$, the shape of it is two-region piece-wise linear due to the hole inversion above the field oxide at $V_{BS} = -40V$.

Consider the high-voltage SOI MOS device as shown in Fig. 1. As the back gate bias is more negative than "back-gate" threshold voltage, hole inversion atop field oxide exists. In order to simplify the analysis, as indicated in Fig. 4, the n- epi region is divided into three regions – 1. the hole inversion region, 2. the low electric field region, 3. the high electric field region as shown in Fig. 4. By analyzing the current conduction in these three regions, the closed-form physical back gate bias dependent quasi-saturation model for the high-voltage SOI MOS device has been obtained as shown in Fig. 5. In order to verify the validity of the closed-form physical model, for the high-voltage SOI MOS device, the closed-form physical model results have been compared to the 2D simulation results. Fig. 6 shows the drain current versus V_{BS} curves for the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 10V - 40V$) based on the analytical model and the 2D simulation results. A close match between the two results can be identified. A more negative back gate bias makes the drain current at quasi-saturation smaller. In addition, a higher drain voltage leads to a higher drain current at quasi-saturation. However, the increase in the drain current is not linearly proportional to that in the drain voltage.

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References

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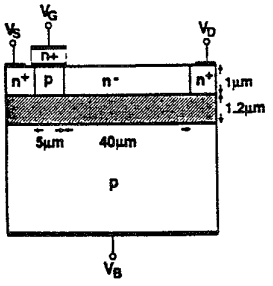

Fig. 1. The cross section of the high-voltage SOI MOSFET under study.

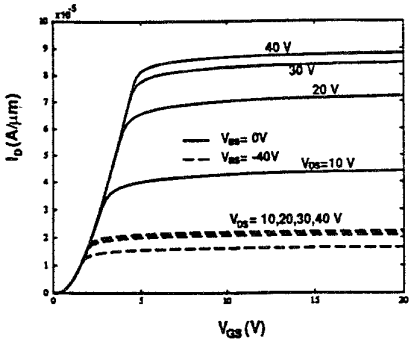

Fig. 2. The I_D vs. V_{GS} characteristics of the high-voltage SOI MOSFET biased at $V_{DS} = 10V - 40V$ for a $V_{BS} = 0V, -40V$.

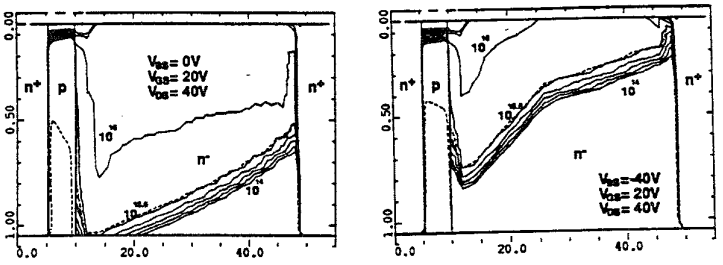

Fig. 3. 2D electron concentration contours in the high-voltage SOI MOSFET biased at quasi-saturation ($V_{DS} = 40V$, $V_{GS} = 20V$) (a) $V_{BS} = 0V$ and (b) $-40V$.

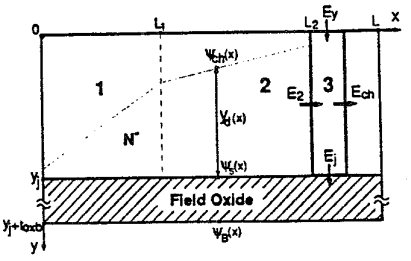

Fig. 4. Partitioning of the n- conduction region of the high-voltage SOI MOSFET under study.

$$I_D = \frac{W v_{sat}(N1 + N2) + E_c F}{(1 - \frac{1}{m})D + E_c L_2} \quad (1)$$

$$N1 = (qN_D y_j + C_{ox} V_{BS})(1 - AV_{BS})(\psi_s(L_2) - \psi_s(L_1)) - \frac{1}{3} AC_{ox}(\psi_s(L_2)^3 - \psi_s(L_1)^3)$$

$$N2 = \frac{1}{2}(AqN_D y_j + 2AC_{ox} V_{BS} - C_{ox})(\psi_s(L_2)^2 - \psi_s(L_1)^2)$$

$$D = (1 - AV_{BS})(\psi_s(L_2) - \psi_s(L_1)) + \frac{1}{2} A(\psi_s(L_2)^2 - \psi_s(L_1)^2)$$

$$A = \frac{C_{ox}^2}{\epsilon_{si} q N_D}$$

$$F = \frac{W q \mu_n N_D (y_d(L_1) - y_d(0))(\psi_{ch}(L_1) - \psi_{ch}(0))}{ln(y_j - y_d(0)) - ln(y_j - y_d(L_1))} \quad (2)$$

$$\psi_s(L_2) = V_{BS} + \frac{q N_D y_j}{C_{ox}} \quad (3)$$

$$L_2 = L - \sqrt{\frac{\epsilon_{si} y_j}{C_{ox}}} \sinh^{-1}\left(\frac{V_{DS} + \phi_{fn} - \frac{A}{2}(\psi_s(L_2) - V_{BS})^2 - \psi_s(L_2)}{\alpha E_c \sqrt{\frac{\epsilon_{si} y_j}{C_{ox}}}}\right) \quad (4)$$

Fig. 5. Important equations.

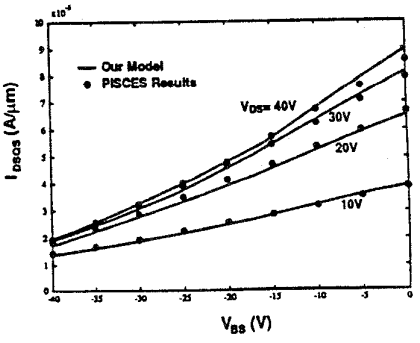

Fig. 6. The drain current versus V_{BS} curves for th high-voltage SOI MOSFET biased at quasi-saturati ($V_{DS} = 10V - 40V$) based on the analytical model and the PISCES simulation results.