Quality Factor Improvement of on-Chip Inductors for HIPERLAN RFIC by Micromachining

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The enhancement of quality factor of on-chip inductors by micromachining for HIPERLAN application is presented in this paper. A process for the selective removal of the substrate underneath of the on-chip inductors was also developed. The fabrication steps consist of aniostropic wet etching of the semiconductor substrate under the inductors followed by laser striping of passivation layers to expose the pads for IC testing. Experimental results show that the Quality factors of the micromachined inductors can be increased up to 50% around 5 GHz, which is suitable for HIPERLAN applications.

1. INTRODUCTION

Recently there is growing interest in RF CMOS technology because of its low cost and integration capability with base band circuits. Modern CMOS FET's certainly have a high enough f_T to provide gain in the frequency range of several GHz. The challenge, interesting enough, is in the difficult fabrication of high quality monolithic passive components such as inductors. Several techniques have been investigated in order to enhance lumped element [1-4]. Particularly micromachining approaches have recently demonstrated to be very useful to reduce losses and parasitic effects by suspending microwave devices, such as coplanar waveguides, Lange-couplers and inductors [4-6]. However post IC micromachining processing tends to damage the pads on a die for circuit testing and hence it is better for pads to be covered by passivation layers during micromachining. If the pads are protected, a mean is necessary to strip the passivation layers after micromachining. In this paper, laser trimming for the striping of passivation layer is proposed. It is found that the quality factors of the inductors can be increased up to 50 % around 5 GHz after the inductors were micromachined.

2. DESIGN OF THE SUSPENDED INDUCTOR

The energy storage and loss mechanisms in an inductor on silicon can be described by the equivalent energy model shown in Fig.1, where L_S, R_S, R_P and C_O ($C_O = C_P + C_S$) represent the overall inductance, conductor loss, substrate loss, and overall capacitance, respectively. According to the fundamental definition of quality factor, Q can be derived to be [7]

$$Q = 2\pi \frac{\left|\textit{Peak Magnetic Energy} - \textit{Peak Electric Energy}\right|}{\textit{Energy Loss in One Oscillation Cycle}} = \frac{\omega L_S}{R_S} \times \frac{R_p}{R_p + \left[\left(\omega L_S / R_S\right)^2 + 1\right] \cdot R_S} \times \left(1 - \frac{{R_S}^2 C_o}{L_S} - \omega^2 L_S C_o\right) \quad (1)$$

where $\omega L_S / R_S$ accounts for the magnetic energy stored and the ohmic loss in the spiral conductor. The second term is the substrate loss factor. The last term is the self-resonance factor describing the reduction in Q due to the increase in the peak electric energy with frequency and the vanishing of Q at self-resonance frequency. From (1), one can conclude that the degradation in Q-factor of an inductor is mainly due to the series resistance of the

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inductor and the substrate resistance. Increasing the thickness or the width of metal lines will reduce the series resistance. However, the thickness of metal lines is limited in a CMOS process, and widening the metal lines not only takes larger chip area but also raises the capacitance between the metal line and substrate. Therefore it seems to be more attractive to increase Q by increasing R_P , which means removing the substrate underneath the inductor. The MEMS simulation program ACES (Anisotropic Crystalline Etching Simulation) has been used to simulate the etching process as shown in Fig.2. The front-side bulk micromachining approach applied herein is based on a post-process wet etching, without modifying the standard IC fabrication and with no influence on the unconcerned electronic parts. The fabrication steps started from anisotropic wet etching of the (100) silicon substrate beneath all the inductors through the uncovered substrate regions around the inductors. The etchant used is KOH solution. Then, Laser trimming was done to remove the passivation layers over the pads for the ease of testing.

3. EXPERIMENTAL RESULTS

The on-chip inductors with pads covered by passivation layers were fabricated by 0.35μm CMOS process provided by TSMC (Taiwan Semiconductor Manufacturing Corporation). HP8510 network analyzer in conjunction with the cascade probe station was used to measure the characteristics of the inductors. Both micromachined and unmicro-machined inductors are measured and compared. The Q factor of the inductors with different turns versus frequencies are shown in Figs.3(a)-(d). Several interesting features can be observed from these figures. First of all, the self-resonance frequencies, defined as the frequencies at which Q is zero, move to lower frequencies as the turns of inductors increase. This is reasonable because the capacitances between the metal lines and substrate increase as the turns increase. Removing the substrate underneath the inductors decreases the capacitances and therefore the self-resonance frequencies increase. Also note that the frequency responses of Q factors for micromachined and unmachined inductors are almost identical at lower frequencies. The Q factors of micromachined inductors are enhanced only at higher frequencies. This is because at low frequencies, the series resistance is the limiting factor and the shunting effect of the meta-to-substrate capacitance is still negligible. However, at high frequencies the shunting capacitance dominates and reduction of this capacitance by removing the substrate underneath the inductors improves the Q factors significantly. From the experimental results shown in Fig.3, micromachining of the micromachined inductor increases the inductor Q's at 5 GHz at least 50%.

4. CONCLUSION

A front-side bulk micromachining approach was proposed for fabrication of suspended inductors without modifying the standard IC fabrication and with no influence on the unconcerned electronic parts. It involves the protection of testing pads by passivation layers during micromachining and stripping of passivation layers Laser trimming after micromachining. The experimental results from the micromachined and unmachined inductors showed that the self-resonance frequencies and Q factors can be improved significantly by selective removal of the silicon substrate underneath the inductors.

ACKNOWLEDGMENT

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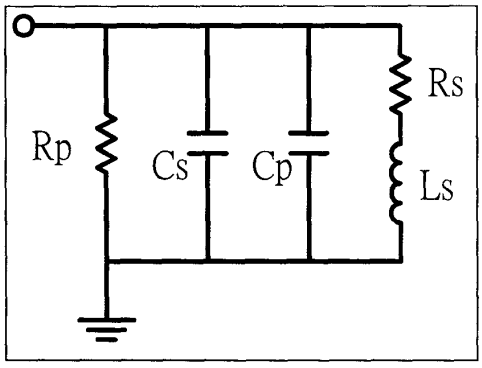
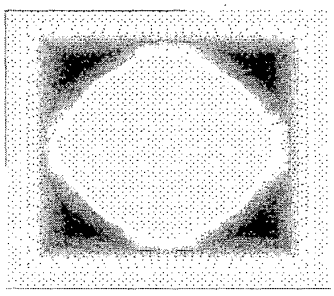
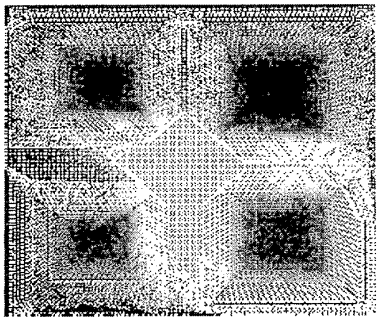


Fig. 1 The one port equivalent circuit model of inductors.



(a)



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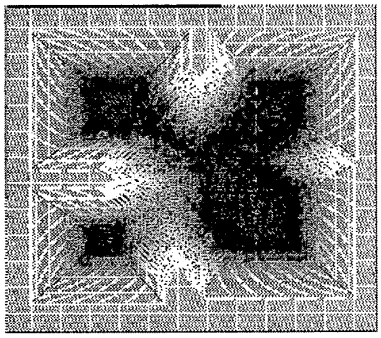
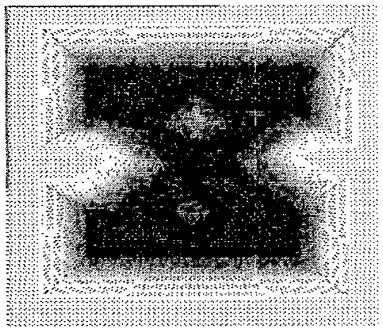
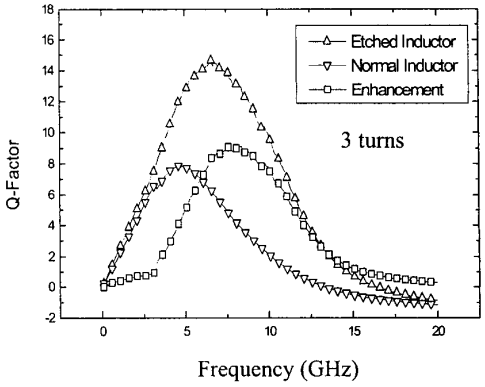


(c)

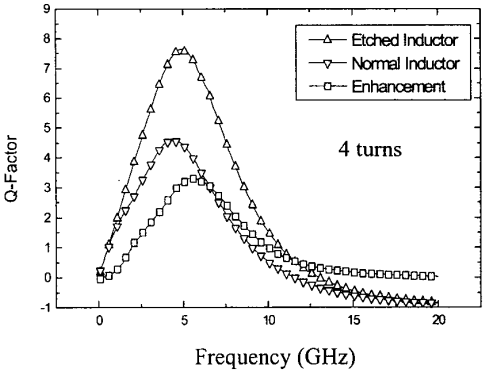


(d)

Fig.2 The sequel of anistropic etching of (100) silicon by simulation



(a)



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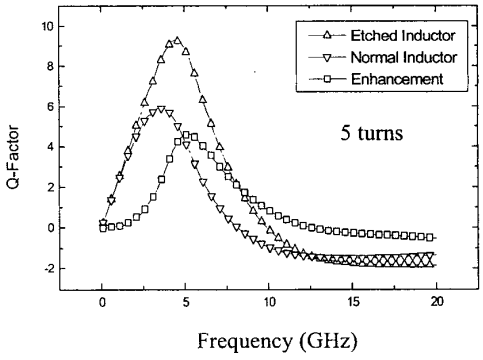

(c)

Fig.3 The frequency responses of micromachined (triangles: △) and unmachined (flipped triangles: ▽) inductors with different turns: (a) 3 turns; (b) 4 turns; (c) 5 turns. Squares □ represent the enhancement of Q factors.