A Low Phase Noise 52-GHz Push-Push VCO in 0.18-μm Bulk CMOS Technologies

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Abstract — **A V-Band fully integrated complementary push-push VCO is first presented in 0.18-μm bulk CMOS technologies. Thin-film microstrip (TFMS) lines are utilized in the circuit to reduce the conductive substrate effect. In order to lower the phase noise, complementary cross-coupled pairs are used to generate negative conductance. The measured phase noise at 1-MHz offset is about -97 dBc/Hz at 52.6 GHz and is -104 dBc/Hz at 26.3 GHz. To the author's best knowledge, this complementary CMOS VCO achieves the lowest phase noise in comparison with other VCOs using standard bulk CMOS processes in V-Band.**

Index Terms — **CMOS, thin-film microstrip line, VCO.**

I. Introduction

The increasing demand of monolithic microwave integrated circuits (MMICs) is motivated by the rapid growth of high speed wireless communications, for example, wireless LANs and mobile phones. Voltage controlled oscillator (VCO) is an important building element in the implementation of modern wireless communication systems. For considerations of low cost and low power consumption, CMOS is the best choice for these applications. However, in microwave and millimeter-wave regime, integrated VCOs are generally realized by III-V compound devices or SiGe HBTs [1]-[3]. CMOS VCOs found few applications due to its low maximum oscillation frequency (f_{max}).

As CMOS technology progresses to deep submicron, it has become possible to realize millimeter-wave circuits in standard CMOS process, leading to low cost and high integration. So far, some V-Band VCOs have been reported in CMOS technology [4]-[5]. A 50-GHz VCO was presented which adopted a modified 0.25-μm CMOS process for high quality factor inductor and high f_{max} of the device [4]. It shows low phase noise of -99 dBc/Hz at 1-MHz offset and the output power is -11 dBm. Another fully-integrated 51-GHz VCO fabricated with 0.12-μm CMOS process, demonstrated -30-dBm output power and -85 dBc/Hz phase noise at 1-MHz offset [5]. In addition to adopting high f_{max} process technology, some other circuit structures were presented to achieve higher oscillation frequency. Push-push VCO is an attractive approach which sums up the differential fundamental signals and takes the second harmonic as the output and is even able to work above device f_{max}.

In this paper, we present the first complementary push-push VCO in V-Band. The VCO core is composed of NMOS and PMOS cross-coupled pairs to lower the phase noise. The second harmonic output signal is taken from two fundamental differential buffers working in triode region for the nonlinearity which deliver more output power. Compared with the conventional topology, the circuit delivers 14 dB more 2nd harmonic output power in our approach from simulations. The MMIC VCO achieves very low phase noise of -97dBc/Hz at 1-MHz offset with a tuning range of 0.5 GHz.

Table 1 summarizes the comparison among previously published MMW VCOs using silicon-based processes and this work. It can be observed that our chip demonstrated the lowest phase noise and comparable chip size, power consumption and output power among the reported VCOs using standard bulk CMOS processes in V-Band.

II. CMOS Characteristics And Process

The chip is implemented by TSMC's 0.18-μm commercial process [6]-[7], with a 2-μm AlCu top metal layer. The substrate conductivity is approximately 10 S/m. With optimized CMOS technology and deep n-well, this technology provides f_T and f_{max} better than 60 and 55 GHz, respectively. MIM capacitors with 1 fF/μm^2 are also provided in the process.

III. Circuit Design

Figure 1 shows the structure of the thin-film microstrip (TFMS) line which consists of the 2-μm AlCu top metal (M6) as the signal line and bottom metal (M1) as ground plane in the 0.18-μm CMOS process. The TFMS line has the advantage of the ground plane shielding to isolate the conductive substrate. The substrate thickness of TFMS line is about 6.52-μm, thus the coupling effect between transmission lines is negligible. Therefore, the matching elements of transmission lines and inductors can be

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TABLE I

COMPARISON WITH PREVIOUSLY REPORTED VCOS IN V-BAND

Process	Frequency (GHz)	Phase noise @ 1 MHz offset (dBc/Hz)	Chip Size (mm^2)	P_{DC} (mW)	Pout (dBm)	Topology	Ref.
0.25-μm SiGe BiCMOS	60	-87	0.4 x 0.75	73.8	-17	Differential colpitts	[1]
	76	-91	0.4 x 0.75	128	-7	Differential colpitts	
SiGe HBT	50	-98	N/A	N/A	-5.6	Push-push	[2]
0.09-μm CMOS SOI	60	-92	0.3 x 0.25	21	-6.8	Cross-coupled	[14]
Modified 0.25-μm CMOS	50	-99	0.52 x 0.39	13	-11	Cross-coupled	[4]
0.12-μm CMOS	51	-85	0.5 x 0.9	1	-30	Cross-coupled	[5]
0.18-μm CMOS	52.5	-86	0.8 x 1	41	-8	Single-ended	[13]
0.25-μm CMOS	63	-86	0.45 x 0.7	118.8	-4	Cross-coupled and push-push	[10]
0.18-μm CMOS	52	-97	0.45 x 0.45	122.4	-5	Complementary cross-coupled and push-push	This Work
				27.3	-16		

replaced by meandering TFMS lines in a very small area to reduce the circuit size. A full-wave EM simulation tool, Sonnet [8], was used to estimate the impedance of the TFMS inductors over the frequency of interest.

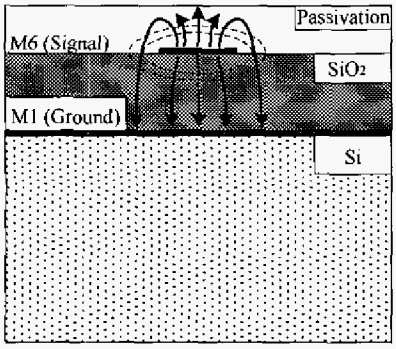

Fig. 1. The structures of the TFMS on bulk CMOS process.

The conventional cross-coupled push-push VCO circuit structure is shown in Fig. 2 where it adopts NMOS cross-coupled pair to generate negative conductance and the output signal is delivered from the middle of the inductor of the LC tank where the differential fundamental signals cancel out each other and the second harmonic signals combine in phase [9]-[10].

Complementary cross-coupled pairs show lower phase noise because it has larger voltage swing within the LC tank and it shows more symmetric effective impulse sensitivity function [11]. Unfortunately, the f_{max} of PMOS is usually much lower than NMOS so that it can not be used in millimeter-wave regime. But for push-push VCO, we can still use PMOS to make the VCO oscillate at fundamental frequency and deliver the 2nd harmonic signal to achieve low phase noise in high frequency. Figure 3 shows the circuit schematic of our design. The LC tank is composed of the TFMS differential inductors and NMOS connected as varactors. We omit the current source to lower the phase noise such that the noise from current source can be eliminated and tank voltage swing can be increased [12]. In addition, the negative conductance is generated by complementary cross-coupled pairs consisting of M_1-M_4 to lower the phase noise. In this design, if we remove the PMOS cross-coupled pair (M_1 and M_2) and maintain the DC current, the phase noise degrades by about 3 dB from the simulation results.

The circuit can deliver both fundamental and second harmonic signals simultaneously. The fundamental 26-GHz output signals are delivered through common-source buffers. Unlike the conventional push-push topology where the 2nd harmonic signal is extracted from the virtual short point inside the resonant tank, the 2nd harmonic signal is first amplified through buffers (M_5 and M_6) and taken from the middle of TFMS inductors (L_3 and L_4). To acquire more output power, M_5 and M_6 are biased in triode region, and therefore, with the increased device nonlinearity, the 2nd harmonic power can be increased. From the simulations, it delivers 14 dB more 2nd harmonic output power in our approach than the conventional one in which the output is taken from the middle of the inductor of the LC tank, that is, from point A shown in Fig. 3.

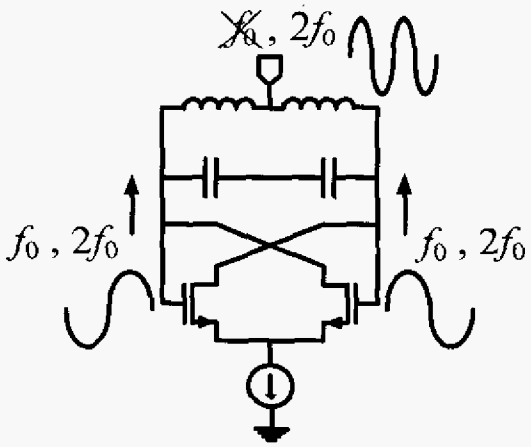

Fig. 2. Schematic of conventional NMOS-only cross-coupled push-push VCO.

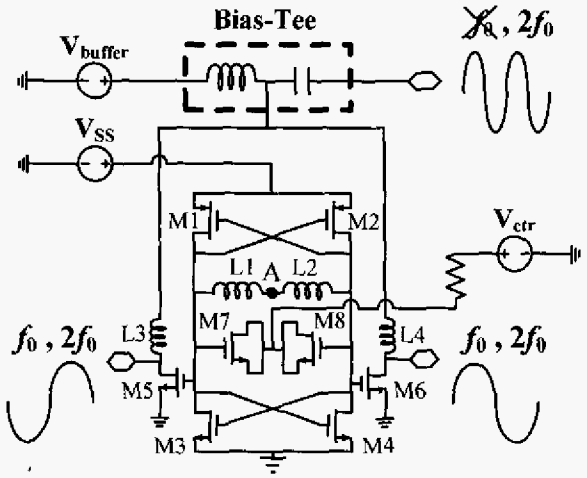

Fig. 3. Schematic of proposed VCO.

IV. Measurement Results

This chip was tested via on-wafer probing and was biased by aluminum bond wires. The VCO core draws 13 mA at 2.1 V and the buffer amplifiers draw 4 mA at 0.3 V. The measured output power is about -16 dBm and the oscillation frequency is from 52.6 to 52 GHz with control voltage (V_{ctr}) from 0.8 to 2.1 V. When we increase the VCO bias voltage up to 3.6 V with 34 mA and the buffers draw 19 mA at 0.7 V, the output power goes up to -5 dBm. And the oscillation frequency is from 52.5 to 52 GHz with control voltage (V_{ctr}) from 1 to 3 V. Figure 4 shows the output power and oscillation frequency versus control voltage in both bias conditions. The measured phase noise is -97 dBc/Hz at 1-MHz offset at 53 GHz and -104 dBc/Hz at 26.5 GHz as shown in Fig. 5 and Fig. 6 respectively. The measured fundamental power from the 2nd harmonic output is –58.6 dBm shown in Fig. 7 with 10 dB cable and transition loss, that is, the fundamental rejection is about 30 dB. Figure 8 shows the chip photo and the size is 0.45 x 0.45 mm^2 including all test pads.

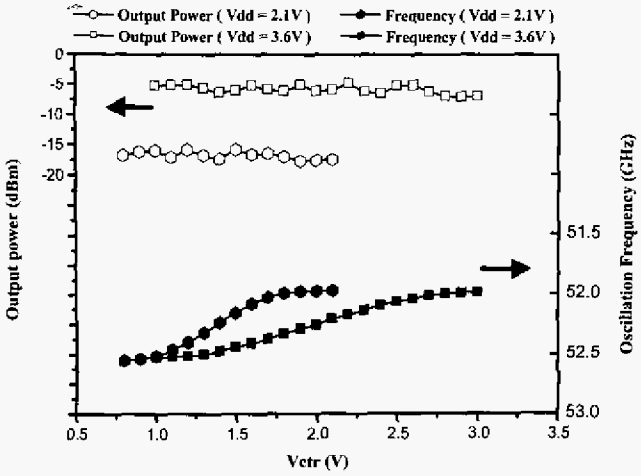

Fig. 4. Measured output power versus control voltage.

V. Conclusion

This paper presents the design and measurement of a 52 GHz complementary push-push VCO using a standard CMOS 0.18-μm process. The chip shows very low phase noise of -97 dBc/Hz at 1-MHz offset at 52 GHz with 0.5-GHz tuning range. The output power is about -16 dBm while dissipating 27.3-mW dc power. This chip shows a miniature size of 0.45 x 0.45 mm^2. To the best of our knowledge, the VCO achieves the lowest phase noise in V-Band in comparison with other VCOs in standard CMOS process.

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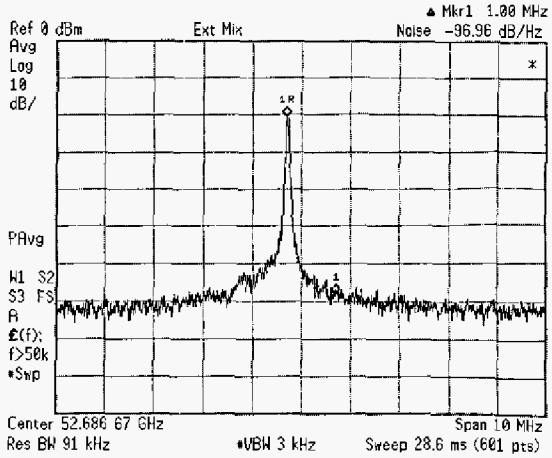

Fig. 5. Measured phase noise at 1 MHz offset.

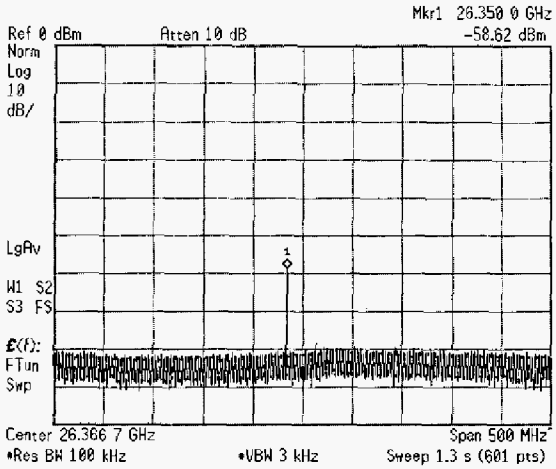

Fig. 6. Measured fundamental power from 2^{nd} harmonic output.

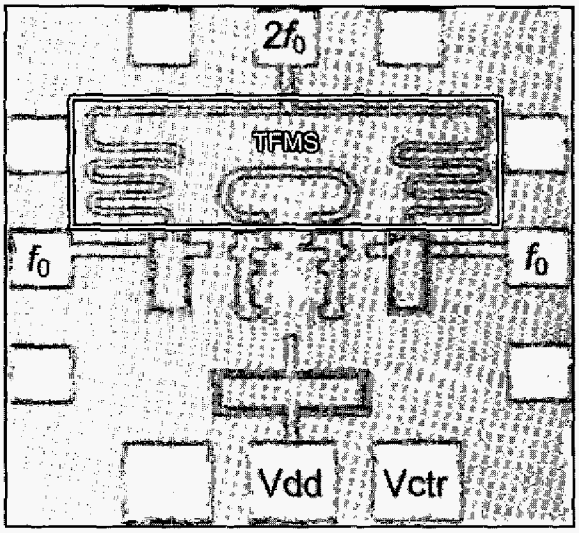

Fig. 7. Chip photo of the push-push VCO with a chip size of 0.45 x 0.45 mm^2.

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