0.7 V Manchester carry look-ahead circuit using PD SOI CMOS asymmetrical dynamic threshold pass transistor techniques suitable for low-voltage CMOS VLSI systems

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Abstract: The authors report a 0.7 V Manchester carry look-ahead circuit using partially depleted (PD) SOI CMOS dynamic threshold (DTMOS) techniques for low-voltage CMOS VLSI systems. Using an asymmetrical dynamic threshold pass-transistor technique with the PD-SOI DTMOS dynamic logic circuit, this 0.7 V PD-SOI DTMOS Manchester carry look-ahead circuit has an improvement of 30% in propagation delay time compared to the conventional Manchester carry look-ahead circuit based on two-dimensional device simulation MEDICI results.

1 Introduction

The Manchester carry chain circuit based on pass transistors and dynamic logic techniques [1–4] has been used to process the 'propagate and generate' signals produced by half adders to generate the carry signals, which are needed to realise arithmetic circuits in CPU VLSI. Using the pass-transistor structure, the Manchester carry chain circuit is the most efficient among all carry look-ahead circuits. In the Manchester carry chain circuit, the carry signal of the present bit C_i is high if the generate signal G_i is high or if the carry signal of the previous bit C_{i-1} and the propagate signal P_i are high: $C_i = G_i + C_{i-1} \cdot P_i$, for $i = 1$–n, where n is the bit number, G_i and P_i are the generate and propagate signals $G_i = X_i \cdot Y_i$ and $P_i = X_i \oplus Y_i$ produced from two inputs X_i, Y_i to the half adder. In the Manchester carry chain circuit, each bit carry signal $\bar{C}_i$ is low if the generate signal G_i is high or if the propagate signal P_i is high and the carry signal of the previous bit $\bar{C}_{i-1}$ is low. Pass transistors have been used to control the operation of the Manchester carry chain circuit. However, when the carry chain is long, the ripple-carry propagation delay due to the RC delay of the pass transistor may not be acceptable for high-speed applications [2–4], which is especially serious for low-voltage VLSI circuits. In 1999, Kuo *et al.* [5] described a 1.5 V bootstrapped pass-transistor-based Manchester carry chain circuit using bootstrapped dynamic logic circuit techniques for low-voltage VLSI. Recently, CMOS dynamic threshold (DTMOS) techniques [6, 7] have been detailed, giving advantages in low-voltage SOI CMOS VLSI circuits. In this paper, a 0.7 V Manchester carry chain circuit using PD-SOI DTMOS techniques suitable for low-voltage CMOS VLSI is described.

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2 Asymmetrical dynamic threshold pass-transistor (ADTPT) technique

Figure 1*a* shows the asymmetrical dynamic threshold pass-transistor (ADTPT) used in the circuit [8]. Derived from the conventional dynamic threshold pass-transistor (DTPT)

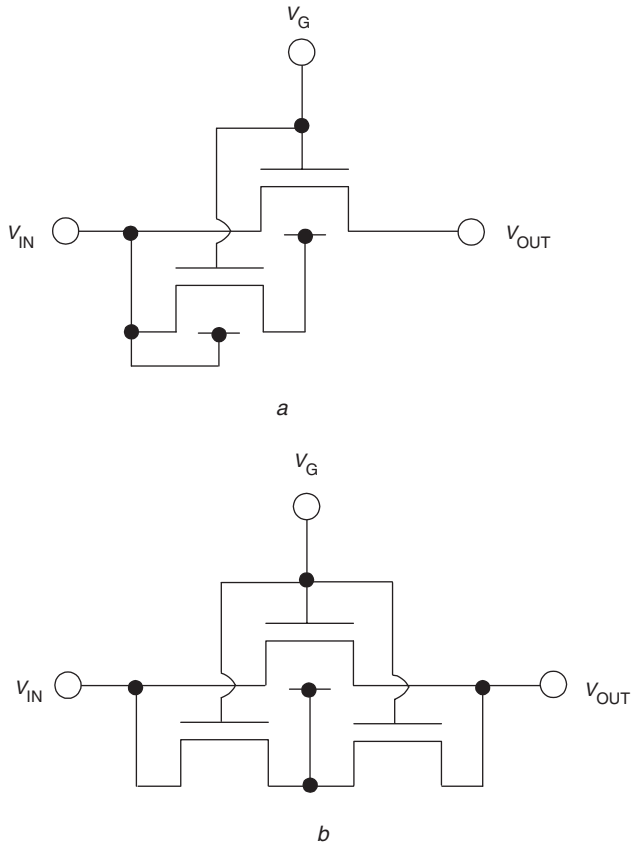

Fig. 1 *ADTPT and conventional DTPT*
a Asymmetrical dynamic threshold pass transistor (ADTPT)
b Conventional symmetrical dynamic threshold pass-transistor (DTPT) circuit with two auxiliary transistors

circuit [9] shown in Fig. 1*b*, which includes two extra auxiliary transistors, the ADTPT shown in Fig. 1*a* needs only one extra auxiliary transistor to control the body bias of the pass transistor. In the conventional dynamic threshold pass-transistor (DTPT) circuit shown in Fig. 1*b*, the body of the main pass-transistor is connected to the source/drain node of the two auxiliary transistors with their gates tied to the gate of the main pass-transistor. In addition, the source/drain nodes of these two auxiliary transistors are connected to the source and drain of the main pass-transistor, respectively. Furthermore, the bodies of these auxiliary transistors are floating. In contrast, as shown in Fig. 1*a*, in the ADTPT, the body of the main pass-transistor is connected to the source/drain node of the auxiliary transistor, whose gate is tied to the gate of the main pass-transistor and whose body is tied to the source/drain node of the main pass-transistor, instead of floating as in the conventional DTPT. The advantage of the new ADTPT can be understood by considering its logic operation. When V_G is high (V_{DD}), both the pass-transistor and the auxiliary transistor are on. During the pass-logic-1 operation, which is the most critical one, the logic-1 level is propagated from the input V_{IN} to the output V_{OUT}. When the input V_{IN} increases from low to high, due to the functioning of the auxiliary transistor, the body of the main pass-transistor (V_B) is raised to V_{DD}–V_{TH}($V_B = V_{DD}$), where V_{TH}($V_B = V_{DD}$) is the threshold voltage of the auxiliary transistor biased with a body bias $V_B = V_{DD}$. Compared to the conventional dynamic threshold pass-transistor (DTPT) circuit, the new ADTPT has faster speed owing to the higher body voltage provided by its auxiliary transistor. In the conventional dynamic threshold pass-transistor (DTPT) circuit, due to the two-auxiliary-transistor structure, the body bias of the main pass-transistor is half way between the input $V_{IN} = V_{DD}$ and the output V_{OUT}, which rises from 0V to V_{DD}–V_{TH}. In the new ADTPT, owing to the single-auxiliary-transistor structure, the body bias of the main pass-transistor is tied to a higher level, V_{DD}–V_{TH} ($V_B = V_{DD}$). Therefore, the effective threshold voltage of the main pass-transistor of the new ADTPT is much smaller than in the conventional case. As a result, a higher speed is obtained passing the logic-1 signal from the input V_{IN} to the output V_{OUT}.

3 PD-SOI Manchester carry chain circuit using DTMOS techniques

Figure 2 shows the 0.7 V two-bit PD-SOI Manchester carry chain circuit using ADTPT techniques. As shown in the Figure, this PD-SOI Manchester carry chain circuit is derived from the conventional Manchester carry chain circuit, with its dynamic logic circuit replaced by the PD-SOI CMOS dynamic logic circuit using DTMOS techniques (M_{p1}–M_{p3}, M_{n1}–M_{n6}, M_{aux1}) and the pass-transistors replaced by the asymmetrical dynamic threshold pass-transistor (ADTPT) technique (M_{n7}, M_{n8}, M_{aux2}, M_{aux3}). Before we describe the operation of the overall circuit, the PD-SOI CMOS dynamic logic circuit using the ADTPT technique for the Manchester carry chain circuit is described below.

3.1 PD-SOI CMOS dynamic logic circuit using ADTPT techniques

Figure 3 shows the PD-SOI CMOS dynamic logic circuit using DTMOS techniques, which is derived from a PD-SOI SRAM cell reported by Kuo *et al.* [10, 11]. As shown in the Figure, the body V_B of M_{n1} and M_{n2} is connected to clock CLK via a pass-transistor M_{auxl} with its gate connected to V_{DD}. With this arrangement this dynamic logic circuit has a shorter propagation delay during the logic evaluation period. The operation of this PD-SOI CMOS dynamic logic circuit is divided into two periods: the precharge period and the logic evaluation period. During the precharge period. CLK is low. At this time, V_B is connected to ground since M_{aux1} is always on and the output V_{out} is precharged to high by M_{p1}. When CLK becomes high during the logic evaluation period, V_B is charged to V_{DD}–V_{TH}, where V_{TH} is the threshold voltage of the pass transistor M_{aux1}. In this situation, if the input C0 is high, M_{n1} and M_{n2} provide a larger discharge current due to the lower threshold voltage from the non-zero body bias V_B. As a result, the output V_{out} is discharged to ground faster. Pass-transistor M_{auxl} is important in this dynamic logic circuit. With M_{auxl}, the body of M_{n1} and M_{n2} is raised to only 0.4 V instead of 0.7 V, such that the unwanted currents from the forward-biased body–source junctions in M_{n1} and

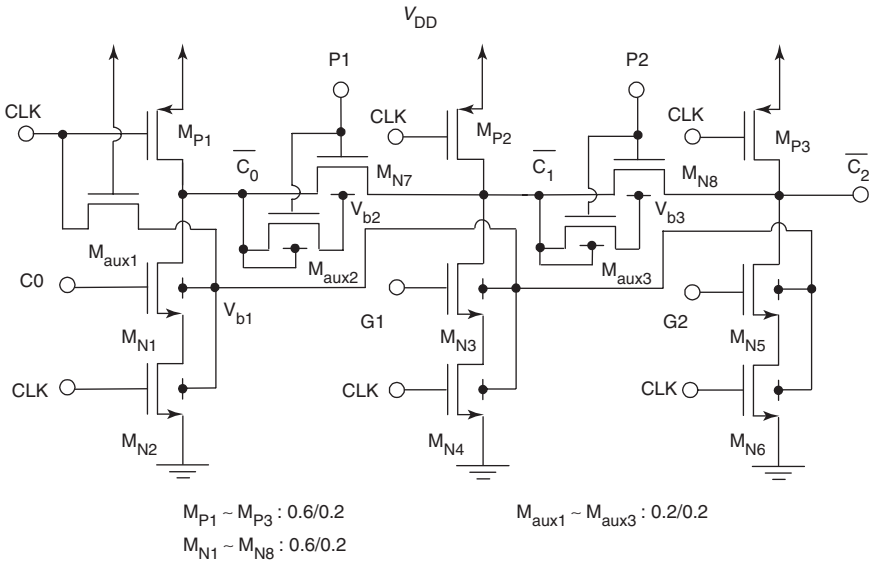

Fig. 2 *0.7 V two-bit PD-SOI Manchester carry chain circuit using DTMOS techniques*

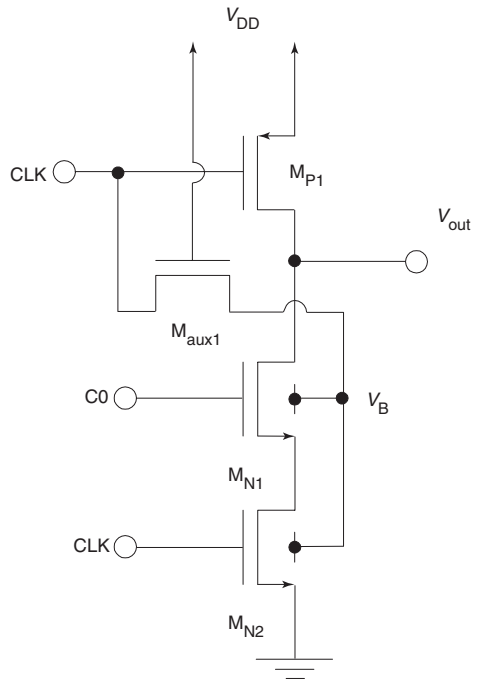

Fig. 3 *PD-SOI CMOS dynamic logic circuit using ADTPT techniques*

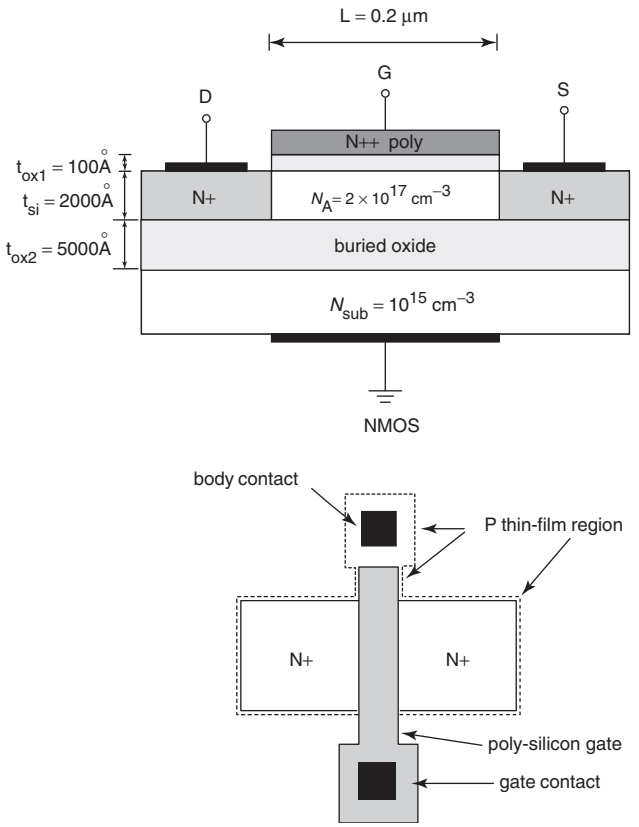

Fig. 4 *Cross-section of partially depleted (PD) SOI NMOS device and layout used in PD-SOI Manchester carry chain circuit using DTMOS techniques*

M_{n2}, which may disturb the pull-down of the output V_{out}, can be reduced.

3.2 Operation of the circuit

The operation of the 0.7 V PD-SOI Manchester carry chain circuit using DTMOS techniques as shown in Fig. 2 is described as follows. When clock CLK is low, it is the precharge phase – the internal output nodes $\bar{C}_0 - \bar{C}_2$ are set to high. At this time, since the auxiliary transistor M_{aux1} is on, the body voltage V_B of the pull-down devices in the dynamic logic circuit, M_{n1}–M_{n6}, is low. The body voltage V_{b2}/V_{b3} of the main pass-transistor in the ADTPT is controlled by the auxiliary transistor M_{aux2}/M_{aux3}. When the propagate signal (P1/P2) is high, the auxiliary transistor M_{aux2}/M_{aux3} is on, the body voltage V_{b2}/V_{b3} is charged to high. When the propagate signal (P1/P2) is low, the body of the main pass-transistor M_{n7}/M_{n8} is floating. When clock CLK is high, it is the evaluation phase. During this time, the body voltage V_{b1} of the pull-down devices M_{n1}–M_{n6} in the dynamic logic circuits is charged to $V_{DD} - V_{TH}$, where V_{TH} is the threshold voltage of the auxiliary device (M_{auxl}) such that the threshold voltages of the pull-down devices are lowered to enhance the current driving capability. When the propagate signal P1/P2 is high, the body voltage V_{b2}/V_{b3} of the main pass-transistor in the ADTPT is charged to high via the auxiliary transistor M_{aux2}/M_{aux3} through the internal node $\bar{C}_0/\bar{C}_1/\bar{C}_2$. Therefore, the threshold voltage of the main pass-transistor in the ADTPT is lowered to decrease the *RC* delay time associated with the pass-transistors.

4 Performance and discussion

In order to investigate the effectiveness of the proposed 0.7 V PD-SOI Manchester carry chain circuit and ADTPT, transient performance was studied. In the transient analysis, typical partially depleted (PD) SOI MOS devices with cross-section and layout as shown in Fig. 4 were used. The PD-SOI NMOS device used in the circuit had a channel length of 0.2 μm, a front gate oxide of 100 Å, an N+ poly-silicon gate, a p-type thin film of 2000 Å doped with a density of 2×10^{17} cm^{-3}, and a buried oxide of 5000 Å on top of the p-type substrate doped with a density of 10^{15} cm^{-3}. Two-dimensional device simulation using MEDICI [12] was used to carry out the transient analysis of the circuit considering the PD-SOI devices in terms of the cross-section described above. Considering the effect of the body contact region, a parasitic capacitance of 1fF and a parasitic resistance of 10 KΩ were placed at the body contact of related devices. Since the transient analysis of the PD-SOI Manchester carry-chain circuit is done at the two-dimensional device level, it is very time consuming. In order to reduce computing time, a two-bit Manchester carry-chain circuit was analysed. Using a 600 MIPS workstation, each transient analysis took about 50 minutes.

Figure 5 shows the transient waveforms of a two-bit Manchester carry chain circuit operating at a supply voltage of 0.7 V, using the PD-SOI DTMOS technique and the conventional approach based on two-dimensional device simulation MEDICI [12] results. In this study, the channel width of all devices was 0.6 μm, except the auxiliary transistors, which had a channel width of 0.2 μm. In order to consider the effect of parasitic capacitances. Parasitic capacitances of 0.1 pF were placed at the internal nodes C_1/C_2. As shown in Fig. 5, initially clock CLK is low – the precharge phase. At this time, M_{p1}–M_{p3} are on, therefore internal nodes $\bar{C}_0 - \bar{C}_2$ are precharged to 0.7 V. At this time, the propagate signals $P1/P2$ are also low. The body voltage of the pull-down devices in the dynamic logic circuit is around 0 V since the auxiliary transistor M_{aux1} is on. In addition, the body voltage of the main pass-transistors in the ADTPT V_{b2}/V_{b3} is around 0.3 V, which is due to the leakage current over the source/body junction of the auxiliary transistor M_{aux2}/M_{aux3} although they are off. The body of the auxiliary transistor M_{aux2}/M_{aux3} is 0.7 V.

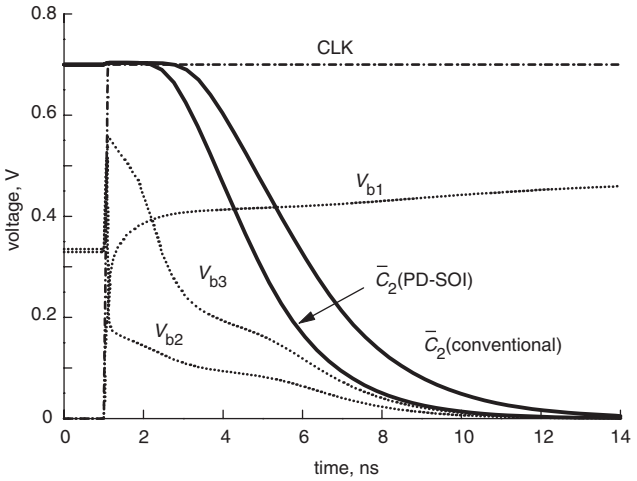

Fig. 5 *Transient waveforms of two-bit Manchester carry chain circuit operating at supply voltage 0.7 V using PD-SOI DTMOS techniques, and using a conventional approach based on a two-dimensional device simulation MEDICI [12] results*

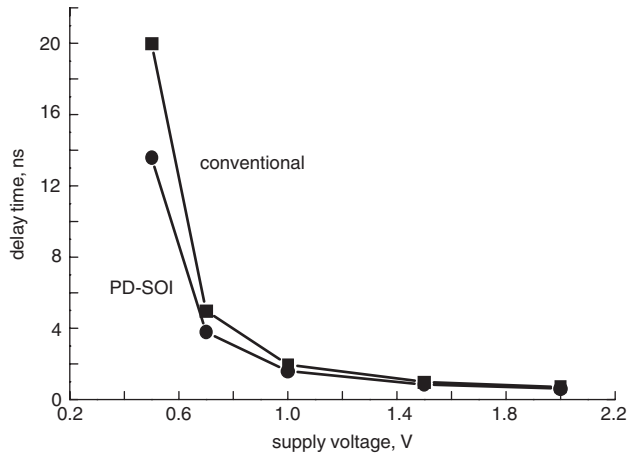

Fig. 6 *Propagation delay time against supply voltage of two-bit Manchester carry chain circuit using PD-SOI DTMOS techniques and using conventional approach*

Owing to the leakage current over the source/body junction of the auxiliary transistor, the body voltage V_{b2}/V_{b3} is forced to be around 0.3 V instead of 0 V. After the precharge cycle, when clock CLK turns high from low with the condition that $C0 = 1$, $P1 = 1$, $P2 = 1$, $G1 = 0$, and $G2 = 0$, which represents the path of the worst delay, the body voltage V_{b1} of the pull-down devices rises to about 0.45 V. On the other hand, the body voltage V_{b2}/V_{b3} of the main pass-transistor in the ADTPT also rises to around 0.55 V. Hence the conductance of the ADTPT has been enhanced to pull-down the internal nodes $\bar{C}_1 - \bar{C}_2$ quickly. Along with the pull-down of the internal nodes $\bar{C}_0 - \bar{C}_2$ the body voltage V_{b2}/V_{b3} also decays accordingly. As shown in the Figure, at a supply voltage $V_{DD} = 0.7$ V, the propagation delay time of the two-bit Manchester carry-chain circuit using the PD-SOI DTMOS techniques is 3.78 ns, which is 25% faster as compared to the one using the conventional approach. At a clock frequency of 100 MHz, the power consumption of the circuit is 14.1 μW with the DTMOS technique, which is slightly larger than that not using the DTMOS technique (13.1 μW).

Figure 6 compares propagation delay time versus supply voltage of a two-bit Manchester carry chain circuit using PD-SOI DTMOS techniques with that using the conventional approach. As shown in the Figure, PD-SOI DTMOS techniques do not show a dominant advantage over the conventional approach at supply voltages over 1 V. On the other hand, PD-SOI DTMOS techniques are especially effective at low supply voltages. At a supply voltage of 0.5 V, improvement of the propagation delay using PD-SOI DTMOS techniques over the conventional approach is as high as 33%. The ADTPT presented in this paper could be used for a Manchester carry look-ahead circuit of any length, with a similar improvement. The ADTPT could also be used in any pass-transistor related circuits to give enhanced speed performance.

5 Conclusions

In this paper, a 0.7 V Manchester carry look-ahead circuit using partially-depleted (PD) SOI CMOS dynamic threshold (DTMOS) techniques has been reported. Using an asymmetrical dynamic threshold pass-transistor (ADTPT) technique with the PD-SOI DTMOS dynamic logic circuit, this 0.7 V PD-SOI DTMOS Manchester carry look-ahead circuit gives an improvement of 30% in propagation delay time over the conventional Manchester carry look-ahead circuit based on two-dimensional device simulation (MEDICI) results.

6 References

1 Weste, H., and Eshraghian, K.: 'Principles of CMOS VLSI design: a system perspective' (Addison-Wesley, 1985), pp. 322–326
2 Kernhof, J., Beunder, M.A., Hoefflinger, B., and Haas, W.: 'High-speed CMOS adder and multiplier modules for digital signal processing in a semicustom environment', *IEEE J. Solid-State Circuits*, 1989, **24**, (3), pp. 570–575
3 Kuo, J.B., Chen, S.S., Chang, C.S., Su, K.W., and Lou, J.H.: 'A 1.5 V BiCMOS dynamic logic circuit using a "BiPMOS pull-down" structure for VLSI implementation of full adders', *IEEE Trans. Circuits Syst. I, Fundam. Theory Appl.*, 1994, **41**, (4), pp. 329–332
4 Kuo, J.B., and Lou, J.H.: 'Low-voltage CMOS VLSI circuits' (John Wiley, New York, 1999), ISBN 0471321052
5 Lou, J.H., and Kuo, J.B.: 'A 1.5 V bootstrapped pass-transistor-based manchester carry chain circuit suitable for implementing low-voltage carry look-Ahead adders', *IEEE Trans. Circuits Syst.*, 1999, **45**, pp. 1191–1194
6 Assaderaghi, F., Sinitsky, D., Parke, S.A., Bokor, J., Ko, P.K., and Hu, C.: 'Dynamic threshold-voltage MOSFET (DTMOS) for ultra-low voltage VLSI', *IEEE Trans. Electron Devices*, 1997, **44**, (3), pp. 414–422
7 Chung, I.Y., Park, Y.J., and Min, H.S.: 'A new SOI inverter using dynamic threshold for low-power applications', *IEEE Electron Devices Lett.*, 1997, **18**, (6), pp. 248–250
8 Wang, B.-T., and Kuo, J.B.: 'A novel low-voltage silicon-on-insulator (SOI) CMOS complementary pass-transistor logic (CPL) circuit using asymmetrical dynamic threshold pass-transistor (ADTPT) technique'. Proc. Midwest Symp. Circuits and System (MWSCAS), August 2000
9 Lindert, N., Sugii, T., Tang, S., and Hu, C.: 'Dynamic threshold pass-transistor logic for improved delay at low power supply voltages', *IEEE J. Solid-State Circuits*, 1999, **34**, (1), pp. 85–89
10 Lin, S.C., and Kuo, J.B.: 'A novel 0.7 V two-port 6T SRAM memory cell structure with single-bit-line simultaneous read-and write access (SBLSRWA) capability using PD SOI CMOS DTMOS techniques'. Proc. IEEE SOI Conf., 1999, pp. 75–76
11 Kuo, J.B., and Liu, S.C.: 'A novel 0.7 V two-port 6T SRAM memory cell structure with single-bit-line simultaneous read-and-write access (SBLSRWA) capability using PD SOI DTMOS techniques', US Patent no. 6061268, May 2000
12 'MEDICI: two-dimensional semiconductor device simulation' (Technology Modeling Associates, Palo Alto, CA, 1996)