This article has been accepted for publication in IEEE Open Journal of Circuits and Systems. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2024.3510921

Synchronization and Channel Estimation Design for Multi-Stream MIMO System in Sub-Terahertz Channel Model

Chung-Lun Tu[1], Chen-Yuan Tseng[1], Wei-Che Lee[1], Kang-Lun Chiu[1], Pei-Yun Tsai[2], and Shyh-Jye Jou[1]

[1]Institute of Electronics, National Yang Ming Chiao Tung University, Hsinchu, Taiwan
[2]Department of Electrical Engineering, National Central University, Jhongli, Taiwan

Corresponding author: Chung-Lun Tu (e-mail: cltu.ee07@nycu.edu.tw).

This work was supported in part by MediaTek, in part by the Taiwan Semiconductor Manufacturing Company (TSMC), and in part by the Ministry of Science and Technology, Taiwan, under Grant NSTC 112-2622-8-A49-013-SB, Grant MOST 108-2221-E-009-090-MY3

ABSTRACT This article presents an advanced synchronization and channel estimation architecture for multi-stream MIMO systems in sub-terahertz environments. To streamline hardware complexity, we employ Golay cross-correlation across all detection and estimation schemes. Key innovations include a precise timing detection algorithm that utilizes pulse shaping impulse response and quadratic regression, along with multiple window-based approaches to enhance performance against non-ideal effects. At the architectural level, a shared optimized Golay correlator reduces hardware usage by 23%, efficiently handling multiple correlation lengths in a single design. Additionally, we propose an indexing-count method that addresses sorting challenges, achieving notable improvements in processing speed and complexity reduction. The proposed design supports the highest modulation schemes defined in IEEE Std. 802.15.3d, achieving an uncoded bit error rate of 1.96×10^{-4} for 16-QAM and 64-QAM at SNRs of 18.8 dB and 25 dB, respectively. This meets the IEEE Std. 802.15.3d standard of 10^{-12} at SNRs of 19.6 dB and 25.6 dB for these modulation schemes after error correction. Our hardware operates at a clock rate of 1.76 GHz, enabling dual-stream transmission and achieving a throughput of 21.12 Gb/s with 64-QAM modulation.

INDEX TERMS Hybrid beamforming, Multi-stream, MIMO, Synchronization, Channel Estimation, IEEE 802.11ay, IEEE 802.15.3d, Sub-Terahertz Communication, Golay Sequence

I. INTRODUCTION

In recent years, to meet the growing data rate requirements of emerging applications, 6G systems are anticipated to complement microwave and mmWave connectivity with wireless communications operating at frequencies far beyond conventional ranges [1]. This includes sub-terahertz (sub-THz) band communications (100–300 GHz), offering continuous spectrum resources spanning tens of gigahertz. To address these needs, IEEE Std. 802.15.3d [2] was developed as an amendment to IEEE Std. 802.15.3–2016 [3], defining a wireless physical (PHY) layer capable of 100 Gbit/s transmission, specifically targeting the sub-THz spectrum for its abundant resources.

As the 6G vision is still in its early stages, the primary goal of IEEE Std. 802.15.3d is to provide a low-complexity, high-rate connectivity standard, focusing on single-stream transmission and bandwidth enhancements to increase data rates, with bandwidths of up to 69 GHz. However, expanding the signal bandwidth to these levels presents substantial design challenges for RF circuits, such as analog-to-digital converters (ADCs), digital-to-analog converters (DACs), and power amplifiers (PAs), thereby complicating practical implementation.

To address these challenges, MIMO (Multiple-Input Multiple-Output) technology offers a promising solution by enhancing spectral efficiency and link reliability through spatial multiplexing and diversity gains. In the sub-THz band, MIMO can significantly boost data rates and link robustness without consuming additional bandwidth, making it a critical enabler for future high-capacity 6G systems.

Although considerable research has been conducted on sub-THz MIMO systems [4-7], much of these work focus on advancing transmission techniques and developing new algorithmic solutions to address high-frequency challenges. While these studies have driven significant progress in the field, they primarily concentrate on improving system

performance from a theoretical and algorithmic perspective.

In contrast, this paper focuses on validating and extending existing standard-defined specifications, particularly IEEE Std. 802.15.3d, to evaluate the feasibility of sub-THz MIMO operations in future communication environments. Instead of introducing entirely new algorithms or transmission paradigms, we investigate whether the existing standard, originally developed for single-stream transmission, can be adapted to support multi-stream MIMO under practical conditions.

An essential element of our approach involves leveraging insights from IEEE Std. 802.11ay [8], a millimeter-wave specification that focuses on MIMO scenarios. This standard shares a critical design feature with IEEE Std. 802.15.3d by incorporating the Golay sequence as a preamble to facilitate synchronization and channel estimation. This similarity makes it feasible to adopt concepts and techniques developed for IEEE Std. 802.11ay's MIMO scenarios within IEEE Std. 802.15.3d.

In this work, we define the environment and specifications for a sub-THz MIMO system by referencing published sub-THz MIMO channel models [9] and accounting for non-ideal effects typical of this frequency range [2]. We then present a Golay correlation-based multi-stream receiver design tailored for sub-THz MIMO systems and propose a corresponding hardware architecture. Through a series of two-stage estimation and compensation approaches, the design achieves accurate synchronization and precise channel estimation.

To meet the high-speed 1.76 GHz clock rate requirement, each module is developed with pipelining techniques and a feed-forward data path. To further reduce hardware complexity, we propose a shared multi-length Golay correlator structure capable of computing correlation results for various detection and estimation algorithms. For high-performance channel estimation, we analyze several algorithms tailored to the system's environment and specifications. Numerous studies have effectively addressed the threshold selection problem [10-14], particularly in sparse channel environments typical of high-frequency systems. Building on these efforts, we propose a streamlined architecture for the channel impulse response (CIR) denoising threshold within the channel estimator. These solutions enhance estimation accuracy while minimizing hardware complexity, ensuring that the system achieves high reliability and a low bit error rate (BER) of 10^{-12}, as specified by IEEE Std. 802.15.3d.

This paper is organized as follows. The system specifications and models for multi-stream MIMO system in sub-THz band are introduced in Section II. The algorithms of synchronization and channel estimation with simulation results are described in Section III. The hardware design is presented in Section IV. Finally, conclusions are given in Section V.

II. SYSTEM SPECIFICATIONS AND MODEL

Since IEEE Std. 802.15.3d does not define MIMO operation, we refer to the multi-stream frame structure from IEEE Std. 802.11ay, as depicted in Fig. 1, where s indicates the stream index, N_s is number of streams. As described in [15], this specification leverages two key features.

First, Golay sequences, a type of complementary sequence, exhibit the property that the sum of their autocorrelation functions is zero for all time shifts except at zero. This characteristic ensures precise alignment, strong noise resistance, and makes Golay sequence ideal for synchronization in communication systems. The autocorrelation property of complementary sequences is expressed as:

$$\mathrm{Ga}_N^*[-n] \otimes \mathrm{Ga}_N[n] + \mathrm{Gb}_N^*[-n] \otimes \mathrm{Gb}_N[n] = N\delta[n] \quad (1)$$

where Ga and Gb form a complementary Golay pair, N is the length of the sequence, $\otimes$ denotes the circular convolution operator, and $\delta[n]$ represents the delta function.

Second, to achieve high estimation accuracy, specific pairs of Golay sequences with zero cross-correlation are employed to minimize interference between different streams, which is critical for channel estimation. This property is given by:

$$\mathrm{Ga}_N^{v^*}[-n] \otimes \mathrm{Ga}_N^{u}[n] + \mathrm{Gb}_N^{v^*}[-n] \otimes \mathrm{Gb}_N^{u}[n] = 0 \quad (2)$$

$$\mathrm{Ga}_N^{u^*}[-n] \otimes \mathrm{Ga}_N^{v}[n] + \mathrm{Gb}_N^{u^*}[-n] \otimes \mathrm{Gb}_N^{v}[n] = 0 \quad (3)$$

where u and v indicate distinct Golay sequences. In IEEE Std. 802.11ay, these indices correspond to different streams, and the zero cross-correlation property holds only if u belongs to $\{1,3,5,7\}$ and v equals to $u+1$. Since the sequences that achieves zero cross-correlation with a given sequence is uniquely determined, the valid pairs are limited to (1, 2), (3, 4), (5, 6), and (7, 8). Only these pairs can mutually satisfy the zero cross-correlation property.

When the system employs more than two streams, the channel estimation field must expand accordingly, as shown in Fig. 1. For transmissions with 3 or 4 streams, the Golay sequence duration must double, and for 5 to 8 streams, it must quadruple. This additional dimension ensures sufficient information to effectively eliminate interference between streams.

The system parameters are listed in Table I, and the system simulation block diagram is shown in Fig. 2. We adopt the sub-THz MIMO channel model from [9] and employ a hybrid beamforming structure [16] to address high signal attenuation and mitigate interference between streams in the sub-THz band. Given the sparse nature of the sub-THz channel [9] and the high correlation within tightly-packed antennas, we focus on two-stream transmission, with the first stream having the largest beamforming gain. As depicted in Fig. 3, our system uses two RF chains for the two-stream transmission, with both the transmitter and receiver equipped with 64 antennas. A DFT codebook is utilized for the analog precoder and combiner design through beam searching, enabling us to concentrate on the effective channel in the digital baseband. This system also

accounts for RF component imperfections, including additive white Gaussian noise (AWGN), carrier frequency offset (CFO), sampling clock offset (SCO), and symbol timing offset (STO).

By leveraging the complementary property of the Golay sequence described in [17], the proposed synchronization scheme exploits the repetitive Golay sequences found within both the legacy-short training field (L-STF) and enhanced directional multi-gigabit short training field (EDMG-STF). The effective channel estimation is processed during EDMG channel estimation field (EDMG-CEF).

III. ALGORITHMS OF SYNCHRONIZATION AND CHANNEL ESTIMATION

The proposed synchronization and channel estimation process flow is depicted in Fig. 4. Initially, during the first segment of L-STF region, we utilize Golay correlation for preamble detection. Subsequently, first-stage timing recovery and coarse CFO/SCO estimation are conducted by analyzing the repetitive Golay correlation peaks. Boundary detection is then achieved by identifying the sign inversion of the correlation peaks at the end of the L-STF. Executing these steps enables effective coarse compensation, ultimately enhancing the precision of subsequent estimations.

Similarly, we make use of the EDMG-STF for second-stage timing recovery to achieve more accurate CFO/SCO estimation. Additionally, the EDMG-CEF is employed to detect the precursor timing, enabling the identification of an ISI-free region. Finally, Golay correlation is utilized to estimate the effective channel, and denoising methods are applied to mitigate the AWGN effect. Detailed operations of the algorithms for each step will be sequentially presented.

A. GOLAY CORRELATION BASED TWO-STEPS SYMBOL TIMING DETECTION

With the beamforming technique, the power of the entire CIR becomes concentrated on the main tone, we can estimate the precise timing of the distinct main tone through Golay cross-correlation, thereby obtaining the symbol timing. Symbol timing detection takes place during the L-STF and consists of two steps as follows:

1) FIRST STEP: POWER-NORMALIZED GOLAY CORRELATION

Inspired by [18], we propose a multi-stream synchronization technique based on power-normalized Golay correlation (P-NGC). This method leverages the properties of the Golay sequence, as described in (1), along with the sparse nature of the sub-THz channel. Specifically, the cross-correlation $\mathrm{XC}[n]$ between the received signal and the original Golay sequence exhibits a significant peak at the main tone of the channel, making it an ideal reference for signal detection. The N-point cross-correlation is expressed as:

$$\mathrm{XC}_{N_c}[n] = \frac{1}{N_c}\left\{ \begin{array}{l} \sum_{m=0}^{\frac{N_c}{2}-1} \left(A^*_{\frac{N_c}{2}}[m] r[n+m-N_A] \right) \\ + \sum_{m=0}^{\frac{N_c}{2}-1} \left(B^*_{\frac{N_c}{2}}[m] r[n+m-N_B] \right) \end{array} \right\} \quad (4)$$

where N_C represents the correlation length, while $A_{N_c/2}$ and $B_{N_c/2}$ denote Golay pairs, each with a length of $N_c/2$. The terms N_A and N_B correspond to the relative displacements required for alignment, and $r[n]$ represents the received signal.

Next, applying power normalization to the cross-correlation allows us to express the P-NGC for stream s as:

$$\text{P-NGC}\left[n^{(s)}\right] = \frac{\sum_{m=0}^{1} \left| \mathrm{XC}_{64}^{(s)}[n^{(s)}-m] \right|^2}{\frac{1}{64}\sum_{m=0}^{63} \left| r^{(s)}[n^{(s)}-m] \right|^2} \quad (5)$$

The normalization simplifies timing detection by enabling the use of a constant threshold, regardless of whether automatic gain control (AGC) has been applied. The peak of the normalized correlation serves as the signal arrival time for each stream.

Unlike the approach in [18], which relies on auto-correlation, our method focuses on cross-correlation to reduce overall system complexity. Furthermore, summing the powers of two successive correlations mitigates the dispersion of the Golay correlation's main-tone power across adjacent samples, particularly under fractional symbol timing offset (fSTO) conditions.

With the incorporation of the power normalization factor in (5), we can consistently detect the preamble using a constant threshold, regardless of the main-tone power. This detection process is described as:

$$n_c^{(s)} = min\left\{ n^{(s)} \middle| \text{P-NGC}\left[n^{(s)}\right] > P_{th} \right\} \quad (6)$$

where $n_c^{(s)}$ represents detected coarse symbol timing for the s-th stream in the first step, and P_{th} is the predefined power threshold.

2) SECOND STEP: THRESHOLD-BASED ADAPTIVE WINDOW SCANNING TECHNIQUE

However, the performance of the P-NGC algorithm is significantly influenced by the threshold selection and is susceptible to noise, leading to potential issues of false alarm or missed detection. To address these challenges, we propose a threshold-based adaptive window scanning (TBAWS) main-tone searching technique to enhance accuracy.

Initially, we set a relatively low threshold on P-NGC to enhance the probability of detection. Upon acquiring $n_c^{(s)}$, we establish a region to identify the maximum P-NGC value, as described as follow:

$$n_f^{(s)} = \underset{n^{(s)} \in R^{(s)}}{arg\ max}\ \text{P-NGC}\left[n^{(s)}\right] \quad (7)$$

where s represents the stream index, $n_f^{(s)}$ denotes the detected fine symbol timing. The scanning region, $R^{(s)}$, is defined as $\left\{n_c^{(s)}, n_c^{(s)}+1, n_c^{(s)}+2, \ldots, n_c^{(s)}+N_w\right\}$, where N_w indicates the window length, and is set as 64 points, corresponding to the repetition period of the correlation peak.

Finally, to mitigate the dispersion problem caused by fSTO effects, we compare the highest cross-correlation power between two successive correlation samples to determine the final main-tone timing, denoted as n_m:

$$n_m^{(s)} = \underset{\left\{n_f^{(s)}-m \mid m\in[0,1]\right\}}{arg\,max} \left|\mathrm{XC}_{64}^{(s)}\left[n_f^{(s)}-m\right]\right|^2 \tag{8}$$

The simulation results depicted in Fig. 5 show the success rate of preamble detection for each individual stream, with and without TBAWS main-tone searching technique. This approach clearly demonstrates a significant improvement in preamble detection success rates for both streams, particularly under low signal-to-noise ratio (SNR) conditions. With the introduction of this search window, even at an SNR as low as -5 dB, a 100% detection accuracy is achieved.

B. GOLAY CORRELATION BASED TWO-STAGE QUADRATIC REGRESSION TIMING RECOVERY FOR STO

To enable more precise estimation under the fSTO effect, we propose a two-stage timing recovery mechanism that exploits the response of the pulse shaping filter (PSF) to recover the timing of the main tone.

First, after detecting the symbol timing in the previous step, we select the sampled data around the main tone. Then, a quadratic regression polynomial model is iteratively applied to fit the correlation samples, gradually approaching the desired shape of the impulse, as depicted in Fig. 6. For each individual stream, the i-th iteration of the estimated CIR main cursor, $y^{(i)}[k]$, can be represented as:

$$y^{(i)}[k] = \mathrm{XC}_{N_c}\left[n_m + N_c(i-1) + x_k + \sum_{p=0}^{i-1}\hat{e}^{(p)}\right] \tag{9}$$

where k is the sample index, x_k is the k-th sample next to the main-tone, $\hat{e}^{(p)}$ is the estimated fractional timing error in the p-th iteration, and N_c is equal to 64 and 128 for first and second stage, respectively. The least squares (LS) fitting quadratic polynomial $f^{(i)}(x)$ and deviation $g^{(i)}$ can be expressed as

$$f^{(i)}(x) = \beta_0^{(i)} + \beta_1^{(i)}x + \beta_2^{(i)}x^2 \tag{10}$$

$$g^{(i)} = \sum\nolimits_k \left(y^{(i)}[k] - f^{(i)}(x_k)\right)^2 \tag{11}$$

Through the least squares fitting technique [19], we can get the coefficients of the polynomial as

$$\beta_0^{(i)} = \mu_{\boldsymbol{Y}}^{(i)} - \beta_1^{(i)}\mu_{\boldsymbol{X}}^{(i)} - \beta_2^{(i)}\mu_{\boldsymbol{X^2}}^{(i)} \tag{12}$$

$$\beta_1^{(i)} = \frac{C_{\boldsymbol{XY}}^{(i)}C_{\boldsymbol{X^2X^2}}^{(i)} - C_{\boldsymbol{X^2Y}}^{(i)}C_{\boldsymbol{XX^2}}^{(i)}}{C_{\boldsymbol{XX}}^{(t)}C_{\boldsymbol{X^2X^2}}^{(t)} - C^{2\,(t)}_{\boldsymbol{XX^2}}} \tag{13}$$

$$\beta_2^{(i)} = \frac{C_{\boldsymbol{X^2Y}}^{(i)}C_{\boldsymbol{XX}}^{(i)} - C_{\boldsymbol{XY}}^{(i)}C_{\boldsymbol{XX^2}}^{(i)}}{C_{\boldsymbol{XX}}^{(i)}C_{\boldsymbol{X^2X^2}}^{(i)} - C^{2\,(i)}_{\boldsymbol{XX^2}}} \tag{14}$$

where μ and C are the mean and cross-correlation operations, $\boldsymbol{X}$ is the sample space of the input time index x_k, $\boldsymbol{Y}$ is the sample space of the Golay correlation samples $y^{(i)}[k]$.

The estimated timing error in the i-th iteration $\hat{e}^{(i)}$ shown in Fig. 6 is the time index of the maximum value of $f^{(i)}(x)$, and it can be described as:

$$\hat{e}^{(i)} = \underset{x}{arg\,max}\, f^{(i)}(x) \tag{15}$$

By solving the differential equation, we can get the estimated timing error:

$$\frac{\partial f^{(i)}(x)}{\partial x} = \beta_1^{(i)} + 2\beta_2^{(i)}x = 0 \tag{16}$$

$$x = \hat{e}^{(i)} = -\frac{\beta_1^{(i)}}{2\beta_2^{(i)}} = -\frac{C_{\boldsymbol{XY}}^{(i)}C_{\boldsymbol{X^2X^2}}^{(i)} - C_{\boldsymbol{X^2Y}}^{(i)}C_{\boldsymbol{XX^2}}^{(i)}}{2(C_{\boldsymbol{X^2Y}}^{(i)}C_{\boldsymbol{XX}}^{(i)} - C_{\boldsymbol{XY}}^{(i)}C_{\boldsymbol{XX^2}}^{(i)})} \tag{17}$$

Finally, the estimation of the timing error is shown as follows:

$$\hat{e}^{(i)} = -\frac{\left\{\begin{matrix}(1-W_1)(\hat{y}^{(i)}[-1]-\hat{y}^{(i)}[1])\\ +W_1(\hat{y}^{(i-1)}[-1]-\hat{y}^{(i-1)}[1])\end{matrix}\right\}}{\left\{\begin{matrix}2(1-W_2)(\hat{y}^{(i)}[-1]-2\hat{y}^{(i)}[0]+\hat{y}^{(i)}[1])\\ +2W_2(\hat{y}^{(i-1)}[-1]-2\hat{y}^{(i-1)}[0]+\hat{y}^{(i-1)}[1])\end{matrix}\right\}} \tag{18}$$

$$\hat{y}^{(i)}[k] = Real\left\{y^{(i)}[k]y^{(i)^*}[0]\right\} \tag{19}$$

For hardware-friendly design, we simplify the timing error estimation by restricting the value of k to {-1, 0, 1}. To mitigate the impact of AWGN and non-ideal effects, we modify $y^{(i)}[k]$ as the Euclidean inner product between the given Golay correlation sample and the Golay correlation main-tone, as shown in (19). Additionally, two loop filters are applied to the estimated timing error to further reduce the AWGN effect during each iterative process. The loop filter coefficients, represented by W_1 and W_2, are carefully designed to be smaller than one, ensuring stability and reliable performance under the influence of AWGN.

In our system, a two-stage estimation process is employed, with the first stage in L-STF and the second stage in EDMG-STF. A key factor enhancing the overall performance is the compensation achieved during the first stage, which sets the foundation for improving the second-stage estimation. The main distinction between these stages lies in the Golay correlation length, which is 64 points in L-STF and 128 points in EDMG-STF. Once the L-STF is completed, we achieve the first stage timing recovery and obtain estimated coarse CFO/SCO values. These estimates enable us to effectively compensate for the CFO/SCO effects during the subsequent fields, particularly during EDMG-STF. With these non-ideal effects mitigated and the extended estimation length, EDMG-STF demonstrates superior performance. As shown in Fig. 7,

the second stage of timing recovery significantly improves the residual timing error from 10^{-1} to 10^{-4}, an enhancement of three orders compared to the first stage.

C. BOUNDARY DETECTION

The sign-inversed Golay sequence at the end of the L-STF is used for boundary detection. This inversion triggers a corresponding sign change in the correlation result, providing a reliable reference to detect the end of the sequence. The condition for boundary detection can be described as follows:

$$Re\left\{\mathrm{XC}_{64}^{(s)*}\left[n^{(s)}+64(l-1)\right]\mathrm{XC}_{64}^{(s)}\left[n^{(s)}+64l\right]\times\left(\sum_{m=1}^{l-1}\mathrm{XC}_{64}^{(s)*}\left[n^{(s)}+64(m-1)\right]\mathrm{XC}_{64}^{(s)}\left[n^{(s)}+64m\right]\right)^{*}\right\}<0 \tag{20}$$

where s is the stream index, and l indicates l-th correlation peaks.

In our approach, we adopt a technique that leverages the repetitive auto-correlation peaks to mitigate the CFO effect. Additionally, we accumulate correlation results to suppress noise and combine results from different streams to enhance performance. This approach achieves a boundary detection success rate of up to 100% when SNR exceeds -5 dB in both streams, as depicted in Fig. 8.

D. GOLAY CORRELATION BASED COARSE AND FINE STREAM-COMBINED CFO/SCO ESTIMATION

Unlike the method in [18], which uses the auto-correlation (AC) of the received signal, we leverage the auto-correlation of the cross-correlation result, thereby reducing hardware overhead by reusing the cross-correlation output. This approach is expressed as:

$$\begin{aligned}\mathrm{AC}[n] &= \mathrm{XC}_{N_C}^{*}[n]\times\mathrm{XC}_{N_C}[n+N_C]\\ &= e^{N_C\times\theta_{CFO}}+\epsilon[n]+\epsilon[n+N_c]\end{aligned} \tag{21}$$

where N_C represents the correlation length, θ_{CFO} denotes the phase error to be estimated and ϵ is the error term due to AWGN.

By exploiting the repetitive Golay correlation peaks in the L-STF, we can suppress noise through accumulated correlation results. The multi-stream CFO estimation method is as follows:

$$\hat{\theta}_{CFO}=\frac{1}{N_C}\times\angle\left\{\sum_{s}\sum_{m}\left(\mathrm{XC}_{N_C}^{(s)^{*}}\left[n^{(s)}+N_C\times(m-1)\right]\times\mathrm{XC}_{N_C}^{(s)}\left[n^{(s)}+N_C\times m\right]\right)\right\} \tag{22}$$

where $\hat{\theta}_{CFO}$ is the estimated CFO, s presents the stream index, and N_c is equal to 64 and 128 for coarse and fine estimation, respectively.

Our algorithm further reuses the auto-correlation of repetitive correlation peaks, enabling efficient integration of the optimized Golay correlator (OGC) [20] within modules for symbol timing synchronization and frequency offset estimation, resulting in a streamlined and effective design.

To avoid frequency ambiguity, we specifically set N_C to 64 for coarse CFO estimation in L-STF. Additionally, the accumulation of auto-correlation results effectively suppresses the noise effect, further enhancing the performance of the CFO estimation process. Furthermore, to mitigate noise effectively, we adopt a maximum ratio combining approach to combine the estimated CFO values obtained from different streams.

The fine CFO estimation takes place in EDMG-STF, where the estimation algorithm remains the same as (20). The major distinction is that coarse CFO compensation has been completed at this period, preventing severe influence from frequency ambiguity. Consequently, N_C can be set to 128 points, enabling more precise and accurate estimation results. This technique yields improved noise immunity and enhances the accuracy of the CFO estimation process. As a result, the mean square error (MSE) of CFO estimation can be as low as 10^{-5}, as shown in Fig. 9.

For SCO estimation, since the carrier and the sampling clock are derived from the same reference oscillator [21], we can estimate SCO by:

$$\hat{\delta}_{SCO}=\frac{\hat{\theta}_{CFO}}{2\pi f_c T_s} \tag{23}$$

where $\hat{\delta}_{SCO}$ is the estimated SCO, f_c is the carrier frequency, and T_S is the sample period.

E. TIMING SYNCHRONIZATION REFINEMENT

Although we accurately detect the CIR main-tone timing during symbol timing synchronization, it is essential to identify the CIR first path precursor timing before channel estimation due to the following reasons:

1) ISI-FREE REGION

Fig. 10 illustrates that if there are precursor samples in the CIR, selecting the main-tone timing as the start timing of the FFT window for frequency-domain (FD) digital combining and equalization will lead to inter-symbol interference (ISI).

2) SAFE RANGE OF GOLAY CORRELATION

Effective channel estimation relies on the complementary correlation property of the Golay sequence. However, the range of the zero-correlation region, crucial for maintaining the orthogonality of the Golay sequence, is impacted by the multipath effect, leading to channel estimation errors, as shown in Fig. 11. Due to this phenomenon, we must limit the correlation range according to the channel delay spreads to ensure estimation accuracy.

Therefore, detecting the timing of the first path precursor, appropriately adjusting the synchronized timing, and identifying the correct correlation region before channel estimation are crucial for achieving high performance.

We propose a power ratio precursor detection technique that establishes a search window before the main tone and compares the power between the main tone and n-th tap within this window to detect the true channel taps. The proposed detection process is expressed as follows:

$$n_r^{(s)} = \underset{\{n \in search\ window\}}{arg\ min} \{n \mid 10\ log_{10} \frac{P_m^{(s)}}{P_n^{(s)}} < P_t\} \tag{24}$$

where s is the stream index, $n_r^{(s)}$ represents the estimated first path time index, i.e., refined timing of the system. $P_m^{(s)}$ denotes the estimated power of main-tone, $P_n^{(s)}$ indicates the estimated power of n-th channel tap, and P_t is a predefined threshold.

Finally, a joint ISI-free timing index, n_t, can be obtained through the estimated refined timing of all streams, described as:

$$n_t = min\left\{n_r^{(s)}\right\}, \quad 1 \le s \le N_s \tag{25}$$

where N_s is the total number of streams.

F. Effective Channel Estimation and Denoising

The effective channel estimation can be achieved by zero cross correlation property as mentioned in (2)(3). By combining different sets of receive data with clean Golay sequence, we can obtain effective channel responses from different paths.

As EDMG-CEF includes two 512-point Golay pairs, we can estimate the CIR twice and then take the average of the two estimates to mitigate noise. Furthermore, to enhance performance, we employ a threshold-based denoising method, as described below:

$$\hat{h}_d^{ij}[n] = \begin{cases} \hat{h}_e^{ij}[n], & if\ \left|\hat{h}_e^{ij}[n]\right|^2 > \lambda^{ij} \\ 0, & otherwise \end{cases} \tag{26}$$

where i and j represent the indices of the received and transmitted streams, respectively, $\hat{h}_e$ donates the estimated channel, $\hat{h}_d$ represents the estimated channel after denoising technique, and λ^{ij} indicates the threshold value corresponding to the stream pair.

In our specific system environment, we evaluate the performance of various algorithms, as depicted in Fig. 12. Ultimately, we opt for the two-stage universal thresholding method [14] due to its superior performance in channels with sparsity and its ability to operate without prior knowledge of channel statistics (KCS) parameters.

The algorithmic flow of the method is illustrated in Fig. 13 with a two-stage approach. In the first stage, the estimated noise standard deviation is utilized to filter out potential real channel taps. This step is crucial to mitigate bias in noise standard deviation estimation, particularly at higher SNR levels where real channel taps can introduce such bias. By excluding real channel, the remaining signal are treated as noise samples, resulting in a more accurate estimation of the noise standard deviation. The threshold is calculated based on the estimated noise statistics as follows:

$$\hat{\sigma}_w^2 = \sqrt{2} \frac{median(|\hat{w}[n]|^2)}{\sqrt{ln\ 4}} \tag{27}$$

where $\hat{\sigma}_w^2$ is the estimated noise variance, and $\hat{w}[n]$ denotes the estimated noise samples, represented as channel taps, $\hat{h}_e^{ij}$, in the first stage and noise taps, $\hat{n}_e^{ij}$, in the second stage.

IV. HARDWARE ARCHITECTURE DESIGN

A. ARCHITECTURE AND PROCESS FLOW

The hardware architecture, illustrated in Fig. 14, incorporates pipelining techniques in each module to achieve a 1.76 GHz chip rate. The notation SI.F on each signal line indicates sign bit S, I-bit integer word length (IWL), and F-bit fractional word length (FWL). Moreover, to reduce hardware complexity, all detection and estimation modules efficiently reuse the shared OGC outputs. The process flow is described as follows.

1) PREAMBLE DETECTION IN L-STF

In the initial state, the multiplexer is switched to 0. The preamble detection module uses the correlation results to detect the main-tone timing. Once the preamble is detected, the multiplexer will be switched to 1.

2) FIRST STAGE TIMING RECOVERY AND CFO/SCO ESTIMATION IN L-STF

When the multiplexer is switched to 1, the first stage timing recovery and CFO/SCO estimation are conducted. The cubic B-spline interpolator in Farrow structure [22] is used to compensate the fractional sample error. The Coordinate Rotation Digital Computer (CORDIC) in vectoring mode is adopted to calculate the phase offset in CFO/SCO estimation module. After detecting the boundary of L-STF, the multiplexer will be switched to 2.

3) SECOND STAGE TIMING RECOVERY AND CFO/SCO ESTIMATION IN EDMG-STF

When the multiplexer is switched to 2, the second stage processing is carried out by using the coarse CFO/SCO compensated EDMG-STF. The CORDIC in CFO/SCO estimation module is shared to compensate the phase error, and the First In First Out (FIFO) is used to compensate the accumulated integer sample error. Once the counter counts to the end of EDMG-STF, the multiplexer will be switched to 3.

4) PRECURSOR DETECTION AND EFFECTIVE CHANNEL ESTIMATION/DENOISING IN EDMG-CEF

When the multiplexer is switched to 3, the fine CFO/SCO compensated EDMG-CEF is used to detect the precursor timing. Once the precursor is detected, the estimated CIR samples are sent into the denoising module. Finally, the denoised effective CIR and the compensated payload are processed by the digital combiner.

B. PROPOSED SHARED OPTIMIZED GOLAY CORRELATOR

In [20], an OGC structure is proposed for Golay correlation. This system requires OGC structures with three different

correlation lengths: 64, 128, and 512 points. Specifically, 64-point correlation is used for preamble detection, first stage timing recovery, and coarse CFO/SCO estimation in the L-STF. 128-point correlation is employed for the fine CFO/SCO estimation and second stage timing recovery in the EDMG-STF, while 512-point correlation is utilized for time domain effective channel estimation in the EDMG-CEF.

Due to the high compatibility of this correlation structure, we propose a shared OGC structure, as illustrated in Fig. 15, to reduce hardware overhead. The figure only illustrates the beginning and end of the shared OGC structure, omitting the repetition of the basic OGC units in the middle for simplicity. Several multiplexers are inserted to select the correct inputs for correlation in L-STF, EDMG-STF, and EDMG-CEF. The synthesis result using the TSMC CMOS 16nm FinFET Compact process shows that the gate count is significantly reduced from 242.3k to 186.2k with the sharing technique, as depicted in Table II, resulting in a remarkable 23% reduction in hardware usage.

C. TWO-STAGE QUADRATIC REGRESSION TIMING RECOVERY

The block diagram of the two-stage timing error detection for one stream is illustrated in Fig. 16. The primary computational expenses include the 6 multiplications for the Euclidean inner products and the division needed to generate the timing error result. To reduce hardware utilization without compromising error rate estimation, appropriate quantization has been introduced. Additionally, to achieve the 1.76 GHz clock rate, the divider is designed with two pipelined stages, and the overall output corresponds to the timing error as shown in (18).

D. DUAL MODE CORDIC

We adopt the CORDIC in vectoring mode to estimate the CFO, and it can be shared to compensate for the phase error of data in rotation mode. Fig. 17 shows the block diagram of the dual-mode CORDIC [23].

The CORDIC process ensures the angle is within the range [-π/2, π/2]. It starts with an initial stage to map coordinates between quadrants and performs angle pre-processing. Then, rotation stages update the coordinates and angles, followed by a scaling stage to adjust the vector amplitude and an angle post-processing stage compensates for the rotation angle.

E. NOVEL EFFECTIVE CHANNEL DENOISING ARCHITECTURE

To realize the median function in (26), the traditional approach involves using a comparison-based sorting algorithm with a lower bound complexity of $O(n \log n)$, where n is the amount of data. However, this approach demands a significant number of comparisons to sort a series of input samples.

To address this, we propose an indexing-count method from a hardware perspective. This method treats the input sample values as array indexes and increments corresponding counters based on the signal magnitudes to provide two significant benefits. Firstly, it achieves linear complexity $O(n+k)$, where k is determined by the range of input values. Secondly, the length of the noise samples required for subsequent calculations can be directly obtained from the value of the counters.

The analysis shows that in our system environment, a 6-bit representation (equivalent to 64 counters) is adequate for representing the median power value of noise samples. In the worst-case scenario, we need to arrange 129 data points. Therefore, with n set to 129 and k to 64, the indexing-count method demonstrates almost five times greater efficiency compared to comparison-based approaches.

After determining the number of noise samples through simulation analysis, we establish a lookup table structure for calculating the $\ln(\cdot)$ value.

These approaches facilitate a straightforward and highly efficient hardware design, as illustrated in Fig. 18.

F. HARDWARE DESIGN RESULTS

To achieve the desired 1.76 GHz chip rate, we utilize pipelining techniques in the hardware architecture. For a two-stream transmission with 64-QAM modulation, we successfully attain a throughput of 21.21 Gb/s. To optimize the hardware, the Golay correlator employs efficient resource utilization, and an indexing-count method is proposed to reduce the hardware complexity of the sorting algorithm. We employ IC Compiler from Synopsys for circuit synthesis. Table III summarizes the overall proposed design. The gate count is calculated based on NAND2 cell with an area equal to 0.2 um^2. The power measurements are conducted using the PrimeTime tool.

The bit error rate (BER) performance results shown in Fig. 19 demonstrate that the proposed system meets the required specifications. In this figure, the target BER is represented by a green dashed line, while the blue and red dashed lines indicate the target SNRs for the 16-QAM and 64-QAM scenarios, respectively. According to the receiver sensitivity specified for each modulation and coding scheme defined in IEEE Std. 802.15.3d, the BER should be below 10^{-12} at SNRs of 19.6 dB for 16-QAM and 25.6 dB for 64-QAM. Based on previous work, a low-density parity-check (LDPC) decoder provides an approximate 10^{8} coding gain for IEEE Std. 802.15.3d [24]. With this coding gain, the system can meet the required performance as long as the uncoded BER remains below 1.96×10^{-4} at the specified SNRs.

V. CONCLUSION

In this paper, we proposed a design for a two-stream synchronizer and channel estimator specifically tailored for sub-THz channels. Our approach, which leverages main-tone-based Golay correlation, has proven effective in sub-THz channels with hybrid structures incorporating beamforming techniques. To enhance accuracy, we introduced new techniques, such as window searching and quadratic regression in timing recovery. Our design effectively handles frequency offsets up to 60 ppm within the sub-THz range, addressing both CFO and SCO effects. Simulation results indicate that our design meets the uncoded BER requirements

at target SNR levels as specified by IEEE Std. 802.15.3d, supporting efficient two-stream transmission.

From a hardware perspective, our shared Golay correlator architecture achieves a 23% reduction in complexity, while a simplified denoising structure based on a counting technique improves efficiency by reducing the number of sorting operations fivefold. Overall, we present a low-complexity baseband module capable of synchronization and channel estimation specifically designed for sub-THz channels, achieving a system throughput of 21.21 Gb/s. This design offers significant potential for future high-speed, high-performance wireless communication systems, with promising applications in next-generation networks.

Additionally, our correlator architecture can be adapted to support higher-order MIMO configurations. By incorporating additional Golay correlators and expanding the summation to include a larger set of correlation terms, interference from additional data streams can be effectively mitigated. As circuit technology advances to support higher-speed operations, our approach could also be extended to accommodate broader frequency bands. This work demonstrates that MIMO extensions can be effectively applied in sub-THz environments based on current standards, verifying the feasibility of achieving expected performance in future sub-THz systems. Thus, this research lays a foundational step toward more scalable and efficient solutions in the evolving landscape of wireless communication technology.

REFERENCES

[1] V. Petrov, T. Kurner and I. Hosako, "IEEE 802.15.3d: First Standardization Efforts for Sub-Terahertz Band Communications toward 6G," in *IEEE Communications Magazine*, vol. 58, no. 11, pp. 28-33, November 2020.

[2] "IEEE Standard for High Data Rate Wireless Multi-Media Networks--Amendment 2: 100 Gb/s Wireless Switched Point-to-Point Physical Layer," in *IEEE Std 802.15.3d-2017 (Amendment to IEEE Std 802.15.3-2016 as amended by IEEE Std 802.15.3e-2017)*, vol., no., pp.1-55, 18 Oct. 2017.

[3] "IEEE Standard for High Data Rate Wireless Multi-Media Networks," in *IEEE Std 802.15.3-2016 (Revision of IEEE Std 802.15.3-2003*, vol., no., pp.1-510, 25 July 2016.

[4] N. Maletic, L. Lopacinski, M. Goodarzi, M. Eissa, J. Gutierrez and E. Grass, "A Study of LOS MIMO for Short-Range Sub-THz Wireless Links," *Mobile Communication - Technologies and Applications; 25th ITG-Symposium*, Osnabrueck, Germany, 2021, pp. 1-6.

[5] S. Bicaïs, A. Falempin, J. -B. Doré and V. Savin, "Design and Analysis of MIMO Systems Using Energy Detectors for Sub-THz Applications," in *IEEE Transactions on Wireless Communications*, vol. 21, no. 6, pp. 3678-3690, June 2022.

[6] D. Q. Nguyen, A. Ashikhmin, H. Yang and T. Kim, "No Analog Combiner TTD-Based Hybrid Precoding for Multi-User Sub-THz Communications," *ICC 2024 - IEEE International Conference on Communications*, Denver, CO, USA, 2024, pp. 1813-1818.

[7] M. Saad, N. Al Akkad, H. Hijazi, A. C. Al Ghouwayel, F. Bader and J. Palicot, "Novel MIMO Technique for Wireless Terabits Systems in Sub-THz Band," in *IEEE Open Journal of Vehicular Technology*, vol. 2, pp. 125-139, 2021.

[8] "IEEE Standard for Information Technology--Telecommunications and Information Exchange between Systems Local and Metropolitan Area Networks--Specific Requirements Part 11: Wireless LAN Medium Access Control (MAC) and Physical Layer (PHY) Specifications Amendment 2: Enhanced Throughput for Operation in License-exempt Bands above 45 GHz," in *IEEE Std 802.11ay-2021 (Amendment to IEEE Std 802.11-2020 as amendment by IEEE Std 802.11ax-2021)*, vol., no., pp.1-768, 28 July 2021.

[9] S. Ju, Y. Xing, O. Kanhere and T. S. Rappaport, "Millimeter Wave and Sub-Terahertz Spatial Statistical Channel Model for an Indoor Office Building," in *IEEE Journal on Selected Areas in Communications*, vol. 39, no. 6, pp. 1561-1575, June 2021.

[10] J. J. van de Beek, O. Edfors, M. Sandell, S. K. Wilson, and P. O. Borjesson, "On channel estimation in OFDM systems," in *Proc. IEEE Vehicular Technology Conf.*, vol. 2, Chicago, IL, July 1995, pp. 815–819.

[11] C. F. Wu, W. C. Liu, C. C. Tsui, C. Y. Liu, M. S. Sie and S. J. J. Jou, "Golay-Correlator Window-Based Noise Cancellation Equalization Technique for 60-GHz Wireless OFDM/SC Receiver," in *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 11, pp. 3323-3333, Nov. 2016.

[12] Y. Kang, K. Kim, and H. Park, "Efficient DFT-based channel estimation for OFDM systems on multipath channels," Communications, IET, vol.1, no.2, pp.197,202, April 2007.

[13] P. Sure and C. M. Bhuma, "Weighted-noise threshold based channel estimation for OFDM systems," *Sadhana*, vol. 40, no. 7, pp. 2111–2128, Oct. 2015.

[14] H. Xie, G. Andrieux, Y. Wang, J.F. Diouris, and S. Feng, "Efficient time domain threshold for sparse channel estimation in OFDM system," *AEU Int. J. Electron. Commun*., vol. 68, no. 4, pp. 277–281, 2014.

[15] Artyom Lomayev *et al*., "EDMG STF and CEF Design for SC PHY in 11ay," IEEE 802.11 Documents, Jul. 2016. [Online]. Available: https://mentor.ieee.org/802.11/documents?is_dcn=SSW&is_group=00ay

[16] O. E. Ayach, S. Rajagopal, S. Abu-Surra, Z. Pi and R. W. Heath, "Spatially Sparse Precoding in Millimeter Wave MIMO Systems," in IEEE Transactions on Wireless Communications, vol. 13, no. 3, pp. 1499-1513, March 2014

[17] M. J. E. Golay, "Complementary Series," IRE Trans. Inform. Theory, IT-7, pp. 82-87, Apr. 1961.

[18] C. Y. Liu *et al*., "Dual-Mode All-Digital Baseband Receiver With a Feed-Forward and Shared-Memory Architecture for Dual-Standard Over 60 GHz NLOS Channel," in *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 64, no. 3, pp. 608-618, March 2017

[19] E. Weisstein, "Least Squares Fitting," Web resource from MathWorld. [Online]. Available: http://mathworld.wolfram.com/LeastSquaresFitting.html

[20] P. G. Donato, M. A. Funes, M. N. Hadad, and D. O. Carrica, "Optimised Golay correlator," *IEE Electron. Lett*., vol. 45, pp. 380–381, Mar. 2009.

[21] *IEEE Standard for High Data Rate Wireless Multi-Media Networks*, IEEE Standard 802.15.3-2016 (Revision of IEEE Std 802.15.3), 2016, pp. 1–510.

[22] C. W. Farrow, "A continuously variable digital delay element," *1988., IEEE International Symposium on Circuits and Systems*, 1988, pp. 2641-2645 vol.3.

[23] E. Grass, B. Sarker and K. Maharatna, "A dual-mode synchronous/asynchronous CORDIC processor," *Proceedings Eighth International Symposium on Asynchronous Circuits and Systems*, 2002, pp. 76-83.

[24] T. H. Wu, C. L. Yeh, Y. S. Huang and S. J. Jou, "A 128 Gb/s LDPC Decoder Using Partial Syndrome-based Dynamic Decoding Scheme for Terahertz Wireless Multi-Media Networks," *2024 IEEE International Symposium on Circuits and Systems (ISCAS)*, Singapore, Singapore, 2024, pp. 1-5.

Chung-Lun Tu received the B.S. degree in Physics from the National Central University, Taoyuan, Taiwan, in 2016. He is currently working toward the Ph.D. degree in the Electronics Engineering Department, National Yang Ming Chiao Tung University, Taiwan.

His research interests include digital wireless communication systems, digital signal processing and digital VLSI systems design.

This article has been accepted for publication in IEEE Open Journal of Circuits and Systems. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2024.3510921

Chen-Yuan Tseng received the B.S degree in electronics engineering from the National Central University, Taoyuan, Taiwan, in 2020, and the M.S. degree in electrical engineering from National Yang Ming Chiao Tung University, Hsinchu, Taiwan, in 2022.

His research interests include digital signal processing and digital VLSI design.

Wei-Che Lee received the B.S degree in electronics engineering from National Cheng Kung University, Tainan, Taiwan, in 2015, and the M.S. degree in electrical engineering from National Chiao Tung University, Hsinchu, Taiwan, in 2017. His research interests include digital signal processing and wireless baseband processing.

He is currently an Engineer in the wireless communication technology chip development department of MediaTek.

Kang-Lun Chiu received the B.S. degree in electrical engineering from National Dong Hua University, Taiwan in 2015. and the Ph.D. degree in electrical engineering from National Yang Ming Chiao Tung University, Hsinchu, Taiwan, in 2023. His research interests include digital wireless communication systems, digital signal processing and digital VLSI systems design.

He is currently an Engineer in the connectivity technology chip development department of MediaTek.

Pei-Yun Tsai (Member, IEEE) received the B.S., M.S., and Ph.D. degrees in electrical engineering from the National Taiwan University, Taipei, Taiwan, in 1994, 1996, and 2005, respectively.

From 1996 to 2000, she worked at ASUStek, Taipei. She is currently a Professor of Electrical Engineering with the National Central University, Taoyuan, Taiwan. Her research interests include digital signal processing algorithms and VLSI design for wireless communication systems and biomedical systems.

Prof. Tsai has received the Acer Longtern Award and the First Asian Solid-State Circuit Conference Student Design Contest Outstanding Award in 2005. She has also received the Macronix International Corporation (MXIC) Golden Silicon Award in 2005, 2010, and 2016. In 2011 and 2014, she received the Outstanding Chip Design Award Honorable Mention from the Chip Implementation Center, Taiwan. Since 2013, she has been serving as a TC Member for International Symposium on Circuits and Systems (ISCAS) Visual Signal Processing and Communications (VSPC) Track. Since 2015, she has been serving as a TPC Member for the Asian Solid-State Circuits Conference (ASSCC) in SoC Subcommittee and also a TC Member for Signal Processing Systems of the Asian–Pacific Signal and Information Processing and Association (APSIPA). Since 2016, she has been serving as a TC Member for the Design and Implementation of Signal Processing Systems (DISPS) of the IEEE Signal Processing Society.

Shyh-Jye Jou (Senior Member, IEEE) received the M.S. and Ph.D. degrees in electronics from the National Chiao Tung University, Hsinchu, Taiwan, in 1984 and 1988, respectively. From 1990 to 2004, he joined the Electrical Engineering Department, National Central University, Taoyuan, Taiwan, and became a Professor in 1997. Since 2004, he has been a Professor with the Electronics Engineering Department, National Chiao Tung University, and served as the Chairperson from 2006 to 2009. He was appointed as the Director General of the Ministry of Science and Technology in charge of the Science Education and International Cooperation Department from January 2016 to December 2017. He was a Visiting Research Professor with the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, Champaign, IL, USA, from 1993 to 1994 and 2010 academic years. In the summer of 2001, he was a Visiting Research Consultant with the Communication Circuits and Systems Research Laboratory, Agere Systems, Allentown, PA, USA. He has published more than 100 IEEE journal and conference papers. His research interests include design and analysis of high speed, low power mixed-signal integrated circuits, and communication and bio-electronics integrated circuits and systems.

Dr. Jou received the Outstanding Engineering Professor Award from the Chinese Institute of Engineers in 2011 and the Chinese Institute of Electrical Engineering in 2013. He has served as the Chapter Chair for the IEEE Circuits and Systems Society Taipei Chapter in 2006 and a Guest Editor for IEEE JOURNAL OF SOLID STATE CIRCUITS in November 2008. He was the Track Chair of Nanoelectronics and Gigascale Systems from 2011 to 2013. He also serves as the Conference Chair and the TPC Chair for many IEEE conferences, such as the Conference Chair for IEEE VLSI Design Automation and Test (VLSI-DAT) and the International Workshop on Memory Technology, Design, and Testing. He has also served as the Technical Program Chair or the Co-Chair for IEEE VLSI-DAT, the International IEEE Asian Solid-State Circuit Conference, and the IEEE Biomedical Circuits and Systems. He has served as the Distinguished Lecturer for the Circuits and Systems (CAS) Society from 2009 to 2010.

This article has been accepted for publication in IEEE Open Journal of Circuits and Systems. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2024.3510921

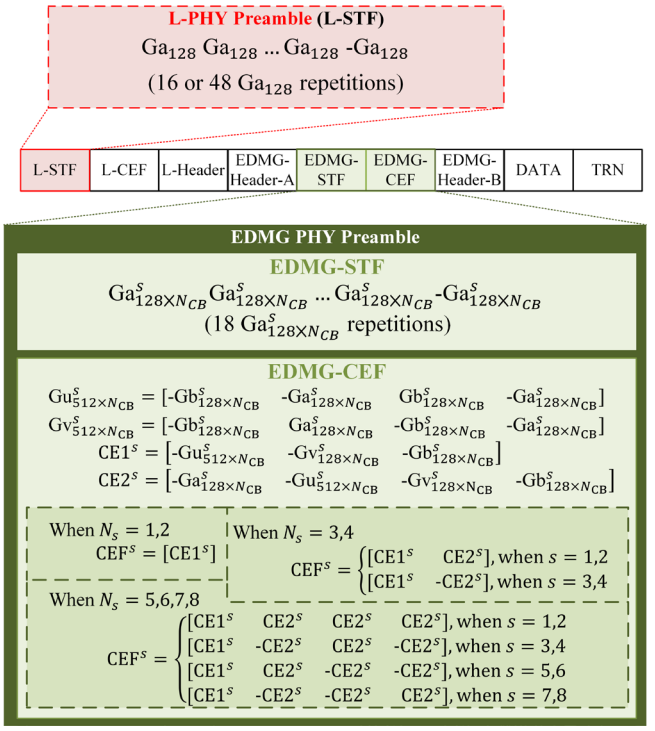

FIGURE 1. Multi-stream frame structure of IEEE 802.11ay.

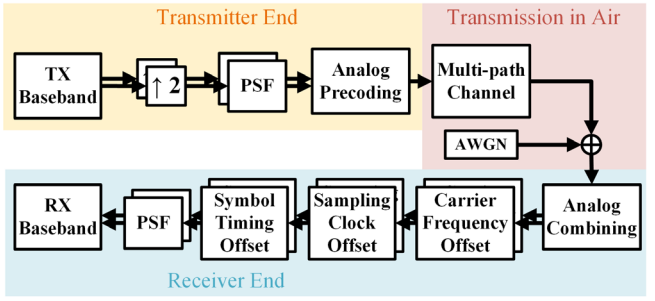

FIGURE 2. System simulation block diagram.

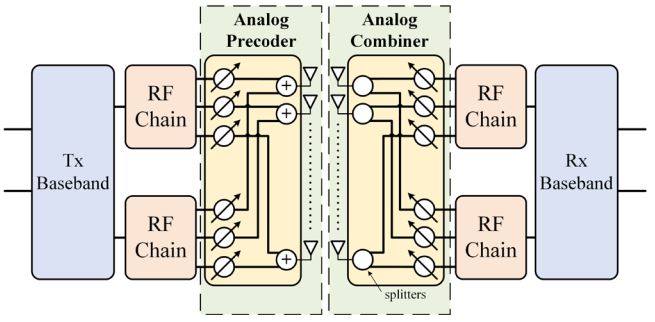

FIGURE 3. Block diagram of a typical hybrid beamforming structure.

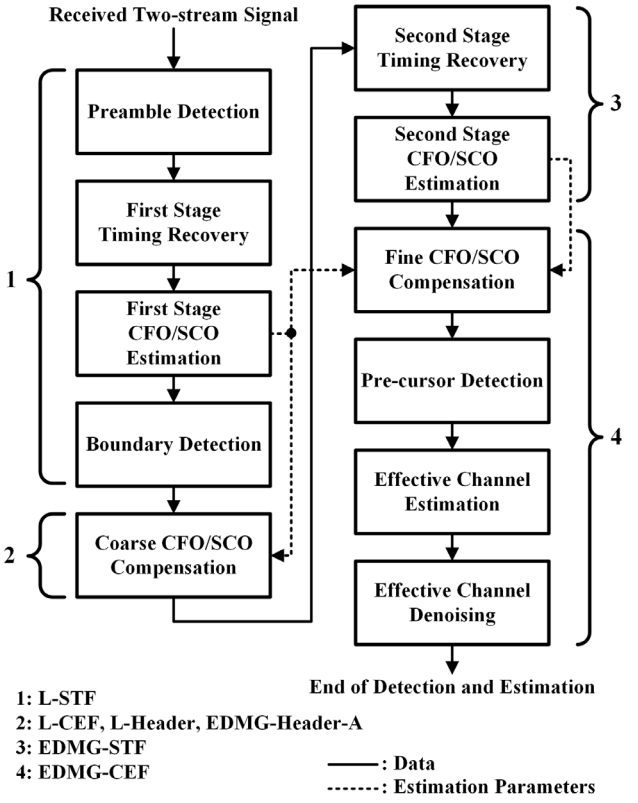

FIGURE 4. The process flow of the proposed synchronization and channel estimation design.

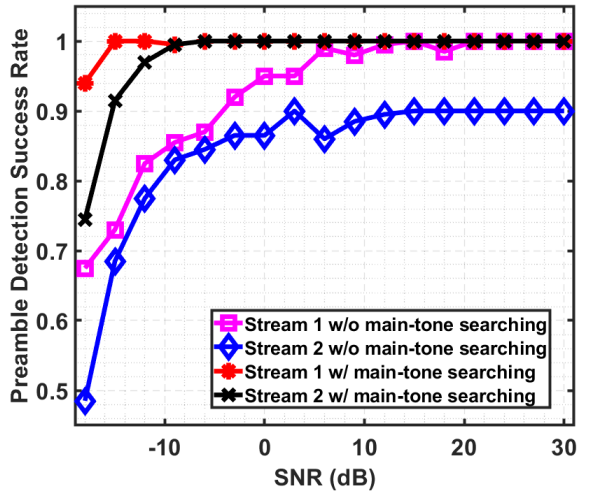

FIGURE 5. Preamble detection success rate for each stream with/without main-tone searching.

This article has been accepted for publication in IEEE Open Journal of Circuits and Systems. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/OJCAS.2024.3510921

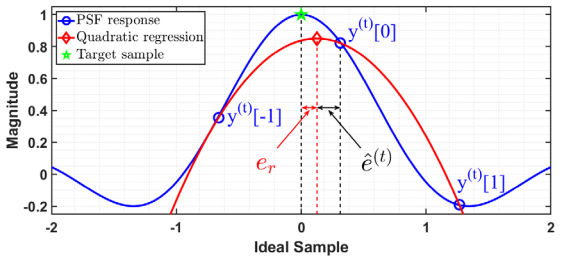

FIGURE 6. PSF response under fractional STO effect and the illustration of the quadratic regression approach.

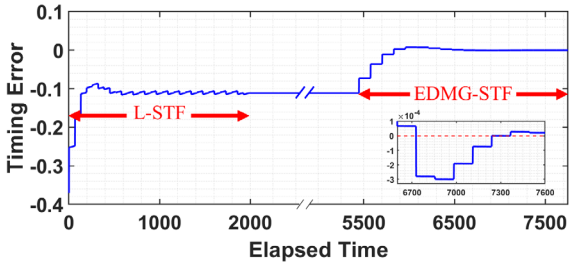

FIGURE 7. The residual timing error vs. elapsed time.

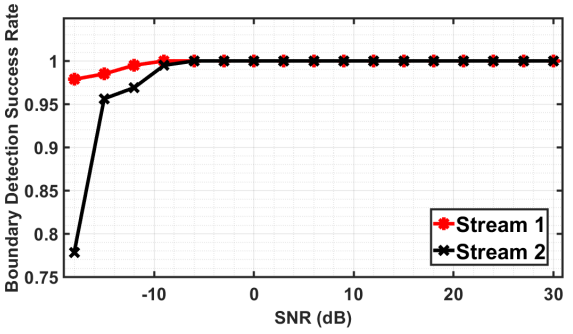

FIGURE 8. Boundary detection success rate vs. SNR.

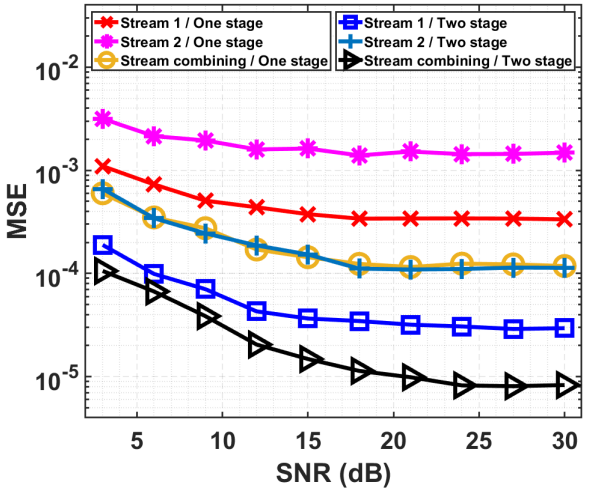

FIGURE 9. MSE of CFO estimation with/without stream combining in one stage/two stage manner.

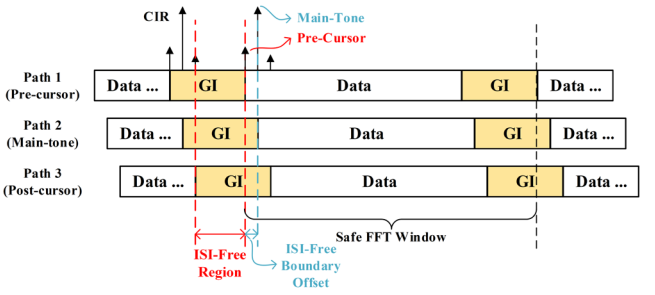

FIGURE 10. Illustration of the ISI-free boundary range.

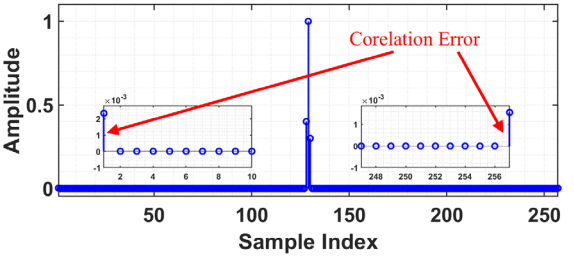

FIGURE 11. Correlation results in the presence of multipath effect.

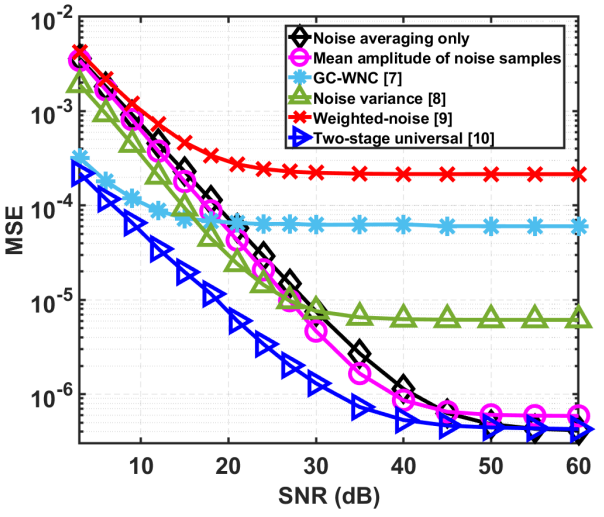

FIGURE 12. MSE of channel estimation results for several denoising methods.

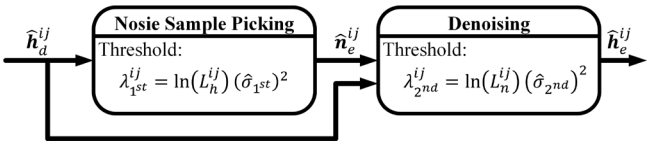

FIGURE 13. Two-stage universal threshold denoising flow [14].

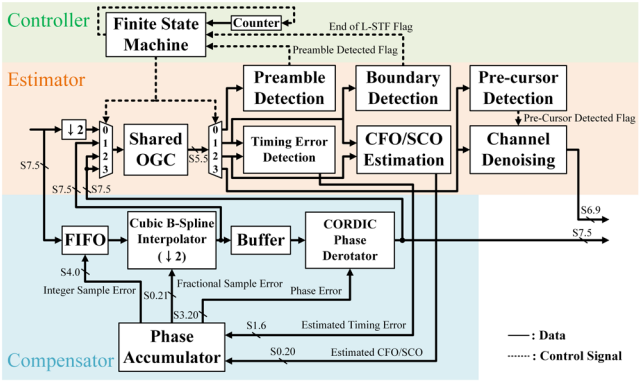

FIGURE 14. Block diagram of the overall design.

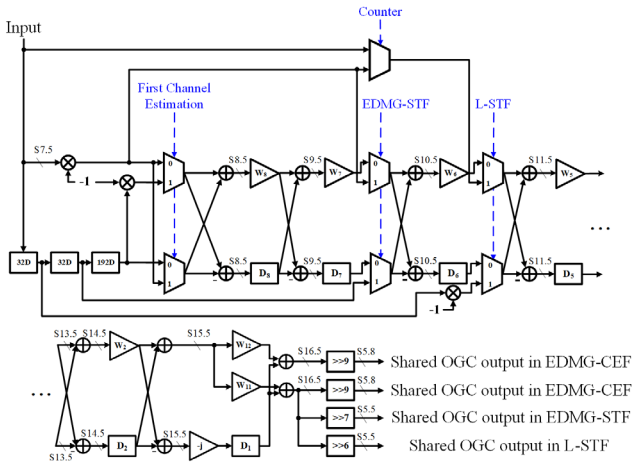

FIGURE 15. The block diagram of the shared OGC structure.

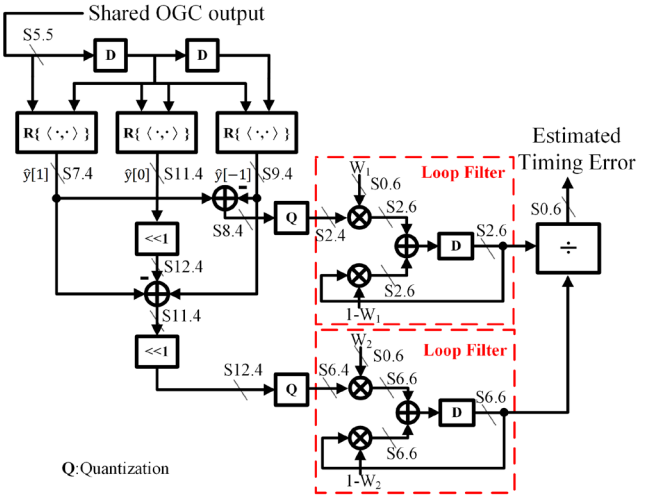

FIGURE 16. The block diagram of the quadratic regression timing recovery technique.

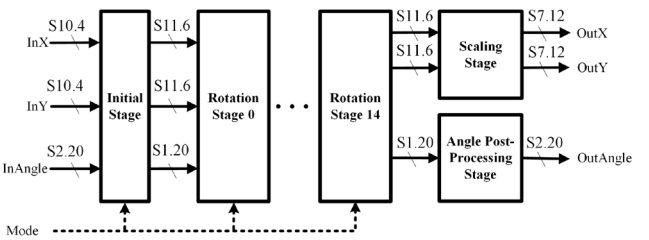

FIGURE 17. The block diagram of the dual mode CORDIC.

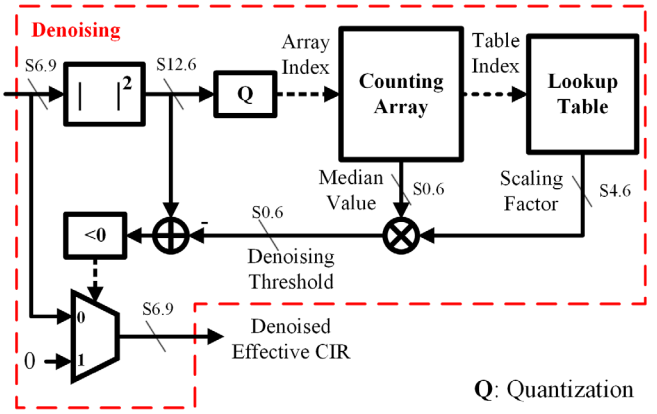

FIGURE 18. The block diagram of the proposed effective channel denoising design.

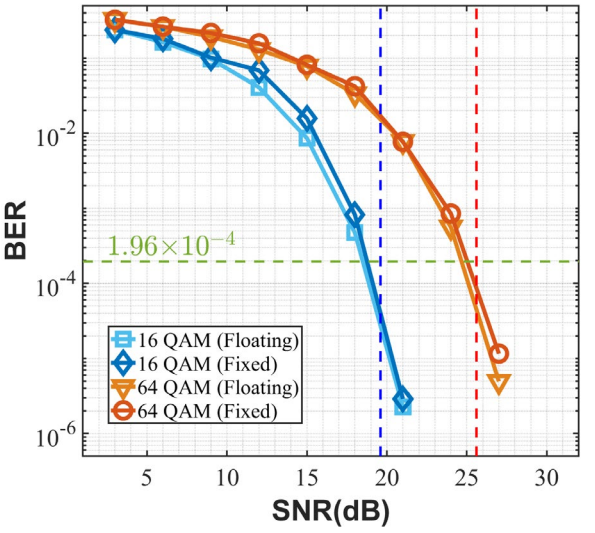

FIGURE 19. Floating-point and fixed-point BER simulation results.

TABLE 1
SUMMARY OF SYSTEM PARAMETERS

Specification	Sub-THz MIMO
Transmission	Single Carrier
Number of stream	2
Carrier Frequency	150 GHz
Modulation	π/2 16/64-QAM
Channel Coding	14/15 LDPC
Training Sequence	Golay Code
Bandwidth of each stream	1.76 GHz
Max. Frequency Offset	60 ppm

TABLE 2
GATE COUNTS OF OGC STRUCTURES WITH AND WITHOUT SHARING FOR ONE STREAM

	Without Sharing			With Sharing
Gate Counts (k)	64-point	128-point	512-point	269.9
	26.8	60.9	263.6	
	Total: 351.3			

TABLE 3
SUMMARY OF THE TWO-STREAM SYNCHRONIZATION AND CHANNEL ESTIMATION DESIGN

Process	CMOS 16nm FinFET	
Transmission Mode	SC	
Modulation	16-QAM	64-QAM
Clock Rate	1.76 GHz	
Throughput (Gb/s)	14.08	21.21
Synthesis Result	Latency	119 cycles (67.6 ns)
	Gate Count	737.9 k
	Power	370.0 mW