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射頻週邊掃描技術

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執行單位：國立臺灣大學電信工程學研究所

計畫主持人：黃天偉

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（一）計畫中文摘要。

關鍵字：射頻週邊掃描、射頻積體電路、射頻系統晶片、系統晶片測試

本計畫開發射頻週邊掃描技術，週邊掃描（IEEE 1149.1）已廣泛使用於數位系統中，可大幅提昇整個系統的可測試性，以及降低測試的成本，本計畫將擴大週邊掃描的涵蓋範圍由數位電路擴展至射頻電路（如 5 GHz WLAN），目前有許多新的週邊掃描測試標準的開發（IEEE 1149.4/1149.6），都希望能擴展週邊掃描至類比電路（<1 MHz）或高速數位電路，但這些新的測試標準仍未能涵蓋系統晶片（SOC）中射頻（RF）電路的測試需求（如 2.4 GHz 藍芽技術）。其中技術的瓶頸在於週邊掃描電路對於射頻電路的負載效應過大，當週邊掃描的低頻數位電路加入射頻輸出（入）端時，此負載效應使射頻設計不易保持原本的射頻性能，若能減少此負載效應至最小，那射頻輸出（入）端即可納入週邊掃描的工作範圍。

本計畫首先對隔離射頻信號與週邊掃描負載的方法進行模擬，以便在正常射頻工作下將週邊掃描對射頻信號的負載減至最小，同時在測試模態（Test mode）下，週邊掃描仍可與其他電路匹配依照週邊掃描（IEEE 1149.1）標準正常工作，其次，CIC 的 CMOS 製程將被使用來設計 5GHz 低雜訊放大器（LNA），並在輸入端加入，隔離電路及週邊掃描電路。在設計中將比較原本的 LNA 的射頻性能，以及加入週邊掃描後對射頻性能的影響。此外，從射頻電路的設計角度來看，加上週邊掃描的負載對原本的射頻電路設計上要作何種程度的調整，以保持原本的射頻特性亦為本計畫的探討項目。而此計畫成果將在 IEEE2004 VLSI TEST 國際會議發表。

（二）計畫英文摘要。

Keywords: RF Boundary Scan, RFIC, RF-SOC, SOC Testing

This project is developing the RF boundary scan technology. Boundary scan (IEEE 1149.1) is a popular testing method for digital systems to increase the system testability and lower the testing cost. This project will extend the coverage of boundary scan from digital circuits to RF circuits (like, 5GHz WLAN). Currently, there are many new boundary scan standards (IEEE 1149.4/1149.6), which intend to extend the boundary scan coverage to analog circuits (< 1 MHz) or high speed digital circuits. Nevertheless, these new standards cannot cover the demand of RF circuit test for System-On-Chip (SOC) ICs (like 2.4 GHz Bluetooth technology). One of the boundary scan bottlenecks for RF circuits is the loading effect from Boundary Scan Cell (BSC) to RF circuits. Adding the low-frequency BSC to the input/output terminals of RF circuits will degrade the RF performance. If the loading effect can be minimized, then the RF input/output can be included into the coverage of boundary scan.

The first task in this project is to simulate the isolation between the RF signals and the BSC, which is to minimize the loading effects during the normal RF operations, and to support normal boundary scan activities during IEEE 1149.1 test mode. The second task is to utilize CIC's CMOS process to design 5 GHz low-noise amplifier (LNA) with BSC and isolation circuits at input. The performance degradation of LNA with BSC will be discussed. On the other hand, from the RF designer's point-of-view, with and without BSC loading effects, the adjustments of RF circuit design to keep the original RF performance will be studied in this project. This research result will be published in IEEE 2004 VLSI Test Symposium.

前言

邊際掃描電路大多用在接腳數非常多的數位電路內，用來確認接腳與接腳相連之間是否有斷路或是短路的現象發生，這提供了一個非常好的結構性的測試方法(structural test solution)。然而在射頻的電路中，這種結構性的測試方法也是提供了一個很好的判斷的方式，來確保射頻電路的結構部份能夠正確；尤其是在未來的射頻電路將會高度整合，接腳數目勢必會大幅增加，因此藉由邊際掃描電路的方法，與射頻電路相結合，使得整合的系統在結構上能夠確認在相連接的部分正確無誤。而此嶄新的構想已得到認同，結果將在2004IEEE VTS 中呈現。

研究目的

本計畫的目的是為了擴展週邊掃描至射頻系統晶片（RF-SOC）中的射頻（RF）電路（如 2.4 GHz 藍芽技術）。週邊掃描（IEEE 1149.1）已廣泛使用於數位系統中，可大幅提昇整個系統的可測試性，以及降低測試的成本，本計畫將擴大週邊掃描的涵蓋範圍由數位電路擴展至射頻電路（如 5 GHz WLAN），並要解決技術的瓶頸即週邊掃描電路對於射頻電路的負載效應過大，尤其是 2.4GHz 或 5GHz 電路。

文獻探討

邊際掃描電路(IEEE 1149.1 standard)是一種有關測試的設計方法,主要是測試數位電路中高密度的 IC 腳位[1]。自從 1990 初期在許多文獻中，我們可以發現邊際掃描電路在微波及射頻電路中的想法已被提出但未實現[1]-[3]。因為無線網路市場大幅增加，使得在 5GHz 的射頻電路(IEEE 802.11a)與人們的生活結合在一起。由於無線通訊產品需要小面積，因此射頻電路的工程師已經設計出許多高整合度 5GHz 的系統晶片(system-on-chip, SOC)[4]以及系統封裝設計(system-on-package, SOP)[5]的產品。5GHz 的射頻系統晶片將結合數位、類比以及射頻電路在一起。而此篇論文將使用 5GHz 的放大器[6]作為一個範例，結合邊際掃描電路與射頻電路在一起，以及測試其結合的可行性。

[1] K. Fitzgerald, "Applications '90: instrumentation," *IEEE Spectrum*, vol. 27, no. 2, pp. 37-38, February 1990.

[2] M. Jarwala, D. Le, and M.S. Heutmaker, "End-to-end test strategy for wireless systems," *Proc. IEEE Int'l Test Conf.*, pp. 940-946, October 1995.

[3] M. S. Heutmaker, and D. K. Le, "An architecture for self-test of a wireless communication system using sampled IQ modulation and boundary scan," *IEEE Communications Magazine*, vol. 37, no. 6, pp. 98-102, June 1999.

[4] M. Zargari, D.K. Su, C.P. Yue, S. Rabii, D. Weber, B.J. Kaczynski, S.S. Mehta, K. Singh, S. Mendis, B.A. Wooley, "A 5-GHz CMOS transceiver for IEEE 802.11a wireless LAN systems," *IEEE Journal of Solid-State Circuits*, vol. 37, no. 12, pp. 1688-1694, December 2002.

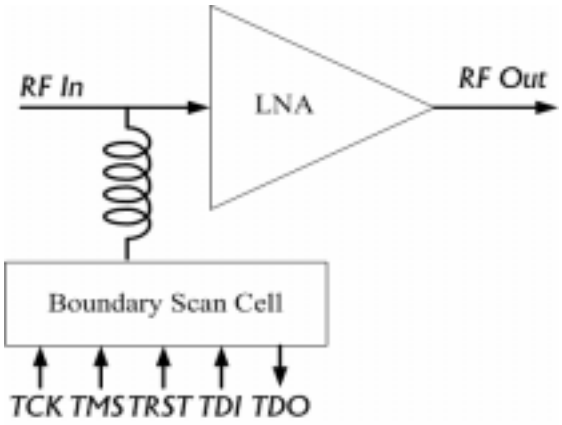
[5] K. Lim, M.F. Davis, M. Maeng, S. Pinel, L. Wan; J. Laskar, V. Sundaram, G. White, M. Swaminathan, and R. Tunimala, "Intelligent network communicator: highly integrated system-on-package (SOP) testbed for RF/digital/opto applications," *Proc. IEEE Electronic Components and Technology Conf.*, pp. 1594-1598, May 2003.

[6] R.C. Liu, C.R. Lee, H. Wang, and C.K. Wang, "A 5.8-GHz two-stage high-linearity low-voltage low noise amplifier in a 0.35-μm CMOS technology," *IEEE Radio Frequency Integrated Circuits (RFIC) Symp. Dig.*, pp. 221-224, June 2002.

研究方法

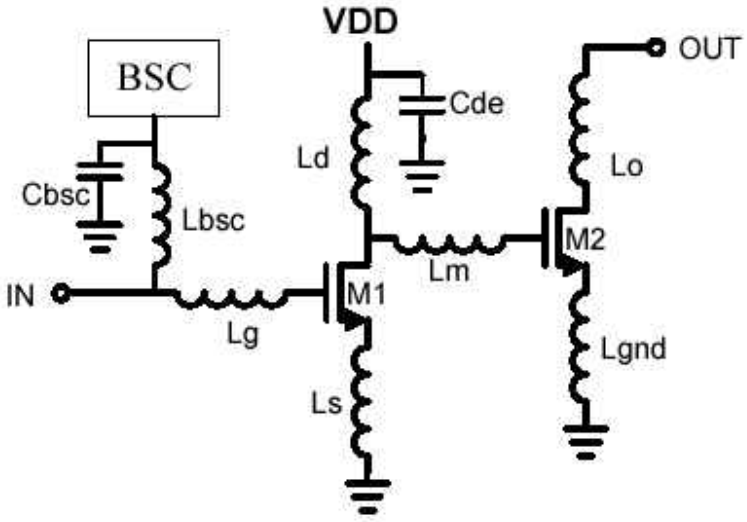
由於射頻電路的性能容易受寄生電路元件的影響，因此要在原本射頻電路的設計中，再加上一個邊際掃描電路並非直接接上即可，必須要使用適當的隔離電路，使得加上邊際掃描電路之後並不會造成射頻電路的效果變差，如此才是我們想要的結果。有了這個方向之後，我們得到了以下的構想：

本電路之電路架構如下圖所示，主要可分為兩個部分，其中一部份為 RF 電路的 LNA，另一部份為數位的邊際掃瞄測試電路。而 LNA 和邊際掃瞄測試電路使用一個電感作為分離，因電感在 5 GHz 對 RF 而言是斷路，不能通過；但對約數十 MHz 的數位訊號而言卻只是一小段線而已，可以通過，故用此方法可以達到隔離數位和 RF 訊號的效果。



圖一. LNA、數位掃描訊號與其阻隔電路的關係

- 5GHz 的 LNA 電路設計部份：



圖二. 5.8GHz 的 LNA 的電路圖

這是兩級 common-source amplifier 串接的架構。前級之 gate inductor 和 source inductor 是為了做 input matching，把我們的 input resistance matching 到 50 Ω，而 drain inductor 是當做 load 來提升在高頻時之 gain，以及調整放大器增益之中心頻率。後級之 gate inductor 及 source inductor 是為了做 inter-stage 的 matching 以及電路的穩定。後級之 inductor 是為了做 output matching ，把 output impedance matching 到 50 Ω。其餘的 inductor 及 capacitor 是為了在 simulation 時考慮寄生效應所加。

低雜訊放大器的輸入級，由一階小訊號模型的簡易分析,我們可求得輸入阻抗為

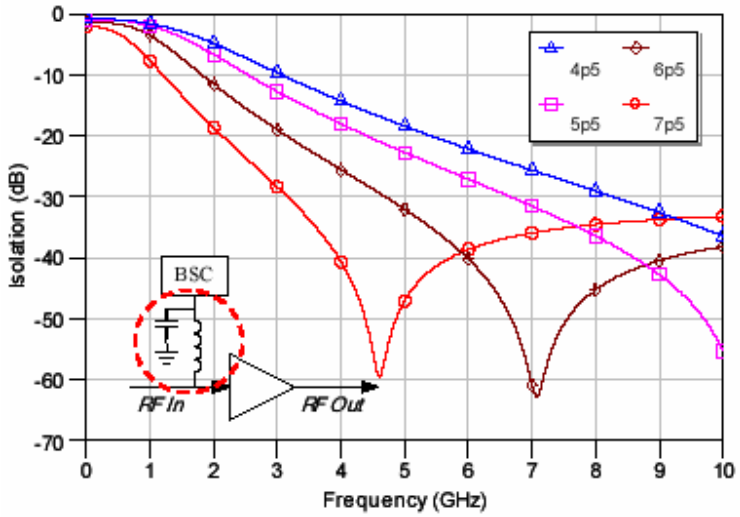
$$Zin = s(Ls + Lg) + \frac{1}{sCgs} + (\frac{gm_1}{Cgs})Ls$$
$$\approx w_T Ls \qquad (at \ \ resonance)$$

在 LC 共振時(w_T 為共振頻率)，我們可藉由調整 Ls 來造成一 50 Ω 的輸入阻。抗利用這個架構我們可以在不犧牲 Noise Figure 的前提下仍然能夠在共振頻率下產生一個 50 Ω 的輸入阻抗，再經由一些調整與 Hspice 的模擬，便是我們所提出的低雜訊放大器。

- 隔絕邊際掃描電路與射頻電路的方法

在射頻電路加上邊際掃描電路的最主要的考量是：要如何選取隔絕的方式，以至加上邊際掃電路後並不會影響到射頻電路的表現。而最直觀的想法就是加上一個夠大的電感，類似 RF chock 的功用。因為電感可以讓數位掃描的訊號通過(因為頻率較低)，而用來隔絕射頻的訊號；此外在加上電感之外還可以再加上一個足夠大電容(Cbsc)接到地，使得射頻訊號可以走電容這一路到地，在 RF chock 之外再度確保射頻訊號不會進入數位掃描電路中。

一般說來，數位掃描訊號的輸入阻抗非常的大，大約是接近數 kΩ 的等級；在此考慮邊際掃描電路的輸入阻抗為 50Ω 下(也就是遠比實際情形差的考量)，各個不同的電感值對頻率的 isolation，如下圖所示：



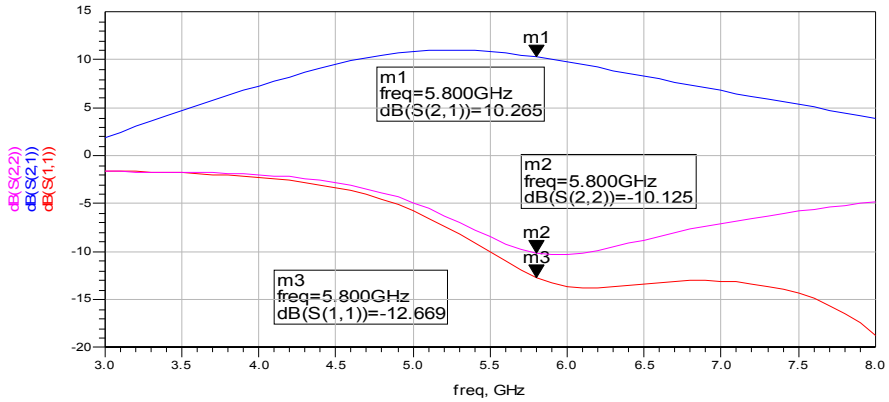
圖三.利用不同的 LC 值，對於射頻訊號與數位掃描訊號隔離度的比較
(假設邊際掃描電路的阻抗為 50Ω，這是考量很差的情況之下)

最後,我們選用 23.59nH 的電感以及 7.5pF 的電容，作為主要隔絕兩個電路的方式。

結果與討論

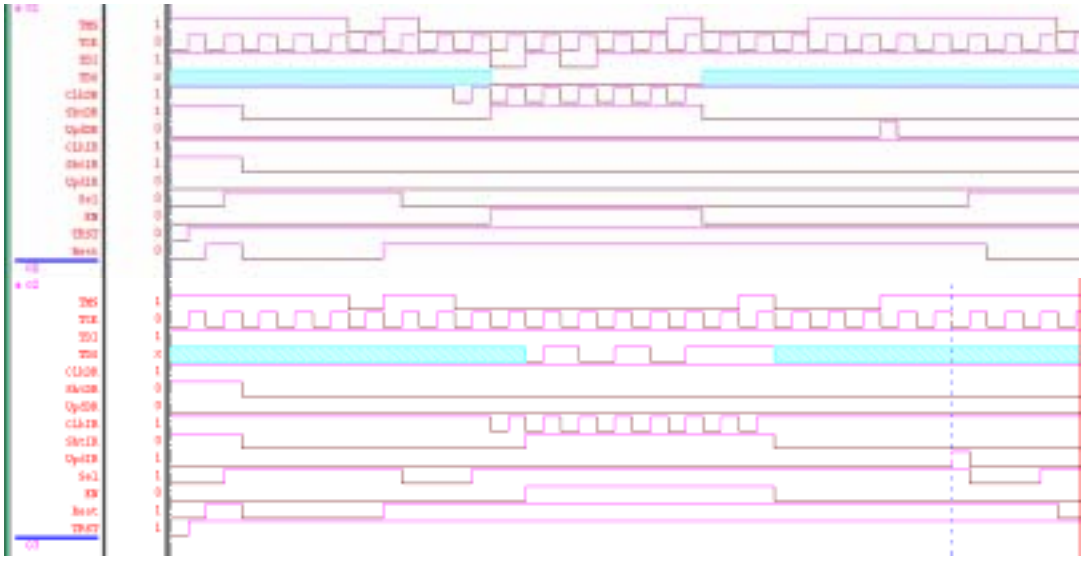
1. LNA:

模擬結果顯示，這個低雜訊放大器中之操作頻率為 5.8 GHz，總電流為 15 mA， supply voltage 為 1.3 V，功率損耗 20 mW， 圖四為其模擬成果，S_{21} 為 10.3 dB，S_{11} 為 –12.7 dB，S_{22} 為 –10.1 dB。



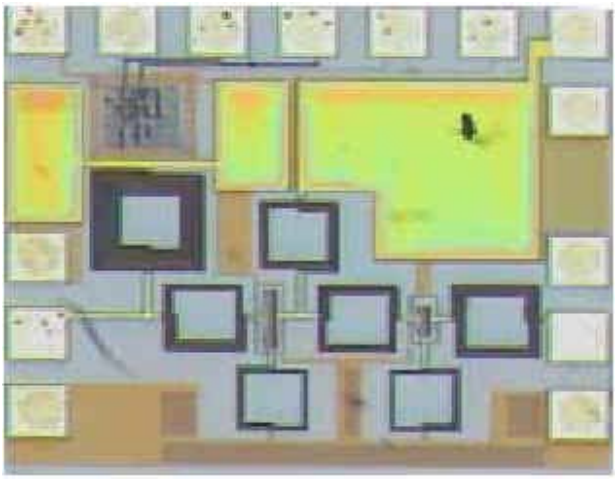
圖四. LNA 的模擬結果

2. 邊際掃描測試方面：



圖五.邊際掃描測試訊號

3. 晶片照片：



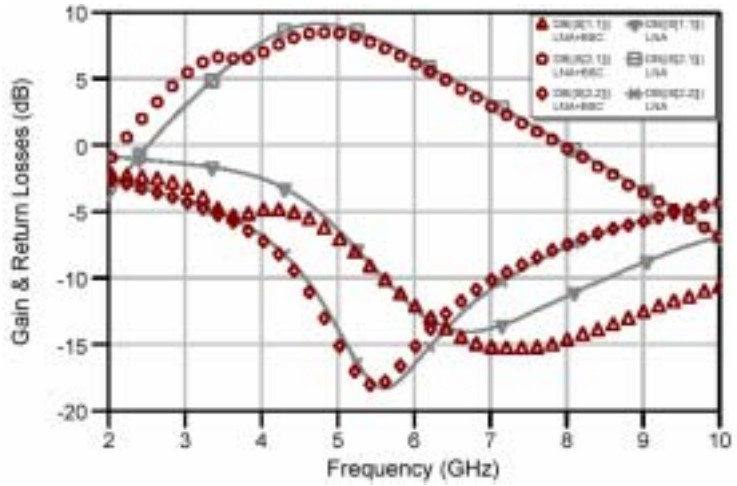
圖六. 晶片照片

4. 實際量測結果：

實際量測結果我們可以清楚的發現：經由適當的電感與電容的選取，的確成功地隔絕射頻與數位訊號，使得射頻的表現幾乎不變，因此利用 LC Isolation Network 的確可達到我們的要求。

表一.加上數位掃描電路後的放大器與沒加上的比較

	Amplifier	Amplifier + BSC
Freq.	5.8 GHz	5.8 GHz
Gain	7.2 dB	6.8 dB
Input Return Loss	11 dB	11 dB
Output Return Loss	17 dB	16.7 dB



圖七.加上數位掃描電路與否對 LNA 的 5GHz 特性影響不大

這篇論文主要是展現利用 0.35μm 製程，結合了 5GHz 的放大器與邊際掃描電路。而此放大器利用了 LC 的隔絕電路，隔絕射頻訊號進入邊際掃描電路，來連結射頻電路與邊際掃描電路在一起。而這種架構克服了一些寄生的負載效應的問題，而且對於最原本的射頻電路作了最少的改變。最後，利用 LC 隔絕電路結合 5GHz 的放大器與標際掃描電路的方法，只造成了放大器大約 0.4dB 的增益衰減，證明此為可行的方法。而此計畫成果將在 IEEE2004 VLSI TEST 國際會議發表。

附件一、IEEE 2004 VTS Paper

（見下頁）

Boundary Scan for 5GHz RF Pins Using LC Isolation Networks

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***Abstract* — The boundary-scan test provides a structural test solution for the densely packed digital electronics. For RF devices, the structural test also provides a good diagnostic resolution to the structural defects of RF circuits, especially for the high pin-count RF-SOCs. This paper tries to implement the boundary-scan test on a 5GHz RF pin using LC isolation networks to connect the RF lines and the boundary-scan cell, which will isolate the RF circuitry from the digital boundary scan cell. This topology overcomes the parasitic loading problems and provides a minimum RF performance degradation to the 5GHz RFIC. The measurement results show only 0.4 dB gain degradation in the 5GHz amplifier with a boundary-scan cell and LC isolation networks**

I. INTRODUCTION

The boundary scan, IEEE standard 1149.1, is a design-for-testability standard to provide a test solution for the densely packed digital electronics [1]. Since the early 1990s, the extension of boundary-scan standard to cover microwave/RF devices has been discussed in many different publications [1-3]. In [2] and [3], the boundary-scan compliant digital signal processors (DSPs) in the baseband processor provide the means for the system controller to activate the RF sub-systems' functional test [2], or to activate the RF self-test [3]. The boundary-scan standard provides only an indirect testability to the RF devices in [2] and [3], which limits the resolution of RF diagnostics. This paper tried to combine the boundary-scan test directly with RF devices, so the resolution of RF diagnostics can be significantly increased.

The significant growth in the wireless LAN market introduces 5GHz RF systems (IEEE 802.11a) into people's daily life. Due to the size reduction trend in wireless products, the RF designers have developed many highly integrated 5GHz sytem-on-chip (SOC) [4], and system-on-package (SOP) [5] products. The test requirements of these 5GHz RF-SOCs will include digital, analog, and RF tests all together. This paper will use a 5GHz amplifier [6] as an example to combine the boundary scan test with the 5GHz RF pin and demonstrate the feasibility of boundary scan for RF and analog pins.

There are many difficulties to perform boundary-scan tests on RF pins. The main reason is that adding additional test circuitry to the parasitic sensitive RF lines is not trivial and can easily degrade the RF performance of the RFIC [7], [8]. This paper will use a RF LC isolation network (RF choke + shunt capacitor) to connect the RF lines and boundary-scan cell, which will overcome the previous parasitic loading problems and provide a minimum RF performance degradation to the RFIC.

The purpose of adding boundary-scan capabilities to the RF pins is to provide a fast structural test for the RF pins in an early manufacturing test stage. This test can be implemented within the standard digital boundary scan test, and without any additional test procedures or expansive RF test equipment. If the boundary scan structural test is important to the high-speed digital circuits, then the structural test is also very important to the RF circuits. Most RF tests are placed within the functional tests or the parametric tests, which provide accurate RF performance tests, but have limited the resolution for RF diagnostics. The boundary scan test for RF pins is like a complementary test to the RF functional test, which provides good diagnostic resolution to the structural defects of RF circuits.

The cost sensitive nature of consumer RF-SOC requires a cost reduction as the SOC complexity increases. The module final test is a key contributor to the manufacturing cost for a packaged RFIC device [9]. Using boundary scan in RF pins can significantly increase the test coverage of RF circuits, and also improve the yield of the final functional test. The *test earlier* strategy [10] is consistent with the boundary scan on RF pins strategy, which can improve the final product yield and reduce production cost. Another concern with the RF boundary scan is that, adding additional test pins could significantly increase the die size or package size, which is not cost effective for most low-cost RFICs. Nevertheless, for the high pin-count RF-SOCs, like the 64-pin 5GHz WLAN SOC [4], adding boundary scan pins will increase the total pin-count for less than 10%. In the future, many RF-SOCs will have more digital circuits inside, and the boundary scan pins can be used for both digital and RF boundary scan.

II. LC Isolation Networks

To overcome the parasitic loading problems and to minimize RF performance degradation to the 5GHz RFIC, an isolation network is required between the RF lines and the boundary scan cell (BSC). The most common isolation network in the microwave frequency is the RF choke, which is a large inductor. This inductor allows the boundary-scan low-frequency signal to pass, but blocks or isolates the RF signal from the BSC. Hence, for the 5GHz in-band applications, no parasitics from BSC can affect the in-band RF performance. All the parasitics from BSC are isolated from the RF lines due to the LC isolation networks.

The LC isolation networks are implemented with a CMOS 0.35µm process. The spiral inductor with some parasitic capacitors and resistors needs an additional shunt capacitor to provide a better isolation. The RF isolation between the RF lines and the BSC is shown in Fig. 1. This simulation is based on 50Ω input/output port impedance. For a real BSC cell using 0.35µm CMOS, the port impedance will be much larger than a kΩ. For larger BSC port impedance, the isolation will be higher than the isolation of 50 Ω port impedance. Hence the plot in Fig. 1 is the worst case isolation. For 5GHz applications, the LC isolation networks consist of a 23.59nH inductor and a 7.5pF capacitor as the major parameters for the network.

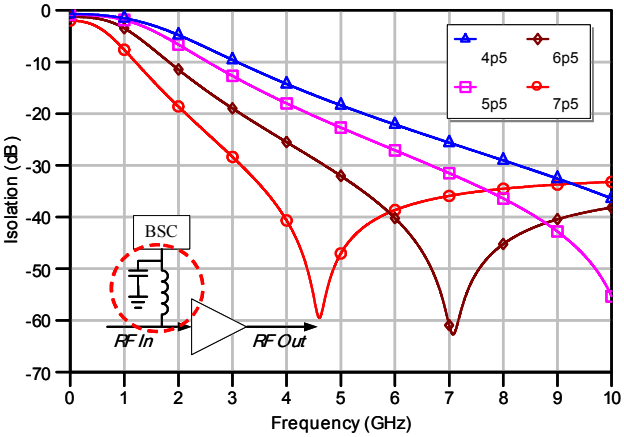


Fig. 1. The RF isolation between RF lines and boundary-scan cell (BSC) for different LC values. (assuming 50Ω input/output port impedance for the worst-case isolation study)

III. 5GHz Amplifier Design

A 5GHz amplifier [6] is used to demonstrate the feasibility of adding boundary-scan cell to 5GHz RF pins. This 0.35µm CMOS amplifier has two gain stages. Inductors are used as 5GHz input/output matching networks. The LC networks are selected as a DC bias network, which allows only DC supply to pass the bias network. This bias network has a similar topology as our LC isolation networks, which provides a similar function to pass low-frequency boundary-scan signals only. Both networks block/isolate any RF noise from outside, and also keep the RF signal with no leakage to the outside.

The BSC cell design in the previous section can be used as a drop-in cell to the boundary-scan compliant amplifier design, as shown in Fig. 2. If the amplifier frequency has significantly changed, then we need a different LC isolation network to cover a different frequency band.

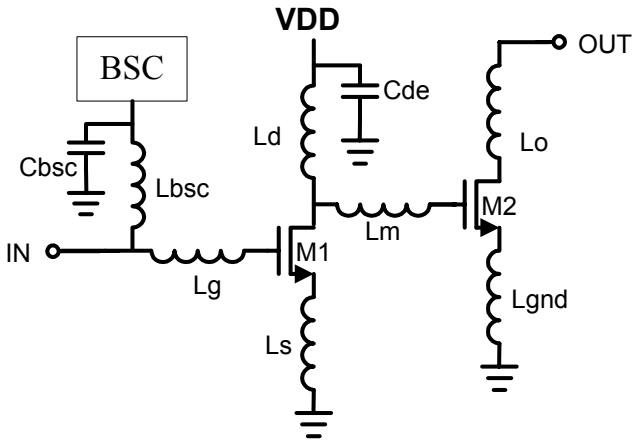


Fig. 2. Schematic of the boundary-scan compliant 5GHz amplifier design.

IV. Digital Measurement

Fig. 3 illustrates the chip-photo of the boundary-scan compliant 5GHz amplifier. The physical size of this CMOS 0.35µm 5GHz amplifier is 1.5 X 1.5 mm^2.

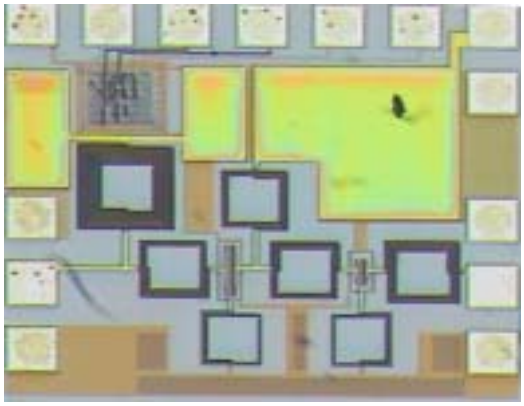
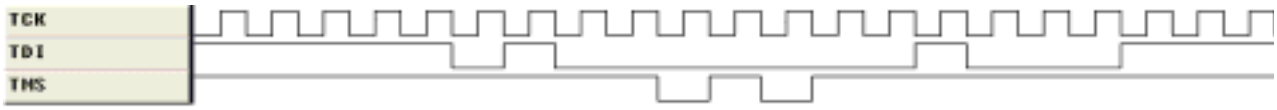
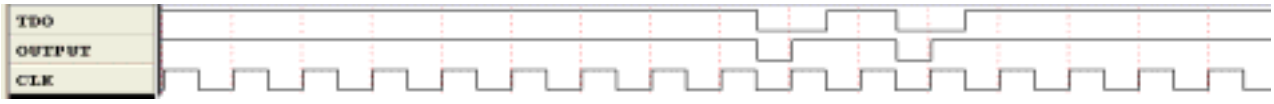


Fig. 3. Chip photo of the boundary-scan compliant 5GHz amplifier design.



(a)



(b)

Fig. 4. (a) Digital input pattern, clock rate is 50 kHz, (b) Digital output pattern, TDO : Digital output pattern OUTPUT : BSC output pattern at RF pin when the amplifier is off and circuit is in test mode.

The 5GHz boundary-scan compliant amplifier has two operation modes:

1) Test mode. The whole circuit in boundary scan test mode is for structural test only. During the test mode, the RF portion of the amplifier is off, and the BSC digital circuit block is powered on for receiving digital patterns and passing on patterns to next devices.
2) RF mode. The BSC digital circuit clock is powered off and no digital pattern is on the RF lines. The RF portion is powered on and the amplifier operates in its normal RF operational region. The LC isolation circuits will make the BSC 'invisible' (-40dB isolation) to the 5GHz in-band signal.

Fig. 4 shows the input digital pattern at TDI, TCK, and TMS, and also the digital output pattern at TDO, and the RF pin. The TDO signal has a similar output at the RF pin. This BSC test mode clock rate is 50 kHz.

V. RF Measurement

The RF performance of the boundary-scan compliant 5GHz amplifier is measured and compared with the original 5GHz amplifier without BSC, shown in Table I. The frequency is centered in the same 5.8 GHz. The gain has only 0.4dB degradation, which is close to the process variation range. These two amplifiers are processed in different wafer lots. The return loss has a similar performance.

Fig. 5 demonstrates the s-parameter performances of these two amplifiers, which have almost identical responses between 5 to 6.5 GHz numbers, and the date. At 5.8 GHz, the gain is not the highest peak, but it is the WLAN operation frequency with a low noise figure.

Table I. RF performance comparison between the original 5GHz amplifier and the boundary-scan compliant 5GHz amplifier

	Amplifier	Amplifier + BSC
Freq.	5.8 GHz	5.8 GHz
Gain	7.2 dB	6.8 dB
Input Return Loss	11 dB	11 dB
Output Return Loss	17 dB	16.7 dB

VI. Conclusion

This paper demonstrates a boundary-scan compliant 5GHz amplifier with 0.35μm CMOS technology. This amplifier implements the boundary-scan test on a 5GHz RF pin using LC isolation networks to connect the RF lines and boundary-scan cell, which will isolate the RF circuitry from the digital boundary scan cell. This topology overcomes the parasitic loading problems and with minimum modification to the original circuits. The measurement results show only 0.4 dB gain degradation in the 5GHz amplifier with a boundary-scan cell and LC isolation networks.

ACKNOWLEDGEMENT

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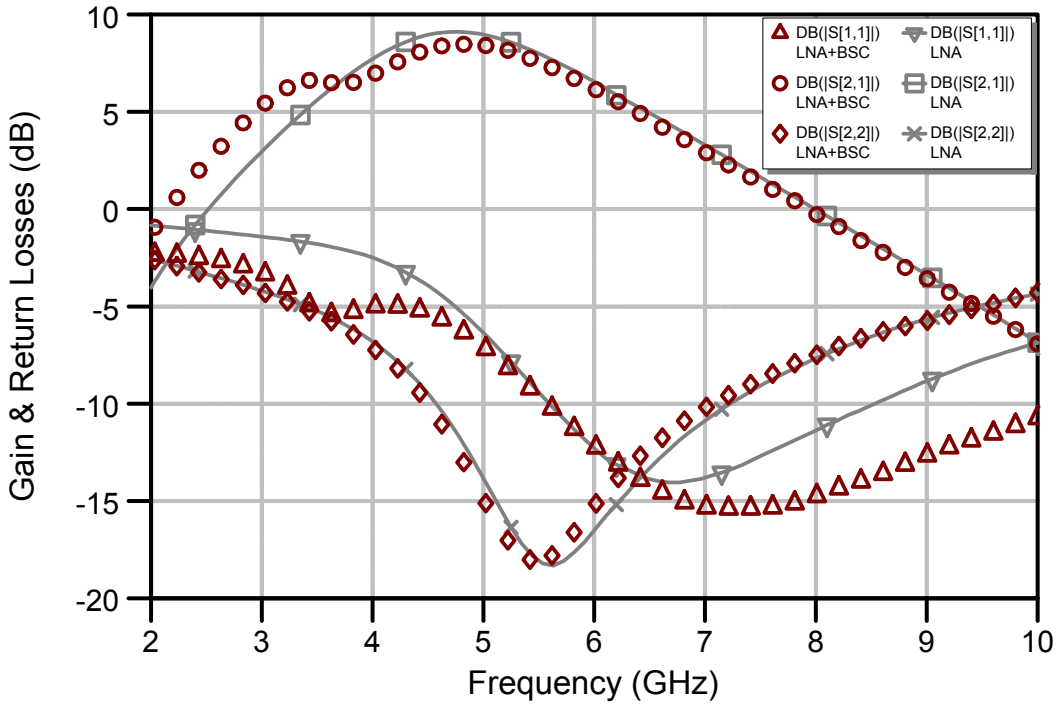

Fig. 5. RF measurements of the 5GHz amplifier (LNA) with and without boundary-scan cell (BSC) and LC isolation networks.