Threading Dislocation Induced Low Frequency Noise in Strained-Si nMOSFETs

W.-C. Hua, M. H. Lee, P. S. Chen, M.-J. Tsai, and C. W. Liu, *Senior Member, IEEE*

***Abstract*—The correlations between the threading dislocations and the low-frequency noise characteristics of the n-type strained-Si field-effect transistors are studied using the devices with different sizes. The device-area-dependent $S_{\rm VG}$ (power spectral density of the gate referred voltage noise) ratio of the strained-Si devices over the control Si devices obtained form geometric average can be understood by the modified carrier number fluctuation model with excess traps from the Poisson distributed threading dislocations. The equivalent trap number per threading dislocation extracted from the area-dependent $S_{\rm VG}$ ratios is ∼85 for the strained-Si devices, and which results in ∼4.2X degradation of the $S_{\rm VG}$ for the strained-Si device with the device area of 625 μm^2.**

***Index Terms*—Flicker noise, MOSFET, strained-Si, threading dislocation.**

I. Introduction

DUE to its enhanced current drive and high-frequency performances [1]–[3], the strained-Si technology is undoubtedly one of the enabling technologies for RF circuit applications. Although the enhanced cutoff frequency of the strained-Si MOSFET [3] can facilitate the RF CMOS circuit design, the unintentionally induced threading dislocations in the strained-Si channel can potentially degrade some RF circuits. Although the threading dislocations in the strained-Si channel may lead to different electrical properties, few literatures are reported regarding this issue. In this letter, the flicker noise characteristics for both the strained-Si and the control Si devices with different sizes are investigated to clarify the correlations between the threading dislocations and the flicker noise characteristics.

II. Device Fabrication

Fig. 1 shows the schematic diagrams of the device structures of the strained-Si nMOSFETs with and without threading dislocations in the channel. The 20-nm strained-Si channel is grown epitaxially on the relaxed 1-μm $Si_{0.8}Ge_{0.2}$ layer and the 1-μm graded $Si_{1-x}Ge_x$ buffer from $x = 0$ to 0.2 by ultrahigh-vacuum chemical vapor deposition. The tensile strain in the channel is ∼0.64%, measured by the surface Raman spectroscopy [4] and increases to 0.7% after the device process. Low-temperature (700 °C) deposited tetraethylorthosilicate gate oxide (30 nm) is used to avoid the high-temperature thermal oxidation-enhanced Ge outdiffusion [5]. The effect of the Ge outdiffusion on the flicker noise is negligible. The output characteristics of the strained-Si devices ($L = 25$ μm) show ∼78% and ∼35% enhancements of $I_{\rm DS}$ at constant overdrive ($V_{\rm GS} - V_T$) at the linear and the saturation region, respectively. The effective mobility of the strained-Si device is extracted from the drain current and the split capacitance–voltage [6] measurements on the large-area devices ($W \times L = 25 \times 25$ μm), and has a 65% enhancement at the effective normal field of 1.0 MV/cm [3].

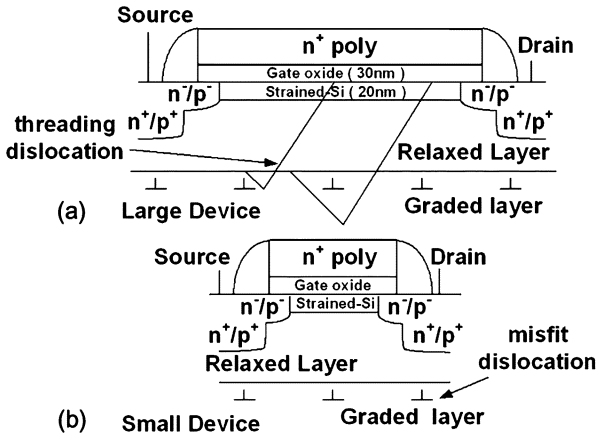

Fig. 1. Schematic diagrams of the strained-Si device structures. (a) A large-area device with threading dislocation in the channel. (b) A small-area device with the dislocation-free channel.

III. Results and Discussion

Fig. 2 shows the surface morphology of the strained-Si film after defect-etching [7]. The density of threading dislocations of the strained-Si film is $\sim 10^{-2}$ μm^{-2}. The existence of the threading dislocations in the strained-Si channel is also confirmed by the transmission electron microscopy on the large-area device. Fig. 3(a) and (b) shows the statistical $S_{\rm VG}$ of the strained-Si and the control Si devices at 30 Hz with $L = 0.8$ μm for different gate width, and $W = 25$ μm for different gate lengths. All the devices are biased at $V_{\rm DS} = 0.5$V with constant gate overdrive ($V_{\rm GS} - V_T = 0.3$V) at the saturation region. The statistical results are obtained from the geometric average of the measured $S_{\rm VG}$ for ten to 20 devices. The geometric average

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W.-C. Hua is with the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, R.O.C.

M. H. Lee, P. S. Chen, and M.-J. Tsai are with the Electronics Research & Service Organization, Industrial Technology Research Institute (ERSO/ITRI), Hsinchu 300, Taiwan, R.O.C.

C. W. Liu is with the Department of Electrical Engineering and Graduate Institute of Electronics Engineering, National Taiwan University, Taipei, Taiwan, R.O.C, and also with the Electronics Research and Service Organization, Industrial Technology Research Institute (ERSO/ITRI), Hsinchu 300, Taiwan, R.O.C. (e-mail: chee@cc.ee.ntu.edu.tw).

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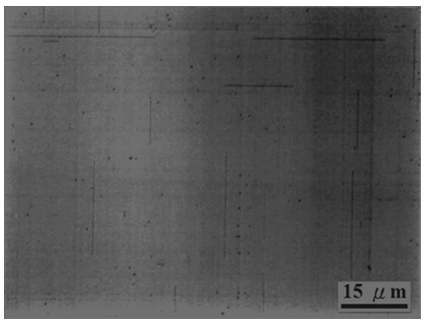

Fig. 2. Surface morphology of the strained-Si channel layer after defect-etching. The black points are the threading dislocations and the density of threading dislocations is $\sim 10^6$ cm^{-2} (10^{-2} μm^{-2}).

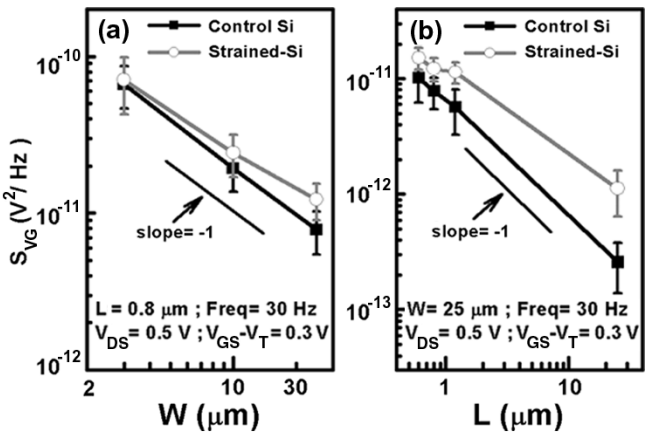

Fig. 3. Statistical result of $S_{\rm VG}$ of the strained-Si and the control Si devices at 30 Hz. The error bars stand for the geometric standard deviations of the $S_{\rm VG}$ (obtained from the arithmetic standard deviation of the $\log(S_{\rm VG})$): (a) $L = 0.8$ μm for various gate widths (b) $W = 25$ μm for various gate lengths.

method shows lower error [8] and can fit the distribution of large number of noise measurements more precisely than the arithmetic average [9]. In Fig. 3(a), the $S_{\rm VG}$ of both the strained-Si and the control Si devices are approximately inversely proportional to the channel width and are consistent with the carrier number fluctuation model [10]–[13] of the nMOSFET biased at saturation, which is given by

$$S_{\rm VG} \cong \frac{q^2 N_{\rm ot}}{C_{\rm ox}^2 WL}\frac{1}{f} \tag{1}$$

where q is the electron charge, $N_{\rm ot}$ is the equivalent oxide trap per unit area and is assumed to be independent of gate bias, C_{ox} is the oxide capacitance per unit area, W is the gate width, L is the gate length, and f is the frequency. The validity of the carrier number fluctuation model is confirmed by extracting the N_{ot} ($\sim 2.3\times10^7$ to 2.7×10^7cm^{-2}) at various gate bias in the saturation region ($V_{\rm GS}-V_T = 0.1$ to 0.5 V, $V_{\rm DS} = 0.5$V) for the control Si devices. The $N_{\rm ot}$ is nearly independent of gate bias at saturation region for the nMOSFETs [12], [13]. Although all the device areas in Fig. 3(a) are smaller than 100 μm^2, there are still some chances to have dislocations in the strained-Si channels. Thus, the $S_{\rm VG}$ of the strained-Si devices are slightly higher than the control Si devices in Fig. 3(a). In Fig. 3(b), the statistical $S_{\rm VG}$ of the control Si devices are inversely proportional to the channel length, but the $S_{\rm VG}$ of the strained-Si devices

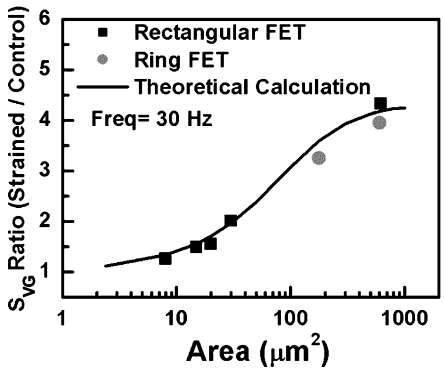

Fig. 4. Measured and calculated $S_{\rm VG}$ ratio of the strained-Si devices over the control Si devices for various device sizes. The calculation of the $S_{\rm VG}$ ratio is based on the Poisson distributed threading dislocations.

shows an increasing degradation as compared to the control Si devices as the channel length increases. The threading dislocations in the channel may act as the trap centers, which play the similar role as the Si/oxide interface trap and increase the $S_{\rm VG}$ of the strained-Si devices. The effect of the dislocations on the $S_{\rm VG}$ can be quantitatively characterized by the Poisson distributed threading dislocations. The probability density function $[p(n, A)]$ of having n dislocations in an area of A (μm^2) for the strained-Si device is given by

$$p(n, A) = \frac{e^{-\mu(A)}\mu(A)^n}{n!}, \quad n = 0, 1, 2\ldots \tag{2}$$

where $\mu(A)$ is the average number of the dislocations in an area of A (μm^2). From the defect etching experiment, $\mu(A)$ is given by $(A/100)$. The equivalent total trap number per unit area $(N_{\rm ot,S-Si}(n))$ for the strained-Si device with n dislocations in the channel is given by

$$N_{\rm ot,S-Si}(n) = N_{\rm ot} + \frac{nN_{\rm TD}}{A} = N_{\rm ot}\left(1 + \frac{nN_{\rm TD}}{AN_{\rm ot}}\right) \tag{3}$$

where $N_{\rm TD}$ is the equivalent trap number per dislocation. The geometric average of the $S_{\rm VG}$ of the strained-Si device $(S_{\rm VG,S-Si}(A))$ with device area of A (μm^2) is given by

$$S_{\rm VG,S-Si}(A) = S_{\rm VG,C-Si}(A)\left[\prod_{n=0}^{\infty}\left(1 + \frac{nN_{\rm TD}}{AN_{\rm ot}}\right)^{p(n,A)}\right] \tag{4}$$

where $S_{\rm VG,C-Si}(A)$ is the $S_{\rm VG}$ of the control Si device with the device area of A (μm^2). Fig. 4 shows the measured and the calculated $S_{\rm VG}$ ratios of the strained-Si devices over the control Si devices with different sizes for both rectangular and ring FETs. The calculated $S_{\rm VG}$ ratios are area-dependent since $p(n, A)$ presents in the power term in (4). Only the first 20 terms in (4) are significant in the practical calculation of $S_{\rm VG}$ ratios in Fig. 4. Significant $S_{\rm VG}$ degradation of the strained-Si devices as compared with the control Si devices are found for the device area larger than 100 μm^2. The $N_{\rm TD}$ is $\sim$85 extracted by fitting the $S_{\rm VG}$ ratios in Fig. 4 using (4). The equivalent total trap number per unit area $(N_{\rm ot,S-Si})$ for the strained-Si can be obtained by multiplying the $N_{\rm ot}$ (2.5×10^7cm^{-2}) of the control Si device by the $S_{\rm VG}$ ratios in Fig. 4. According to the proposed model, the calculated $S_{\rm VG}$ ratio has a saturation value

of 4.5 when the device area is very large, and which is very close to the S_{VG} ratio derived from the conventional approach $(1 + ((85/(100\,\mu\mathrm{m}^2))/(2.5 \times 10^7 \mathrm{cm}^{-2}))) = 4.4)$.

IV. Conclusion

The excess flicker noise induced by the threading dislocation shows a device-area-dependent behavior and which is different as compared to the behavior of the S_{VG} in unstrained Si nMOSFETs. This phenomenon can be quantitatively characterized by the Poisson distributed threading dislocations with geometric average of the measured S_{VG}. In order to take advantage of the enhanced performance of the strained-Si MOSFET and maintain the flicker noise performance, the devices with lower density of threading dislocations in the channel is required.

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