rail. *TG2* belongs to different control loops depending on input signal *C*. If $C = 0$ the control loop is created by *TG2* and *TG3*. As the transmission gate receives $C = 0$, it is open and the control loop is in a floating state. Otherwise, if $C = 1$, *TG2* belongs to the control loop created by *TG1* and *TG2*. In this case the module driving *TG1* is disconnected, so the control loop is then also in a floating state. Thus, for both values of input signal *C*, the bridged node belongs to a control loop in a floating state, it may be a state modifying bridge and the sizing of the transistors has to be considered. In the example, the sizing of transistors makes the faulty circuit I_{DDQ} undetectable. Similar analyses are carried out for the remainder of the state modifying bridges and they have been detected by a voltage-based test methodology.

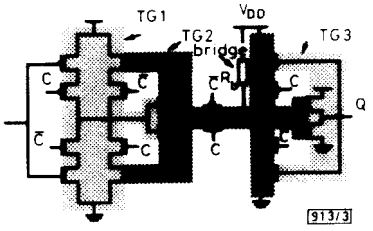

Fig. 3 *Example of a realistic state modifying bridge in the scan-path FF*

In the example, for R_b greater than 2kΩ, the bridges do not have any state modifying behaviour and, consequently, are I_{DDQ} testable.

Conclusions: In sequential CMOS circuits control loops may be used to implement memories. These structures may introduce an undesired evolution of their signals if bridging defects are present. It has been shown that irredundancy is not a sufficient condition for current detectability of these CMOS sequential defective circuits affected by bridges. However, every time a control loop is not current testable, an erroneous logic value and a voltage logic test may be applied. A simple example of a scan-path FF has been studied and 8.1% of realistic bridges (shorts, $R_b = 0$) has been found to modify the memorised state. For bridge resistance greater than 2Ω, all bridges were I_{DDQ} detectable.

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References

1 LEVI, M.W.: 'CMOS is most testable'. Int. Test Conf., 1981, pp. 217–220

2 SODEN, J.M., HAWKINS, C.F., GULATI, R.K., and MAO, W.: 'I_{DDQ} testing: A review', *J. Electron. Testing: Theory and Applications*, December 1992, **3**, (4), pp. 291–303

3 SHEN, J.P., MALY, W., and FERGUSON, F.J.: 'Inductive fault analysis of MOS integrated circuits', *IEEE Design and Test*, December 1985, pp. 13–26

4 NIGH, P., and MALY, W.: 'Test generation for current testing', *IEEE Design and Test of Computers*, 1990, pp. 26–38

5 MILLMAN, S.D., and MCCLUSKEY, E.J.: 'Detecting bridging faults with stuck-at test sets'. Int. Test Conf., 1988, pp. 773–783

6 LEE, K.J., and BREUER, M.A.: 'Design and test rules for CMOS circuits to facilitate I_{DDQ} testing of bridging faults', *IEEE Trans.*, May 1992, **CAD-11**, (5), pp. 659–670

Low-voltage BiCMOS dynamic minimum circuit using a parallel comparison algorithm for fuzzy controllers

J.B. Kuo, J.Y. Wang and Y.G. Chen

Indexing terms: Fuzzy control, BiCMOS integrated circuits

The Letter presents a low-voltage BiCMOS dynamic minimum circuit using a parallel comparison algorithm for VLSI implementation of fuzzy controllers. Using low-voltage BiCMOS dynamic circuits [1] and a parallel comparison algorithm, a four-4-bit-input minimum circuit designed, based on a 1μm BiCMOS technology, shows a 9.5ns comparison time, which is a ×2.5 improvement in speed as compared to that based on CMOS technology.

Introduction: Fuzzy controllers that mimic human behaviour have been successfully applied to replace traditional control systems. In a fuzzy controller, the most important part is the inference engine, which is mainly composed of minimum/maximum circuits. Minimum/maximum circuits using various CMOS circuits have been reported [2, 3]. Recently, BiCMOS technology is becoming a major tool for building VLSI systems owing to its superior advantages in speed performance. A minmium circuit [4] using a BiCMOS dynamic circuit [5] and a parallel comparison algorithm for fuzzy controllers was reported. For advanced BiCMOS technologies, scaling power supplies is unavoidable [6]. For a deep sub-half-micrometre BiCMOS technology, a 1.5V supply is necessary. With a 1.5V supply, the BiCMOS dynamic circuit introduced before cannot be used. In this Letter, using low-voltage BiCMOS dynamic digital circuits [1], a low-voltage BiCMOS dynamic minimum circuit suitable for realising large-scale fuzzy controllers is described.

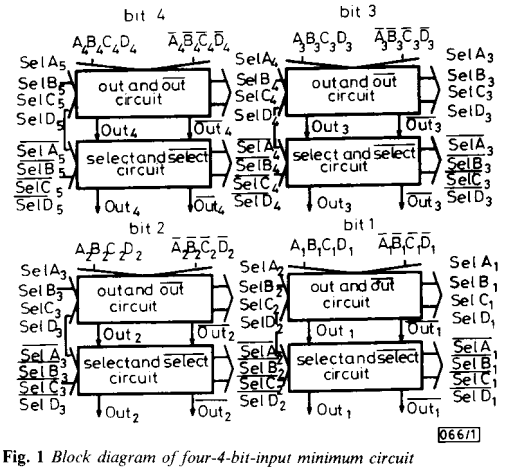

Fig. 1 *Block diagram of four-4-bit-input minimum circuit*

Circuit: Fig. 1 shows the block diagram of the four-4-bit-input minimum circuit using low-voltage BiCMOS dynamic circuits and a parallel comparison algorithm. For selecting the minimum of four 4-bit inputs ($I_{i4}I_{i3}I_{i2}I_{i1}$, $i = 1,4$), instead of comparing two at a time, four inputs are compared at the same time from MSB ($j = 4$) to LSB ($j = 1$) using the the parallel comparison algorithm:

$$\overline{Out_j} = \bigcup_{i=1}^{4}(\overline{I_{i,j}} \wedge \overline{Sel_{i,j+1}}) \qquad j = 4,1 \qquad (1)$$

$$Sel_{i,j} = Sel_{i,j+1} \vee (I_{i,j} \wedge \overline{Out_j}) \qquad i = 1,4 \quad j = 4,1 \quad (2)$$

$$Sel_{i,5} = 1 \qquad i = 1,4 \qquad (3)$$

where $I_{i,j}$ is the jth bit of the ith input. Each cell contains *Select*/$\overline{Select}$ and *Out*/$\overline{Out}$ circuits to realise eqns. 1 and 2. As shown in Fig. 2*a*, during the precharge period, the outputs of both the *Select* and the $\overline{Select}$ circuits are precharged to high. After the precharge period, the outputs may be pulled down and stay high

according to the specific input logic states. As shown in Fig. 2*b*, the *Out*/$\overline{Out}$ circuits have a similar configuration.

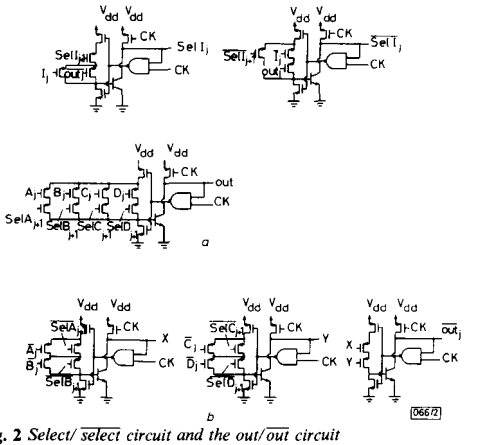

Fig. 2 *Select*/$\overline{select}$ *circuit and the out*/$\overline{out}$ *circuit*

a Select/$\overline{select}$ circuit
b Out/$\overline{out}$ circuit

As in a pipelined system, cascading dynamic logic gates may have serious race problems. In the minimum circuit using the low-voltage BiCMOS dynamic logic circuit, no race problems exist because the operation of the Bi*p*MOS pulldown structure is a 'buffer' instead of an 'inverter'.

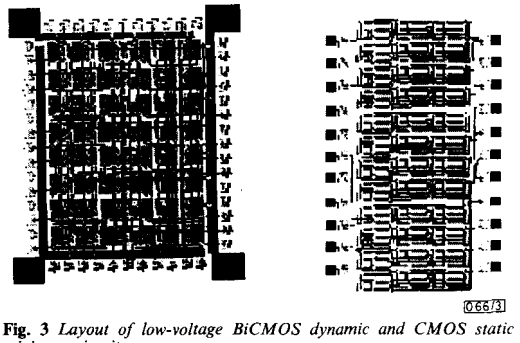

Fig. 3 *Layout of low-voltage BiCMOS dynamic and CMOS static minimum circuits*

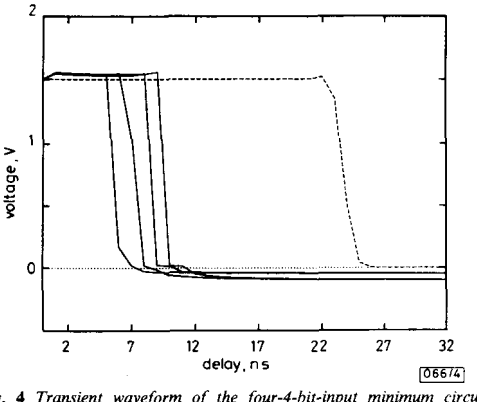

Fig. 4 *Transient waveform of the four-4-bit-input minimum circuit using the low-voltage BiCMOS dynamic and CMOS static circuits*

—— Bi*p*MOS
----- CMOS

Performance: To show the effectiveness of the low-voltage BiCMOS dynamic minimum circuit, a test chip including the four-4-bit-input minimum circuit using the 1.5V BiCMOS dynamic circuit and the 1.5V CMOS static circuit based on a 1μm BiCMOS technology, which has a gate oxide thickness of 180Å, a threshold voltage of ±0.7V and a bipolar device with a unity gain frequency of 8GHz, has been designed. The aspect ratios of all *n*MOS and *p*MOS devices used are 36μm/1μm and 64μm/1μm, respectively. Fig. 3 shows the layout of the 1.5V BiCMOS dynamic circuit and the CMOS static circuit. The die areas of the dynamic and CMOS static circuits are 755 × 919μm² and 609 × 959μm², respectively. Fig. 4 shows the transient waveform of the four-4-bit-input minimum circuit using 1.5V BiCMOS dynamic and CMOS static circuits. The propagation delay of the BiCMOS dynamic circuit is 9.5ns, which is 2.5ns less as compared to that of the CMOS static circuit. In addition, the 1.5V BiCMOS dynamic minimum circuit using a parallel comparison algorithm has an expansion capability to realise large-scale minimum circuits: 4 bit inputs using five four-4-bit-input minimum circuits. Compared with the conventional minimum circuit that does not use the parallel comparison algorithm, this BiCMOS dynamic minimum circuit is much more compact.

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References

1 KUO, J.B., CHEN, S.S., CHIANG, C.S., SU, K.W., and LOU, J.H.: 'A 1.5V BiCMOS dynamic logic circuit using a 'BiPMOS pull-down' structure for VLSI implementation of full adders', to be published in *IEEE Trans. Circuits and Systems*
2 WATANABE, H., DETTLOFF, W.D., and YOUNT, K.E.: 'A VLSI fuzzy logic controller with reconfigurable, cascadable architecture', *IEEE J. Solid State Circuits*, 1990, pp. 376–380
3 SASAKI, M., INOUE, T., SHIRAI, Y., and UENO, F.: 'Fuzzy multiple-input maximum and minimum circuits in current mode and their analyses using bounded-difference equations', *IEEE Trans. Computers*, 1990, pp. 768–774
4 CHEN, S.S., CHIANG, C.S., SU, K.W., and KUO, J.B.: 'BiCMOS dynamic minimum circuit using a parallel comparison algorithm for fuzzy controllers', *Electron. Lett.*, 1993, **29**, (6), pp. 551–553
5 KUO, J.B., LIAO, H.J., and CHEN, H.P.: 'A BiCMOS dynamic carry look-ahead adder circuit for VLSI implementation of high speed arithmetic unit', *IEEE J. Solid State Circuits*, 1993
6 HIRAKI, M., YANO, K., MINAMI, M., SATO, K., MATSUZAKI, N., WATANABE, A., NISHIDA, T., SASAKI, K., and SEKI, K.: 'A 1.5V full-swing BiCMOS logic circuit', *IEEE J. Solid State Circuits*, 1992, **SC-27**, (11), pp. 1568–1573

Temperature dependence of gate induced drain leakage current in silicon CMOS devices

K. Rais, F. Balestra and G Ghibaudo

Indexing terms: CMOS integrated circuits, Silicon, Semiconductor device testing

The temperature dependence of the gate induced drain leakage (GIDL) current in CMOS devices is investigated from 20K up to 300K. It is shown that, at sufficiently high electric field, the conventional band-to-band tunnelling GIDL current law is applicable down to near-liquid helium temperatures for both N- and P-channel devices. The exponential factor *B* of the GIDL current law is found to be nearly independent of temperature. Moreover, the decrease of the GIDL current as the temperature is lowered, is shown to originate from the temperature variation of the pre-exponential coefficient *A* of the GIDL current law.

Introduction: Gate induced drain leakage (GIDL) may constitute a serious constraint as regards off-state current in the scaling down process of ULSI CMOS technologies [1–4]. On the other hand, the operation of MOS devices at low temperature could represent a