AAIC Homework 4

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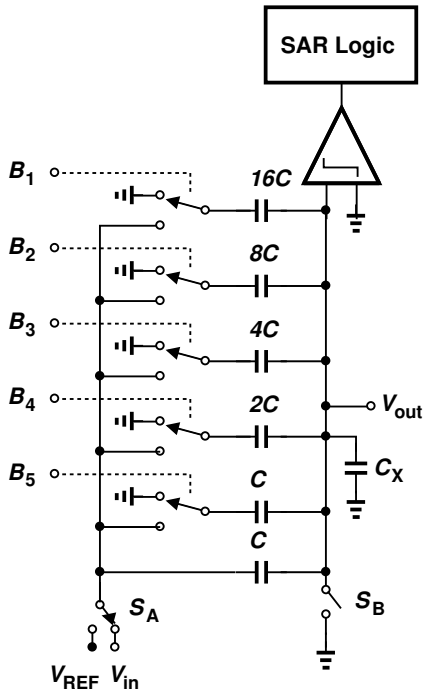
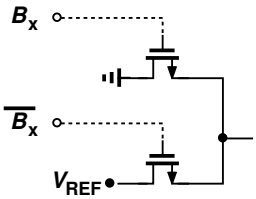
1. For a 5-bit SAR ADC can be implemented as the following. You can also read Sedra/Smith Microelectronic Circuits pg 933 for the detail operation



(a)



(b)

(a) In order to avoid charge injection effect of switch S_A, please draw the detail timing diagram to control the switches.

(b) Now if C_x is equal to 0.5C. Draw the DNL and INL. Note that you draw DNL/INL as a function of the output codes (there are 31 code transition). To maintain DNL less than 1/2 LSB, what's the requirement for C_x?

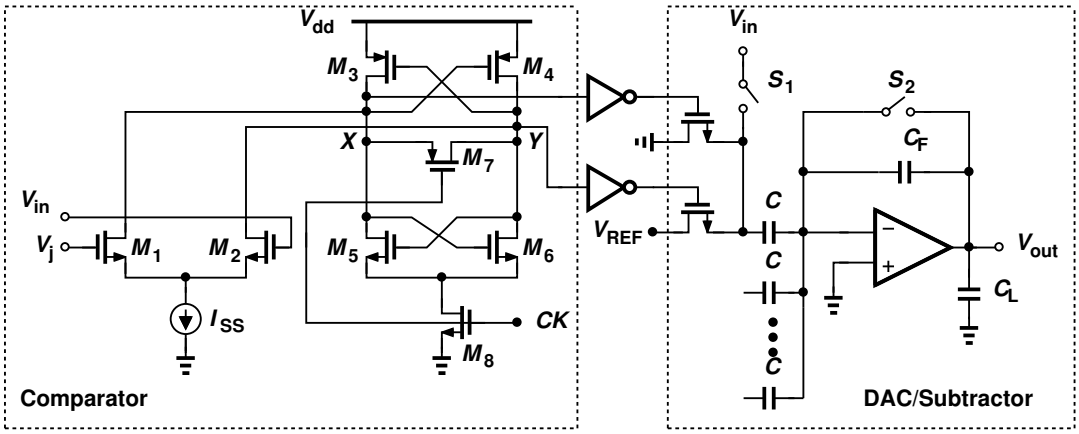
(c) If comparator has an offset voltage V_{os}, what's DNL and INL? Again, draw DNL/INL.

(d) If the double-throw switches (B_x) are implemented as in (b), what's the effect of overlap capacitor feedthrough? Let's say each transistor has an overlap capacitor C_{ov}?

(e) What's the effect of the charge injection of switches B_x? You can assume the charge difference underneath channel is ΔQ for connecting switches between GND and V_{REF}.

2. In this problem, we analyze the critical path in a two-step 9-bit ADC (with 4 bits resolved in coarse stage and 5 bits in fine stage). Shown below is a slice of the converter up to the input of the second stage (the front-end SHA is not shown):

For simplicity, assume $W/L = 10/0.3$ for all the devices except M_3, M_4 and M_7 and model the op



amp with $g_m = 0.001\ \Omega^{-1}$ and $R_o = 1\ \text{M}\Omega$ (As in HW #2, make sure you include nonlinear region for this problem). The power supply (V_{dd}) is equal to 1.8 V. The bias current of the comparator (I_{ss}) is equal to 50 μA and the reference voltage of DAC (V_{REF}) is equal to 0.7 V. Also, $V_j = 0.5$ V, and V_{in} is held (by the SHA) at 0.501 V. The load capacitance C_L represents the total input capacitance of the 32 comparators in the second stage. $C = 0.15$ pF, $C_F = 1.2$ pF, and $C_L = 0.35$ pF. Switches S_1 and S_2 perform sampling of the analog input onto the DAC/subtractor. You may use 1-GΩ resistors to model these switches. (To make life easier, we assume V_{in} can go down to zero, although that's not possible in the circuit.)

(a) When CK is low, choose the size of M_3 and M_4 such that $V_X = V_Y = 1.1V$ at equilibrium. Then, choose M_7 such that $G_{m34}R_{on7} = 1$. Following that, calculate the small-signal gain of the comparator when CK is low.

(b) Calculate the gain error of the subtractor. Will it cause the overall DNL to greater than 0.5 LSB?

(c) Using a transition time of 0.5 nsec for CK, find the total time needed for the subtractor output to reach within 0.5 LSB with respect to its final value. Repeat this with $V_{in} = 0.531$ V. Which case takes longer? Why?

(d) We need to decide on the best resolution per stage: 4-5, 5-4, 3-6 or 6-3. Assume C_L is proportional to the number of the comparators in the second stage and C_F is chosen such that the subtractor has a voltage gain of 4. simulate 5-4, 3-6 and 6-3 cases and compare the response with that obtained in (c).