A 1.5V BiCMOS Dynamic Subtracter Circuit for Low-Voltage BiCMOS CPU VLSI

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Abstract

This paper presents a 1.5V BiCMOS dynamic subtracter circuit for low-voltage BiCMOS CPU VLSI. With an output load of $0.2pf$, the 1.5V BiCMOS dynamic subtracter circuit shows a more than 2.98 times improvement in speed as compared to the CMOS static one.

1 Introduction

Subtracter circuit is an important circuit in a CPU. Usually, subtraction is done via addition using 2's complement of subtrahend. For a deep submicron BiCMOS technology, scaling power supply is unavoidable [1]. For a deep submicron BiCMOS technology, a 1.5V supply is necessary. With a 1.5V power supply voltage, the BiCMOS dynamic circuit introduced before [2] cannot be used. A 1.5V BiCMOS dynamic logic used for multipliers has been reported [3]. In this paper, a 1.5V BiCMOS dynamic subtracter without using 2's complement is described. In the following sections, the 1.5V BiCMOS dynamic subtracter circuit is described first, followed by performance evaluation and discussion.

2 The 1.5V BiCMOS Dynamic Subtracter Circuit

Fig. 1 shows the block diagram of the 1.5V dynamic subtracter circuit, which is composed of subtracter cells. In each subtracter cell, for both A and B between zero and 1, $A - B$ is obtained by R_i and N_{i+1}:

$$R_i = \overline{N_i} \oplus A_i \oplus B_i, \qquad i = 1, 8 \qquad (1)$$
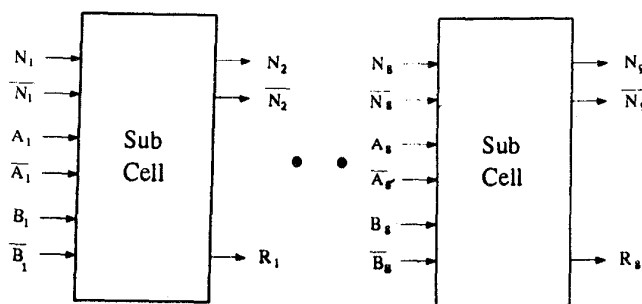$$N_{i+1} = A_i\overline{B_i} + A_iN_i + N_i\overline{B_i}, \qquad i = 1, 8 \qquad (2)$$

Figure 1: Block diagram of the 1.5V BiCMOS dynamic subtracter circuit.

If $A > B$, R is $A - B$ and $N_9 = 1$, which represents a positive result. If $A < B$, R is equal to $1 - A + B$ and $N_9 = 0$, which implies a negative result. Fig. 2 shows N, $\overline{N}$, R, and $\overline{R}$ circuits used in the subtracter cell. These circuits are based on the BiCMOS dynamic circuit using a BiPMOS pulldown structure [3]. The operation of the BiCMOS dynamic circuit is divided into two periods – the precharge period and the logic evaluation period. During the precharge period, CK is low, the output is pulled high to V_{DD}. At this time, the bipolar device is turned off by the NMOS device, which is controlled by FB coming from the CMOS NAND gate. After the precharge period, during the logic evaluation period, both the precharge PMOS device and the NMOS device are turned off. If both inputs are low ($0V$), the bipolar device is turned on. As a result, the output is pulled low to the ground level. After the output is pulled down, FB will switch to high. As a result, the bipolar device is turned off. During operation, the bipolar device is on only during switching. In order to avoid charge sharing problems
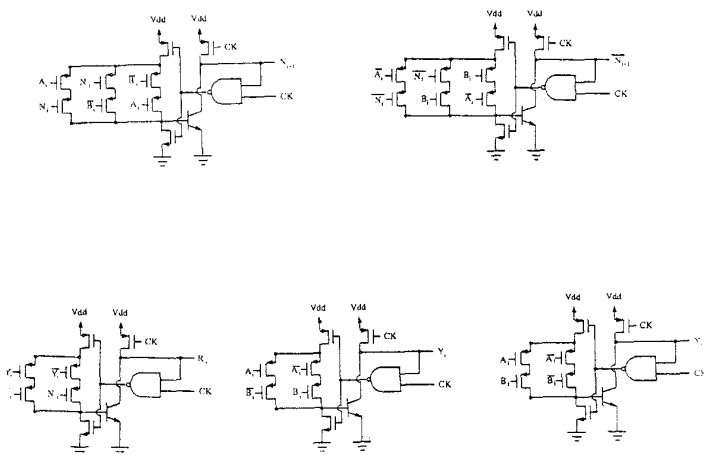
Figure 2: Circuit diagrams of the subtracter cell using the 1.5V BiCMOS dynamic circuit. (a) NB circuit. (b) $\overline{NB}$ circuit. (c) R circuit. (d) Y circuit. (e) $\overline{Y}$ circuit.

Figure 3: Layout of the 8-bit subtracter using the 1.5V BiCMOS dynamic circuit. The die area is $747\mu m \times 836\mu m$.

[2], in each path, only two input PMOS transistors are stacked together. Owing to the BiPMOS pulldown structure, a full swing of 1.5V is obtained.

3 Performance Evaluation & Discussion

In order to show the effectiveness of the 1.5V BiC-MOS dynamic subtracter circuit, a test chip including an 8-bit BiCMOS dynamic subtracter circuit and an 8-bit CMOS static circuit has been designed based on a $1\mu m$ BiCMOS technology. Fig. 3 shows the layout of the 8-bit 1.5V BiCMOS dynamic subtracter circuit, which occupies an area of $747\mu m \times 836\mu m$. Fig. 4 shows the transient waveforms at each cell ouput of the 8-bit subtracter using 1.5V BiCMOS dynamic and CMOS static circuits. Using the BiCMOS dynamic circuit, the speed improves 2.98 times.

4 Conclusion

In this paper, a 1.5V BiCMOS dynamic subtracter circuit for low-voltage CPU VLSI. With an output load of 0.2pf, the BiCMOS dynamic subtracter circuit shows a more than 2.98 times improvement in speed as compared to the CMOS static one.
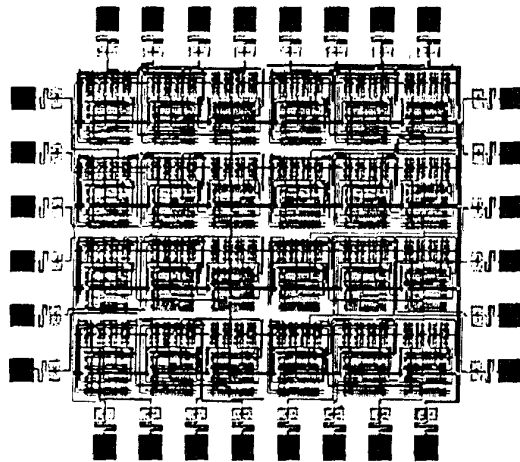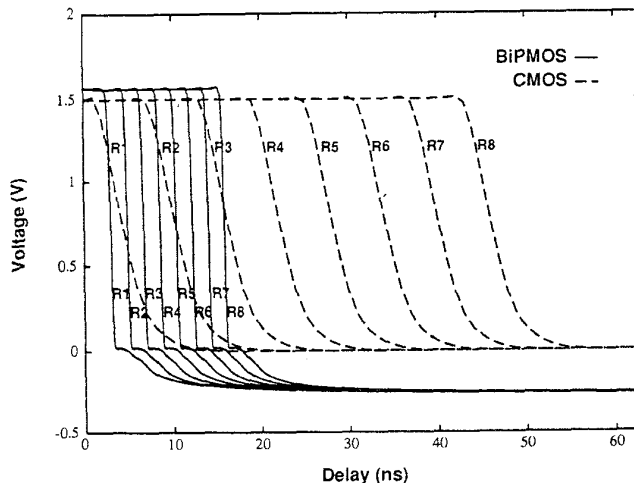

Figure 4: Transients of the 8-bit subtracter using the 1.5V BiCMOS dynamic circuit and the CMOS static circuit.

References

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