Evidence of Si/SiGe heterojunction roughness scattering

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The separation distance between the electron channel at oxide/Si interface and the strained-Si/relaxed-SiGe heterojunction can significantly affect the effective electron mobility of metal–oxide–silicon field-effect transistors due to the roughness scattering of the underneath Si/SiGe heterojunction. The mobility degradation due to the Si/SiGe heterojunction with the roughness of 7 nm becomes insignificant when the strained-Si thickness is larger than ~20 nm. A clear hole confinement shoulder is observed in the accumulation region of the capacitance–voltage curves, indicating that the abrupt transition from the SiGe buffer to strained Si is maintained at the rough heterojunction. The heterojunction roughness scattering not only degrades the electron mobility, but also degrades the device characteristics such as the transconductance and cut-off frequency. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1828224]

The large drain saturation current (Idsat) of metal–oxide–silicon field-effect transistors (MOSFET) is obtained by scaling the thickness of gate insulator (oxynitride) down to the limit of quantum mechanical tunneling. To avoid the gate current leakage, strained-Si is used to enhance electron mobility and thus the Idsat without using the leaky ultrathin oxynitride.[1,2] Alternatively, high dielectric-constant material can be potentially used to reduce the gate leakage and to increase the Idsat, but suffers the process temperature instability, interfacial layer, and remote phonon scattering.[3,4] Conventionally, the strained-Si is grown on the relaxed SiGe to obtain tensile strain in the Si and a strained-Si/relaxed-SiGe heterojunction is inevitably formed underneath the carrier channel. Note that the strain of Si originates from the lattice misfit between the Si and relaxed SiGe grown on the Si substrate. The relaxation of SiGe causes the roughness on the SiGe surface on the order of several nanometers, and forms the rough Si/SiGe heterojunction, which has the potential impact on the carrier scattering. It is well known that the roughness scattering from the oxide/Si interface is an important factor to affect the high field carrier mobility in the conventional device,[1] where the oxide roughness is only several tenths of nanometer. The effect of the heterojunction scattering can be reduced by the chemical mechanical polishing of the SiGe buffer[5] or by increasing thickness of strained-Si at the expense of the possible extra misfit and threading dislocations generated in Si. Even though the thick strained-Si with few defects can be obtained at the low growth temperature (500–700 °C) due to metastable growth, the high process temperature can make strained Si reach the equilibrium state with possible dislocation generation.[6–8] Therefore, it is interesting and technologically important to know the minimum thickness of strained-Si to reduce the Si/SiGe heterojunction roughness scattering.

The *n*-channel MOSFETs were fabricated on a 100 mm wafer. The $Si_{1-x}Ge_x$ buffer layer was expitaxially grown on a *p*-type Si substrate at 600 °C by ultrahigh-vacuum chemical vapor deposition. Silane (SiH_4) and germane (GeH_4) were used as the Si and Ge precursors, respectively. After the graded $Si_{1-x}Ge_x$ buffer layer with $x=0$ to 20% over the thickness of ~1 μm was grown, a ~1-μm-thick relaxed $Si_{0.8}Ge_{0.2}$ layer was then deposited on the top of the graded buffer layer. The strained-Si channel with the thickness from 12 to 24 nm was grown on the relaxed $Si_{0.8}Ge_{0.2}$ layer to investigate the thickness effect on Si/SiGe heterojunction scattering. The rms value of surface roughness of the MOSFETs measured by atomic force microscopy is around 5.3 nm, and the strain in the Si channel measured by the micro-Raman spectroscopy[9] is ~0.7% (Fig. 1). The interface roughness at the SiGe/Si heterojunction cannot be measured directly, but it is believed that the interface roughness is similar for all the devices, since all the devices have the same structure (the inset of Fig. 1) and the same thermal budget. The bare SiGe buffer without Si cap has a roughness ~7 nm, and the Si cap can smoothen the surface to yield a roughness of 5.3 nm. The heterojunction roughness is believed to be ~7 nm. The doping concentration of control Si is $\sim 2\times10^{15}$ cm^{-3}. All strained-Si devices have doping concentration of 1×10^{17} cm^{-3}, except the 20 nm strained-Si channel ($\sim 1\times10^{16}$ cm^{-3}). Note that the mobility at high field perpendicular to the channel is not dependent on doping concentration due to the carrier screening. A 20 nm tetraethylorthosilicate (TEOS) deposited at 700 °C was used as gate dielectrics to avoid Ge outdiffusion during the high temperature thermal oxidation process, since the injection of Si in-

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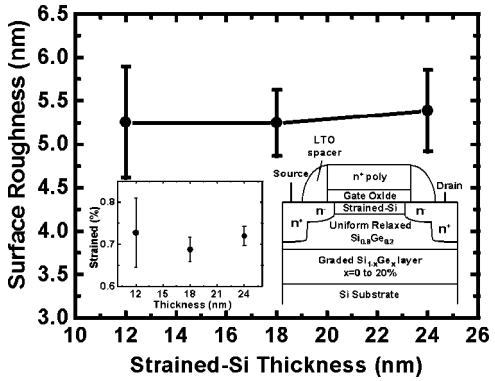

FIG. 1. The surface roughness on strained-Si of the MOSFET devices. Note that the roughness of relaxed SiGe surface is ~7 nm before deposition of the strained-Si channel layer. The area of AFM measurement is $50\times50\ \mu m^2$. The inset is the strain of the Si channel measured by micro-Raman spectroscopy.

terstitials by the thermal oxidation can enhance the Ge out-diffusion and yield high interface trap density.[10] The interface trap density (D_{it}) at midgap, extracted by high–low frequency capacitance–voltage ($C-V$), is $\sim1\times10^{11}\ cm^{-2}\ eV^{-1}$, which is low enough not to degrade the carrier mobility, according to our calculation. Note that due to the roughness of our sample (7 nm) and thin strained Si layers (12–24 nm), the secondary ion mass spectroscopy cannot give the reliable in-depth Ge profiles to measure the Ge diffusion at the Si/oxide interface.

The quasistatic $C-V$ (Fig. 2) measurement was used to probe the abruptness of the strained-Si/relaxed-SiGe heterojunction. The clear hole confinement shoulders are observed at the accumulation region for all strained-Si devices with different thickness, suggesting an abrupt transition from $Si_{0.8}Ge_{0.2}$ to Si at Si/SiGe heterojunction interface.[11,12] The hole confinement at the heterojunction interface (the inset of Fig. 2) forms an extra capacitor in parallel with the oxide capacitance, and leaves the shoulder on the $C-V$ curve as a signature. Numerical simulation shows that a graded junction at $Si/Si_{0.8}Ge_{0.2}$ with a graded rate of 10% Ge/nm cannot have such hole confinement. Note that the strained-Si has lower valence band edge in energy than the relaxed SiGe buffer, and an energy barrier is formed to prevent a fraction of the holes from reaching the oxide/strained-Si interface (the inset of Fig. 2). However, the defects in the strained Si

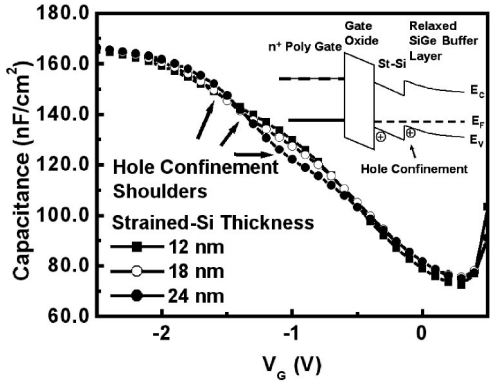

FIG. 2. Quasistatic $C-V$ measurement of the strained-Si devices. The gate oxide is 20 nm TEOS. All the devices show the shoulders in the curves, indicating abrupt Si/SiGe interfaces. The hole confinement is shown in the inset.

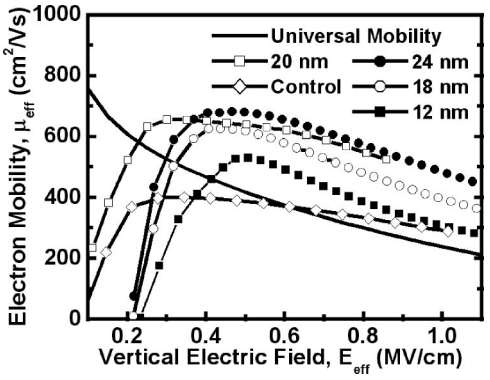

FIG. 3. The effective electron mobility of strained-Si. The thicker strained-Si channel has a higher mobility.

and the relaxed SiGe can also trap holes to form the similar shoulders in the $C-V$ curves, but the $C-V$ measurement at elevated temperature can de-trap the hole and the shoulder vanishes. The shoulder in our samples is maintained at the elevated temperature up to 150 °C, and this further confirms that the shoulders in the $C-V$ curves are due to the hole confinement at heterojunction. The capacitance value at the shoulder increases with the decreasing strained-Si thickness (Fig. 2), because the thinner strained-Si defines a larger capacitance.

All MOSFET devices show the good linear and saturation regions of the output characteristics. The typical drain current enhancements for strained-Si (20-nm-thick) devices with the gate width (W) of 25 μm and the gate length (L) of 1 μm are found to be ~35% at the saturation and ~65% at the linear regions as compared to the control Si devices. The 20 nm strained-Si devices show a mobility (μ_{eff}) enhancement of ~65% at 1 MV/cm compared to control devices. The threshold voltage shift is ~−0.14 V as compared to the control Si devices due to the lower conduction band edge of strained-Si as compared to Si.[12] The effective mobility is extracted from the split $C-V$ and the output characteristics of the MOSFET devices.[13] The mobility at the low field (≲0.4 MV/cm) is dominated by impurity scattering (Coulumb scattering), and the high field mobility (~1 MV/cm) is determined by the roughness scattering and the phonon scattering.[1] Note that the electric field in the horizontal axis of Fig. 3 is the field perpendicular to the electron channel and is controlled by the gate voltage. Conventionally, the roughness scattering is originated from the oxide/Si interface, which is the same in all the samples. The high field mobility in our samples increases as the thickness of the strained-Si increases (Fig. 3). Since all the samples have similar oxide/strained-Si interface, the only mechanism to yield the difference in mobility is the scattering from the strained-Si/ relaxed-SiGe heterojunction. The thicker strained-Si can make the electrons in the oxide/strained-Si channel further away from the heterojunction roughness and yields the higher mobility at the high field. The shoulders on the $C-V$ curves clearly show that the potential at the heterojunction can affect the carrier kinetics and thus can potentially scatter the remote electrons in the oxide/strained-Si channel. The roughness at the heterojunction for all the samples is estimated to be ~7 nm. For the strained Si thickness larger than 20 nm, the effect of the heterojunction roughness becomes weak, and the mobility remains almost constant. For the device with a gate length of 0.8 μm, gate

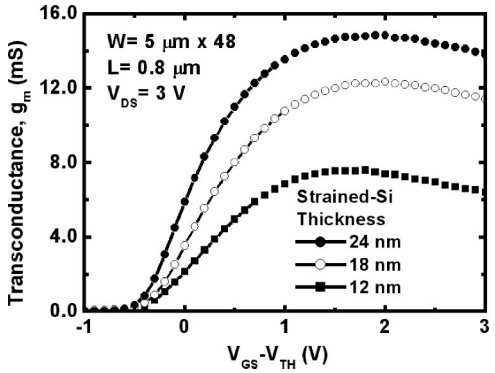

FIG. 4. The transconductance (g_m) for different strained-Si channel thickness.

width of 5 μm, and 48 fingers, the transconductance g_m also increases with increasing strained-Si thickness (Fig. 4), since the higher mobility for the thicker strained-Si sample yields a larger drain current. For the device speed characterized by the cut-off frequency (f_T),[14] the high mobility can reduce the transit time in the channel for the electron traveling from the source to the drain. The thicker strained-Si gives the higher cut-off frequency (Fig. 5).

In conclusion, the device performance such as transconductance and cut-off frequency is improved with the increasing thickness of the strained-Si channel by the reduction of the underneath Si/SiGe heterojunction roughness scattering. With the Si/SiGe heterojunction roughness of ~7 nm, the minimum thickness of strained-Si to reduce the Si/SiGe heterojunction scattering is ~20 nm. However, for the different roughness at the heterojunction, this minimum thickness can be different. The chemical mechanical polishing to remove the roughness at heterojunction seems not to be the only way to maintain the high mobility of the strained-Si channels.

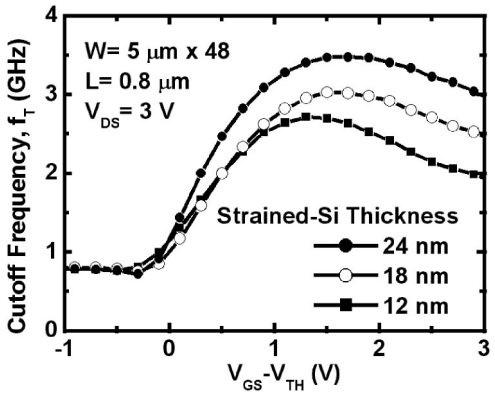

FIG. 5. The cutoff frequency f_T for different strained-Si channel thickness.

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