A NOVEL CURRENT MODEL FOR CMOS GATES *

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ABSTRACT

Accurate current analysis is required in circuit designs to analyze electromigration failure rate, power consumption, voltage drops, etc. A new current model for CMOS gates is presented in this paper. The current waveform of a CMOS gate can be divided into three regions and the characteristics in each region can be approximated by an exponential function. After analyzing the possible transition of a gate, the current waveform under one input vector can be obtained with only four parameters. This model can be used in any switch-level timing simulators to generate the current waveforms after the voltage waveforms are obtained. The simulated current waveform, instead of the average estimation, helps solving the VLSI reliability problems due to the electromigration and excess voltage drops in the power buses. When comparing the results obtained by using SPICE and our model, we can find the agreement, especially the time points that current pulses happen.

1 Introduction

The quality of an integrated circuit is measured by both functional and reliability standards. Many simulation approaches exist to verify that a design will meet functional specifications. Within the past decade, the CAD community has developed an impressive array of graphics layout systems, geometric design rule checkers, circuit extractors, simulation tools and timing analyzers to manage the mass complexity of the current day VLSI digital designs. Recently, the researches of the high-level synthesis try to finish the circuit design directly from the functional specifications. Meanwhile, the reliability of integrated circuits is quickly becoming a major concern for the electronics industry because the circuit is more large and the speed is more fast ; this creates a need for efficient and accurate CAD tools that guarantee design reliability.

In large integrated circuits, such as in VLSI/ULSI, current flow in power and ground buses leads to the problems of voltage drop and metal migration, which is the major reliability problem. The problems are especially important in the widely-used CMOS technology, where switching transients from different part of a circuit can occur almost simultaneously and thus, may originate large noise spikes (in the form of voltage drops) in the power/ground buses. Unrestricted voltage drops in the power/ground buses may result in incorrect logic operation and degradation in switching speed. Restricting voltage drops to safe limits requires the knowledge of peak currents in the power/ground buses. Among the existing approaches, Cirit [1], Tyagi [2], and Burch et al. [3] applied the value-independent algorithm to avoid a large amount of test vectors problem. These, however, may not reflect the "real" current pattern since the waveform shape, compared with the power consumption, is much more input-dependent. The probabilistic waveform presented in [3] seems to be a reasonable estimation for measuring electromigration failures, but provides little information about the worst-case voltage drop in the power bus.

A time-domain current waveform simulation is proposed in [4]. In this literature, the current associated with a high-to-low/low-to-high state transition is approximated by a triangular current pulse by the triplet $(s.time, I_{peak}, \Delta T)$ where $s.time$ is the time that I_{peak} occurs and ΔT is the time width that the current pulse occupies. This model can achieve great accuracy when the load capacitances of each gate are small. But when the load capacitance or the fan out is large, the current waveform is asymmetric, so it will results in large errors to approximate the current waveform with an isosceles triangle. Also because the asymmetry, the peak current obtained by the model in [4] will deviate from the real peak current, so the peak value of the total current after the summation is not correct. Although better estimation can be achieved by using an asymmetric triangular pulse parameterized by $(time, I_{peak}, \Delta T_1, \Delta T_2)$ where ΔT_1 and ΔT_2 are respectively the rising and falling times of the pulse, but it is very difficult to calculate these two times. We adopt another approach which is more complex, but it can give accurate results even when the load capacitance is very large. The current waveform of a CMOS gate can be divided into three regions and the characteristics in each region can be approximated by an exponential function. After analyzing the possible transition of a gate, the current waveform under one input vector excitation can be obtained with only four parameters.

Our work is based on a switch-level timing simulation for various input vectors. The dynamic simulation, com-

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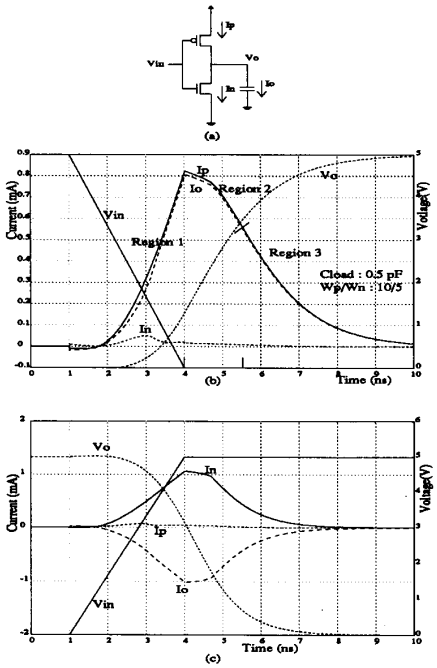

Figure 1: (a) A CMOS inverter with a load capacitance 0.5pF. (b) and (c) : The waveforms of currents and voltages of the CMOS inverter when the input signal changes from high to low and low to high.

pared with the static current estimation [2, 3], in general will suffer from the excessively CPU time. We develop this current simulator based on (1) the event-driven technique, (2) a recursive technique for computing delays in series-parallel MOS transistor circuits [5], and (3) the precharacterized current model, so as to reduce the simulation time to within a practically acceptable level. When comparing the results obtained by using SPICE and our model, we can find the agreement, especially the time points that current pulses happen.

2 Current Model

We consider the model by using an example of currents flowing from V_{DD} to to GND in the CMOS inverter gate as shown in Fig. 1(a). Fig. 1(b) and (c) show the voltage waveforms and the current waveforms of this gate. When V_{in} decreases, the output voltage V_o increases. Because the input signal V_{in} is not a pulse in most cases, so the transition can be divided roughly into three regions. Before the input begins to decrease, the pMOS is off and the nMOS is on. After the input begins to change, the pMOS will turn on firstly, and then the nMOS will turn off. After the pMOS turns on, there is a large current flowing from the power bus into the load capacitance. Meanwhile, there is a small current flowing to GND through the nMOS before the nMOS turns off. By applying the Kirchhoff's current law,

$$I_p = I_o + I_n. \tag{1}$$

In this case, I_n is the so-called short-circuit current which is small compared with I_p and I_o, as shown in Fig.1(b). Owing to the existence of the parasitic capacitances, there are currents induced when the input is changing. Its quantity is a function of the changing rate of the input signal. As shown in Fig.1(b), this quantity is small and can be neglected. On the other hand, if V_{in} increases, then V_o decreases. A large current flows from the load capacitance into the ground. Then I_p is the so-called short-circuit current. In the case, only I_p flows from the power bus. So in each case, we add I_P only to the total current provided by the power bus.

As shown in Fig. 1, the current waveform is asymmetric. More large the load capacitance, more asymmetric the current waveform is. Not as assumed in [4] that the current waveform is approximated by an isosceles triangle, we divide the current waveform into three regions. In region 1, the input signal changes state and the pMOS is saturated. The current begins to increase in this region. In this region, the pMOS is saturated. If we neglect the second order effects and the channel modulation effect, the pMOS can be viewed as a constant resistance. So the waveform of the output voltage is an exponential function, and also the current, because the derivation of an exponential function is also an exponential function. When the input signal reaches the final state or the pMOS leaves out the saturation region, the current reaches the peak value for most cases and then enters into the region 2. It is difficult to describe the current waveform after the peak value point with just one time constant, so we divide this region into two regions. For calculating simplicity, the current enters region 3 when its value is 70% of the peak current. In region 2 and 3, pMOS is in linear region. The behavior of the current waveform is very much complex. But as shown in Fig 1(b), these two regions can still be approximated by exponential functions. So in our model, the current waveform is approximated by three exponential functions with four parameters, I_{peak}, τ_1, τ_2, and τ_3.

$$\begin{aligned} I &= \Delta \cdot e^{\frac{t}{\tau_1}} && when \;\; t < T_{peak} \\ &= I_{peak} - \Delta \cdot e^{\frac{t-T_{peak}}{\tau_2}} && when \;\; T_{peak} < t < T_{crit} \\ &= 0.7 \cdot I_{peak} \cdot e^{-\frac{t-T_{crit}}{\tau_3}} && when \;\; t > T_{crit} \end{aligned}$$

where T_{peak} is the time that the current reaches its maximum value I_{peak}. T_{crit} is the time that the current decreases to 70% of I_{peak}. Δ is a constant used to matching the curve. Fig. 2 shows the comparison between two

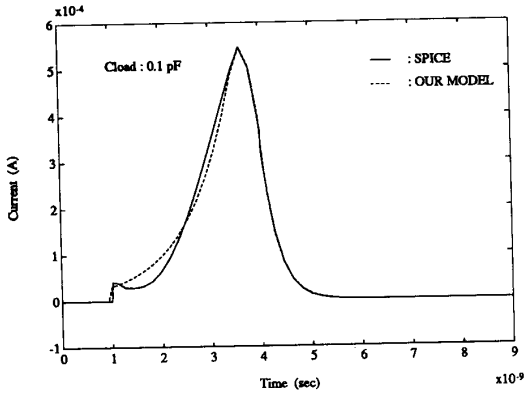

Figure 2: The current waveforms obtained by using SPICE and obtained by three matching exponential functions.

current waveforms. The solid curve is obtained by using SPICE to simulate an inverter. The dashed curve is the matching result using the above three exponential functions. It seems to be very accurate when the current decreases from its peak value. The large error in region 1 is due to the existence of the gate capacitance. When the input signal changes, the voltage drop across the gate capacitance changes, and then current flows across the capacitance. So the current waveform in region 1 is the summation of the currents of the gate capacitance and of the MOS transistors.

3 Macro Modeling

The MOS transistor can be viewed as a linear resistance in switch-level tools, so the voltage waveforms and the current waveforms are functions of the total effective resistance of the gate. Of course, it is also a function of the load capacitance. The total effective resistance depends on how many MOS turns on in the gate, the size of the turned-on MOS and the slopes of the input signals. So the current waveforms of a gate under various input excitations are different. For example, the current waveforms of a 2-input NAND gate may be one of the four cases shown in Fig 3, two for high-to-low transition and two for low-to-high transition. We analysis the effective transition of input vectors for each basic logic gate, and establish four empirical functions for I_{peak}, τ_1, τ_2, and τ_3 for each logic gate with one effective transition. I_{peak}, τ_1, τ_2, and τ_3 are functions of load capacitances, aspect ratios of MOS transistors, and the slopes of input signals. So for each input transition of each gate, we can obtained four equations.

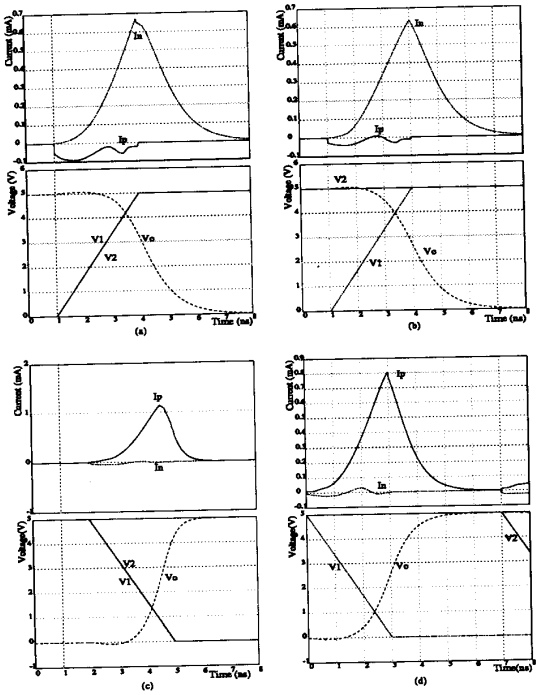

Figure 3: The current and voltage waveforms of a 2-input NAND gate under various input transition. (a) 00 → 11, (b) 01 → 11, (c) 11 → 00, and (d) 11 → 01.

$$I_{peak} = F_1^*(S_{in}, W/L, C_{load}) \quad (2)$$
$$\tau_1 = F_2^*(S_{in}, W/L, C_{load}) \quad (3)$$
$$\tau_2 = F_3^*(S_{in}, W/L, C_{load}) \quad (4)$$
$$\tau_3 = F_4^*(S_{in}, W/L, C_{load}) \quad (5)$$

where $*$ is the effective input transition for the gate. For example, the effective input transition for a 2-input NAND gate are 00 → 11, 01 → 11, 11 → 00 and 11 → 01, two for high-to-low transition and two for low-to-high transition. In the analysis, 01 and 10 are views as the same. For an n-input gate, the number of total input transition is $2^n \cdot (2^n - 1)$. But the number of the effective input transition is less than this. For a n-input NAND/NOR gate, the number of the effective input transition is $2 \cdot n$, not $2^n \cdot (2^n - 1)$, as shown in Fig. 4(a). For a n-input complex gate, the effective input transition will be larger than $2 \cdot n$, but less than $2^n \cdot (2^n - 1)$. For example, there are 16 effective input transitions for a three-input CMOS complex gate with function $Z = (A + B) \cdot C$. These transitions are shown in Fig. 4(b).

After an event is processed, the current waveform associated with this event can be obtained by choosing suitable functions with the input transition of that gate and their

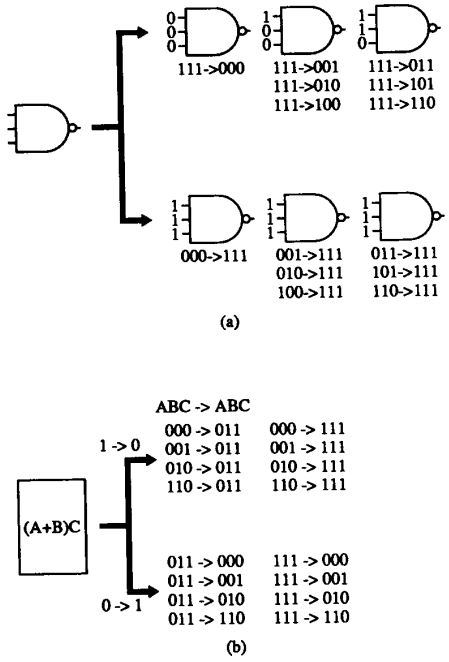

Figure 4: (a) The effective combination of inputs transitions for a 3-input NAND gate, and (b) the effective input transitions of a CMOS complex gate $(A+B)\cdot C$.

slopes at that event time. For example, an event occurs when the input vectors change from 11 to 01 for a 2-input NAND gate, we can obtain I_{peak}, τ_1, τ_2, and τ_3 with the four equations.

$$I_{peak} = F_1^{11\to 01}(S_1, S_2, W/L, C_{load}) \quad (6)$$
$$\tau_1 = F_2^{11\to 01}(S_1, S_2, W/L, C_{load}) \quad (7)$$
$$\tau_2 = F_3^{11\to 01}(S_1, S_2, W/L, C_{load}) \quad (8)$$
$$\tau_3 = F_4^{11\to 01}(S_1, S_2, W/L, C_{load}) \quad (9)$$

where S_2 is zero for this transition. So it is not necessary to search the conducting path to calculate the charges stored in the internal capacitances and then to obtain the current [4].The advantage of this model is the little CPU time and more accurate results when the load is large. Furthermore, the peak current will be more accurate.

4 Result

This current model has been embedded into our switch-level timing simulator. This switch-level timing simulator uses a recursive technique to calculate the delays in the series-parallel MOS circuits [5]. The waveform comparisons with SPICE is shown in Fig. 5 where, for the purpose of comparison, the current waveform is the summation of all the currents from individual subcircuits. The simulated circuit is an one-bit full adder. Because we neglect negative value of the short-circuit current I_p when the gate changes state from high to low, so the results will deviate from that of SPICE when the current is negative. But as shown in this figure, we can find the agreement of these two curves, especially the time points that current pulses happen.

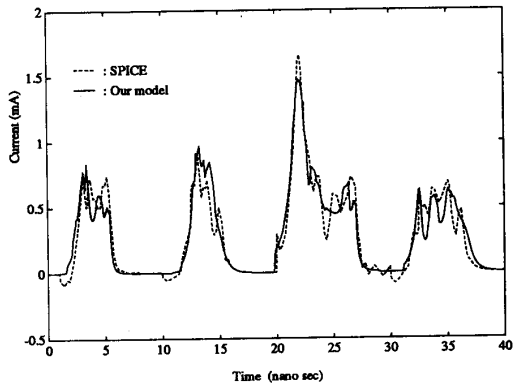

Figure 5: The current waveforms of one bit full adder. The dashed line is the result obtained by using SPICE and the solid line is obtained by using our model.

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