Analog Maximum, Median and Minimum Circuit

Shen-Iuan Liu, Poki Chen, Chin-Yang Chen and Jenn-Gwo Hwu

Department of Electrical Engineering
National Taiwan University
Taipei, Taiwan, R.O.C. China

Abstract

In this paper, we present a new analog maximum, median and minimum circuit with a new preamplifier. This circuit can be used for sorting multiple-input analog signals. The median circuit has been implemented in a 0.8μm single-poly double-metal (SPDM) CMOS process. The measured output error of this median circuit is less than 2.5mV. Its frequency response can be up to 1MHz. The maximum and minimum circuit are also verified by simulations. The experimental and simulation results confirm with the theoretical analysis.

I. Introduction

Median filters play an important role in many applications, such as digital signal processing and image processing [1-7]. Median circuit is the core circuit for a median filter. Maximum and Minimum circuits are also the important building blocks for fuzzy applications such as process control, robotics and expert systems [8-10]. Conventionally, the median, maximum, minimum circuits can be implemented in either digital or analog forms [1-7]. For the median circuits, the most common analog approach is based on a feedback configuration [5]. However, there is a poor transfer characteristic with important 'corner' errors. One way to decrease the corner errors is to use a limiting amplifier with a reduced linear range in stead of simple differential pairs. But the errors is still significant. An improved approach is to place an additional gain stage in the front of the differential pairs [5]. This method requires an amplifier for each input and becomes fairly complex for multiple- input circuits. In this paper, we proposed a new median, maximum and minimum circuit with a new preamplifier which can be used for multiple inputs and this circuit is quiet compact.

II. Circuit Description

The core circuit of this proposed analog maximum, median, and minimum circuit, which consists of three conventional differential pairs and a current source I_{SUM}, is shown in Fig. 1(a). The operation principle of this circuit is explained as follows: Assume that these three differential pairs are matched. Let the voltages V_k (k=1,2 and 3) be input voltages and V_R be the output voltage (in fact, the voltages V_K and V_R are not the true input voltages and the output voltage). If a maximum (MAX) operation is required, i.e., one of the voltages V_K (k=1,2 and 3) is required to be equal to the output voltage V_R and the remaining two voltages will be smaller than V_R. Assuming that the differences among the remaining two voltages and V_R are enough large, then the total current flowing through three diode-connected nMOS transistors (M_2, M_4, M_6), which are connected to the voltage V_R, should be equal to $2.5I_{SS}$. To operate the MAX function by this circuit, the current source I_{SUM} must be equal to $2.5I_{SS}$. That is to

0-7803-3583-X/97 $10.00 ©1997 IEEE

say, if we design the I_{SUM} to be equal to $2.5I_{SS}$, the output voltage V_R will be the maximal voltage among the voltages V_K (k=1,2 and 3). Similarly, if a minimum (MIN) operation is required, the current source I_{SUM} should be equal to $0.5I_{SS}$. Moreover, if a median (MED) operation is required, the current source I_{SUM} must be equal to $1.5I_{SS}$.

However, if any input voltage V_k (k=1,2 or 3) is not equal to V_R, their voltage difference should be enough large to flow the current I_{SS} or no current through the diode-connected transistors in Fig. 1(a). Thus, a new preamplifier circuit, which is shown in Fig. 1(b), is developed to enlarge their voltage differences. For example, let us design an median circuit with $I_{SUM}=1.5I_{SS}$. The gate voltages of the matched pMOS transistors M_{1p}-M_{4p} in the preamplifier circuit are connected to the voltage V_R of the circuit in Fig. 1(a). The voltages V_1 , V_2 and V_3 in Figs. 1(a) and 1(b) are also connected together. The matched nMOS transistors M_{1n}-M_{4n} of the preamplifier circuit are in common source configuration. The transistors M_{kn} (k=1, 2 and 3) and M_{4n} can be viewed as differential pairs. The transistors M_{5p}, M_{6p}, M_{5n} and M_{6n} are used to reduce the channel length modulation effect to make the voltage V_4 to be approximate to the voltage V_R. If any one of the voltages V_{ink} (for k=1, 2 and 3) $>V_{out}$, the equilibrium condition requires that M_{4n} will enter into the triode region since M_{kp} and M_{4p} have the same source-gate voltage. Similarly, if any one of V_{ink}(for k=1, 2 and 3)$<V_{out}$, the corresponding M_{kp} will also enter into the triode region. Thus, once any V_{ink} (for k=1, 2 and 3) is not equal to V_{out}, their difference is amplified to be the voltage difference between V_K (k=1, 2 or 3) and V_4. These voltage differences will be enough large for the circuit in Fig. 1(a) to operate properly. It will force the voltage V_R to be equal to the median among V_1, V_2 and V_3 provided that $I_{SUM}=1.5I_{SS}$. Finally, V_{out} will be equal to the median of V_{in1}, V_{in2}, and V_{in3}. Thus, this preamplifier amplifiers the difference between V_R (or V_4) and any non median V_{ink} (k=1, 2 or 3) to be larger than the linear range of the differential pairs, the "corner" errors will be effectively suppressed. Similarly, the MAX and MIN circuits can also be realized by the same ways. Since the polarity of the voltage V_k and V_{ink} (k=1,2 and 3) are out of phase, the MAX operation will need that $I_{SUM}=0.5I_{SS}$ which is different from the explanation in the beginning of this section. The MIN operation can also be obtained provided that $I_{SUM}=2.5I_{SS}$. Therefore, this circuit can be used to be a sorting circuit with three inputs by programming the current source I_{SUM}.

III. Experimental and Simulation Results

To verify the theoretical analysis, the median circuit with the proposed preamplifier in Figs. 1(a) and 1(b) has been fabricated in a 0.8μm SPDM CMOS process. The aspect ratios for all the transistors are listed in Table 1. The supply voltage is 5V. Fig. 2 show the measured DC transfer characteristic by using $V_{in1}=1.5V$ and $V_{in2}=3.5V$ while V_{in3} was swept from 0 to 5V. The measured error is quiet small (<2.5mV) that is consistent with the simulated one (<2.5mV) when V_{in3} is the median. However, when V_{in1} or V_{in2} is the median, the error is larger than 2.5mV. Its frequency response can be up to 1MHz.

The simulation results of the MAX and MIN operation for a 3-input circuit are also given. Fig. 3 shows the transfer function for a MAX circuit with $I_{SUM}=0.5I_{SS}$ and $V_{in1}=1.5V$ and $V_{in2}=3.5V$. Fig. 4 shows the transfer function for a MIN circuit with $I_{SUM}=2.5I_{SS}$ and $V_{in1}=1.5V$ and $V_{in2}=3.5V$. The

experimental and simulation results confirm the theoretical analysis.

IV. Conclusions

We have presented the simple maximum, median and minimum circuit with the compact preamplifier which can be used to be an analog sorting circuit. Experimental and simulation results have been presented to verify the theoretical analysis. This configuration can be easily generalized to a multiple-input maximum, median and minimum circuit by programming the current I_{SUM}. Moreover, by properly choosing the value of the current source I_{SUM}, this circuit can be made to select any other rank, such as the maximum or minimum.

V. Acknowledgment

The authors would like to thank the National Science Council for financial supporting and thank Chip Implementation Center (CIC), National Science Council, Taiwan, R.O.C., for the fabrication of the test chip. This work was sponsored by NSC-85-2215-E-002-021.

References

[1] K. Oflazer, "Design and implementation of a single-chip 1-D median filter", IEEE Trans. on Acoustics, Speech on Signal Processing, ASSP-31, (5), pp. 1164-1168, Oct. 1983.

[2] Y. H. Lee and S. A. Kassam, "Generalized median filtering and related nonlinear filtering techniques", IEEE Trans. on Acoustics, Speech on Signal Processing, ASSP-33, (3), pp. 672-683, March 1985.

[3] P Heinonen and Y. Neuvo, "FIR-median hybrid filters", IEEE Trans. on Acoustics, Speech on Signal Processing, ASSP-35, (6), pp. 832-838, June 1987.

[4] J. S. Li and W. H. Holms,"Analog implementation of median filters for real-time signal processing', IEEE Trans. Circuits and Systems, CAS-35, (8), pp. 1032-1033, 1988.

[5] P. Dietz and R. Carley, "An analog circuit technique for finding the median", IEEE Custom Integrated Circuit Conf., pp. 6.1.1-6.1.4, 1993.

[6] P. Dietz and R. Carley, "Simple networks for pixel plane median filtering", IEEE Trans. Circuits and Systems, Pt: II, CASII-40, pp. 797-801, Dec. 1993.

[7] I. Opris and G. Kovacs, "Improved analogue median filter", Electron. Lett., vol. 30, (4), pp. 284-285, 1994.

[8] T. Yamakawa, " A programmable fuzzifier integrated circuits -synthesis, design, and fabrication", Information Sciences, vol. 45, pp. 75-112, 1988.

[9] M. Sasaki, T. Inoue, Y. Shirai and F. Ueno, "Fuzzy multiple-input maximum and minimum circuits in current mode and their analyses using bounded-difference equations", IEEE Trans. Computers, vol. 39, pp. 768-774, June 1990.

[10] S. I. Liu, Y. S. Hwang and J. H. Tsay, "CCII-based fuzzy membership function and MAX/MIN circuits", Electronics Letters, vol. 29, pp. 116-117, Jan. 1993.

Table 1. The aspect ratios of the transistors in Fig. 1(a) and Fig. 1(b)

Fig. 1(a)	M_1-M_6,M_{14} M_7-M_9,M_{11}-M_{13}	5μ/2μ
	M_{10}	7.5μ/2μ
Fig. 1(b)	M_{1n}-M_{6n} M_{1p}-M_{6p}	5μ/2μ
	M_{7n}	14μ/2μ

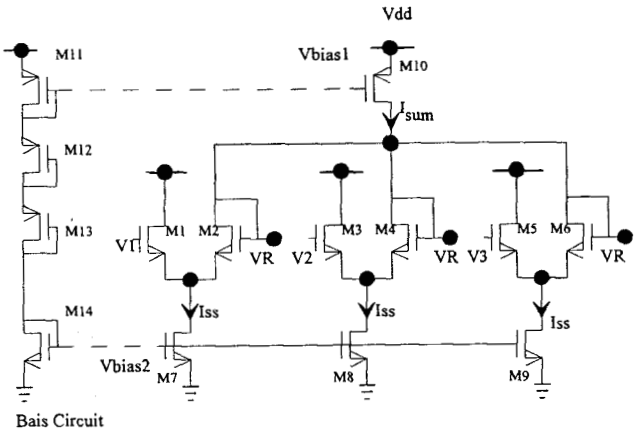

Fig. 1(a)

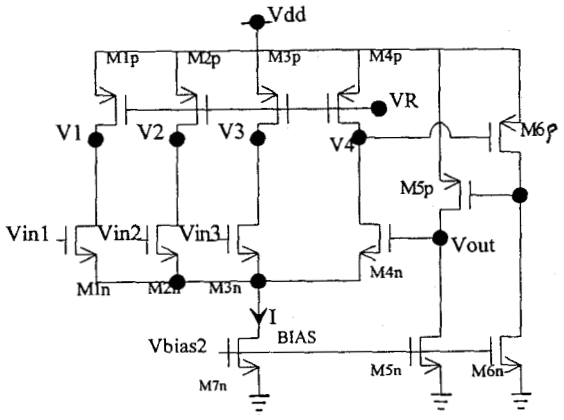

Fig. 1(b)

Fig. 1 The proposed analog maximum, median and minimum circuit with (a) differential pairs and (b) a preamplifier.

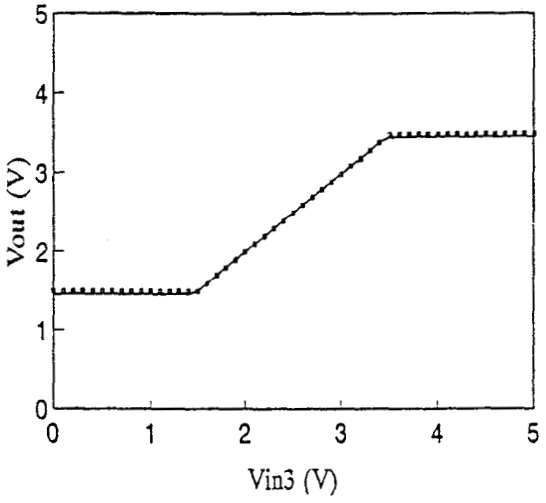

Fig. 2 The measured and simulation results of the median circuit for V_{in3} being swept from 0V to 5V and V_{in1}=1.5V and V_{in2}=3.5V. (□ : Experimental results, - : simulated results)

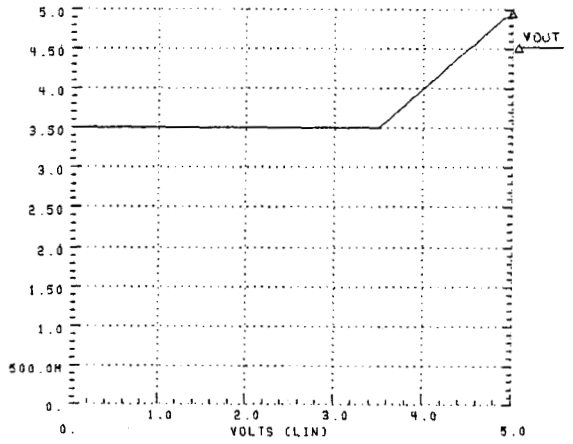

Fig. 3 The simulated transfer function of the MAX circuit with I_{SUM}=0.5I_{SS}, V_{in1}=1.5V and V_{in2}=3.5V.

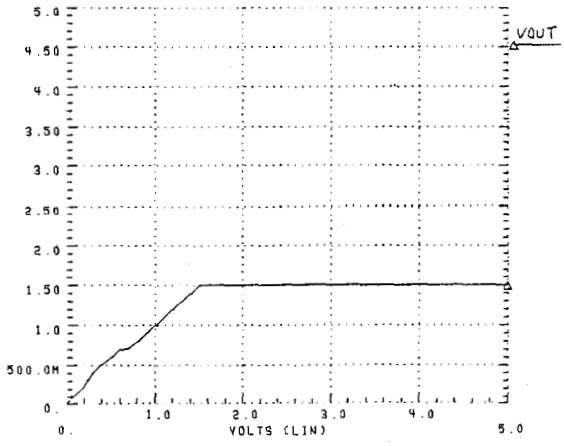

Fig. 4 The simulated transfer function of the MIN circuit with I_{SUM}=2.5I_{SS}, V_{in1}=1.5V and V_{in2}=3.5V.