Briefs

An Analysis of the Anomalous Dip in Scattering Parameter S_{22} of InGaP–GaAs Heterojunction Bipolar Transistors (HBTs)

Hsing-Yuan Tu, Yo-Sheng Lin, Ping-Yu Chen, Shey-Shi Lu, and Hsuan-Yu Pan

***Abstract*—The kink phenomenon in scattering parameter S_{22} of InGaP–GaAs heterojunction bipolar transistors (HBTs) was explained quantitatively for the first time. Our results show that the output impedance of InGaP–GaAs HBTs can be represented by a simple series resistance–capacitance (R–C) circuit at low frequencies and a simple parallel R–C circuit at high frequencies very accurately because of the high output resistance of HBTs. The behavior of S_{22} of HBTs is in contrast with that of field effect transistors (FETs), where the smaller drain–source output resistance R_{ds} obscures the ambivalent characteristics.**

***Index Terms*—HBT, InGaP, kink phenomenon, scattering parameter.**

I. Introduction

The anomalous dip in scattering parameter S_{22} of BJTs or HBTs have been seen frequently in the literatures [1], [2]. Even though qualitative argument has given to explain this phenomenon [3], yet up to now no quantitative analysis has been done for verification. Therefore, in this paper, the work of [3] was extended for the quantitative explanation of the anomalous dip in S_{22} of BJTs or HBTs. The concept of dual-feedback circuit methodology [3] was used to simplify the circuit analysis of the hybrid π-model of an InGaP–GaAs HBT and then the output impedance of the HBT was derived. The formula shows that the output impedance of the HBT follows a constant resistance circle at low frequencies and then a constant conductance circle at high frequencies, which is in excellent agreement with the experimental results.

II. Expressions of Scattering Parameter S_{22}

The setup for the measurement of transistor S-parameter is shown in Fig. 1(a), where $Z_O(=1/Y_O) = 50\,\Omega$ is connected to the input and output ports of the device-under-test. S_{11} and S_{21} can be measured by setting $V_2 = 0$ and $V_1 \neq 0$, while S_{22} and S_{12} can be measured by setting $V_1 = 0$ and $V_2 \neq 0$. What also shown in Fig. 1(a) was the small-signal hybrid π-model of an InGaP–GaAs HBT provided by a commercial foundry. The circuit parameters were extracted from measured S parameters. If the expression for the output impedance $Z_{\rm out}$ of this circuit has been found, then S_{22} is given by

$$S_{22} = \frac{Z_{\rm out} - Z_O}{Z_{\rm out} + Z_O}. \tag{1}$$

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H.-Y. Tu, P.-Y. Chen, S.-S. Lu, and H.-Y. Pan are with the Department of Electrical Engineering, National Taiwan University, Taipei, Taiwan, R.O.C. (e-mail: sslu@cc.ee.ntu.edu.tw).

Y.-S. Lin is with the Department of Electrical Engineering, National Chi-Nan University, Puli, Taiwan, R.O.C. (e-mail: stephenlin@ncnu.edu.tw).

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The circuit configuration, in general, is too complicated to find its output impedance. Nevertheless, if this circuit is viewed as a dual feedback circuit in which R_e is the local series–series feedback element and C_μ is the local shunt–shunt feedback element, then the problem becomes much more tractable. For simplicity, all the inductors in Fig. 1(a) are temporarily neglected. We will refer to them in later discussions in Section III. In addition, pad parasitic capacitances $C_{\rm pbe}$ and $C_{\rm pbe}$ can be neglected because their effect is very small. From local series–series feedback theory [3], the circuit of Fig. 1(a) can be transformed into that of Fig. 1(b) with some necessary circuit element modifications, which are also shown in Fig. 1(b).

Since the hybrid π-model is very similar to the small-signal model of FETs, the derived equations in [3] can be easily applied to case of InGaP–GaAs HBTs with some modifications. Under the assumption that $(1/sC'_\pi \| r'_\pi) \gg R_e$, which is usually the case, the intrinsic output impedance can be expressed as follows:

$$\begin{aligned} Z_{{\rm out},\,i} &= \frac{(sC'_\pi + Y'_{O1})^{-1} + \frac{1}{sC'_\mu}}{1 + g'_m(sC'_\pi + Y'_{O1})^{-1}} \\ &= \frac{1 + s(C'_\pi + C'_\mu)Z'_{O1}}{(1 + g'_m Z'_{O1})sC'_\mu + s^2 C'_\pi C'_\mu Z'_{O1}} \end{aligned} \tag{2}$$

where $C'_\pi = C_\pi/(1 + g_m R_e)$, $C'_\mu = C_\mu$, $g'_m = g_m/(1 + g_m R_e)$, $Z_{O1} = Z_O + R_b$, and $Y'_{O1} = 1/Z'_{O1} = 1/Z_{O1} + 1/r_\pi$. Once this intrinsic output impedance is known, the normal output impedance is nothing but the parallel combination of $Z_{{\rm out},\,i}$ and r'_0, followed by a series combination with R_c as follows:

$$Z_{\rm out} = Z_{{\rm out},\,i} \| r'_o + R_c \approx Z_{{\rm out},\,{\rm i}} + R_c. \tag{3}$$

Here, the symbol $\|$ represents parallel combination. Note that in HBTs collector-to-emitter capacitance and collector-to-emitter output resistance can be neglected because their effect is very small. At low frequencies, the output impedance can be simplified to a series R–C circuit as follows:

$$\begin{aligned} Z_{\rm out} &\approx Z_{{\rm out},\,i} + R_c \\ &\approx \left(\frac{Z'_{O1}}{1 + g'_m Z'_{O1}} + \frac{g'_m}{(Y'_{O1} + g'_m)^2} \times \frac{C'_\pi}{C'_\mu} + R_c \right) \\ &\quad + \frac{1}{j\omega(1 + g'_m Z'_{O1})C'_\mu} \\ &\approx r + \frac{1}{j\omega C_s}. \end{aligned} \tag{4}$$

On the other hand, at high frequencies, the output admittance can be simplified to a parallel R–C circuit as follows:

$$\begin{aligned} Y_{\rm out} &= \frac{1}{Z_{\rm out}} \approx \frac{1}{Z_{{\rm out},\,i}} \\ &\approx \left[Y'_{O1} \left(\frac{C'_\mu}{C'_\pi + C'_\mu} \right)^2 + g'_m \frac{C'_\mu}{C'_\pi + C'_\mu} \right] + j\omega \left(\frac{C'_\pi C'_\mu}{C'_\pi + C'_\mu} \right) \\ &\approx g + sC_P. \end{aligned} \tag{5}$$

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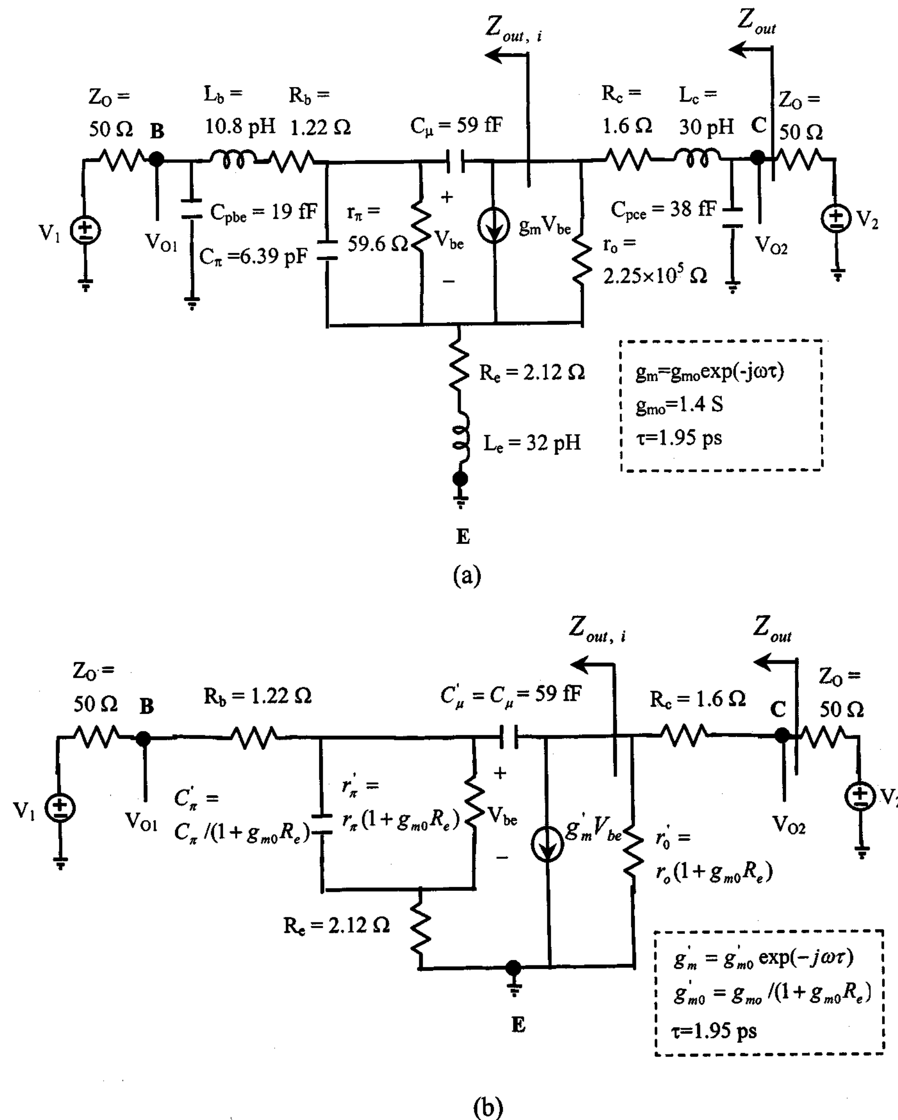

Fig. 1. Setup for the measurement of InGaP–GaAs HBTs S-parameters. (a) Complete circuit including small-signal π-model and extracted equivalent circuit parameters. (b) Simplified circuit with the local series–series feedback element (R_e) absorbed.

III. Results and Discussions

The HBTs studied in this paper was fabricated by 2-μm InGaP–GaAs HBT technology. There were two connected emitter fingers within the device and the width and length of each emitter mesa are 2 μm and 20 μm, respectively. The dc operation point was chosen at $V_{CE} = 3$ V and $I_B = 210\,\mu$A. The corresponding I_C equals 17.7 mA. The frequency dependent S-parameters were measured by HP8510C network analyzer with on-wafer SLOT calibration. The pad parasitic effect can be modeled by an equivalent C component parallel to a series LR circuit. This setup together with Cascade air coplanar ground–signal–ground probes can provide reliable RF measurement.

Fig. 2 shows that the measured S-parameters of our InGaP–GaAs HBTs range from 100 MHz to 20 GHz. Note that the kink phenomenon appears at about 7.5 GHz, as pointed in Fig. 2. The S-parameters generated by the small-signal hybrid π-model were also shown in Fig. 2. Note that the model data are almost identical with the experimental data and the kink phenomenon also appears at about 7.5 GHz.

The asterisks shown in Fig. 3 was the calculated S_{22} data based on the simplified small-signal π-model shown in Fig. 1(b). The effect of

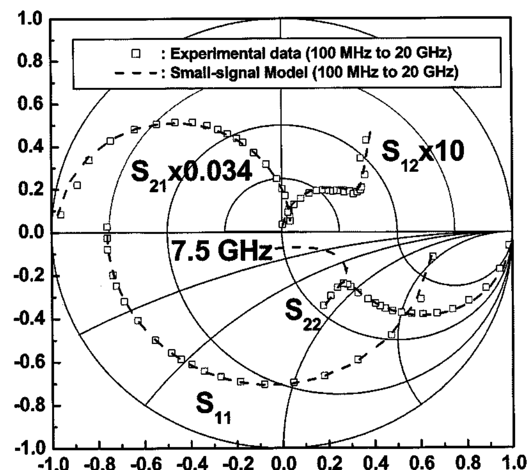

Fig. 2. Comparison of the experimental and calculated S-parameters of InGaP–GaAs HBTs. Dashed line (- - -): experimental data (from 100 MHz to 20 GHz), squares (□): calculated values (from 100 MHz to 20 GHz) based on the π-model shown in Fig. 1(a).

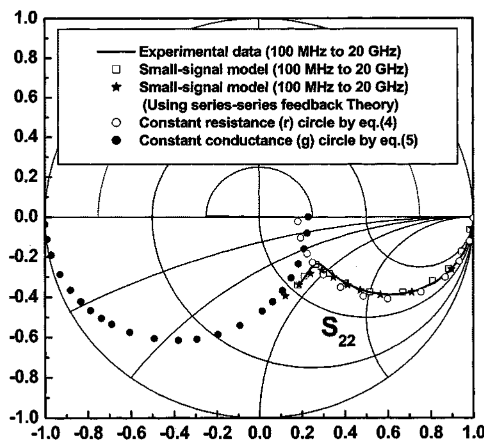

Fig. 3. Comparison of the experimental and calculated scattering parameters S_{22} of InGaP–GaAs HBTs. Solid line (—): Experimental data (from 100 MHz to 20 GHz). Squares (□). Calculated values (from 100 MHz to 20 GHz) based on the small-signal π-model shown in Fig. 1(a). Stars (★): calculated values (from 100 MHz to 20 GHz) based on the simplified small-signal π-model shown in Fig. 1(b). Hollow circles (○): calculated values (from 100 MHz to 20 GHz) based on (4). Solid circles (•): calculated values (from 100 MHz to 20 GHz) based on (5).

inductors in Fig. 1(a), which we neglected previously in Section II, can be easily included by replacing R_b, R_e, and R_c with $R_b + j\omega L_b$, $R_e + j\omega L_e$, and $R_c + j\omega L_c$, respectively. As can be seen, the asterisks fit the experimental data (solid line) of S_{22} well. The calculated frequency corresponding to the kink point is about 6.8 GHz, close to the experimental data 7.5 GHz. To further verify the dual-feedback circuit methodology, we have also applied the method mentioned in [3] to obtain the other three S-parameters, i.e., S_{11}, S_{21} and S_{12}, and compared them with our experimental data. Excellent agreement between theoretical values and experimental data was found (not shown here). What also shown in Fig. 3 was the calculated constant resistance (r) circle and constant conductance (g) circle according to (4) and (5). The calculated r and C_s is 70.6 Ω and 0.94 pF, respectively, for the series R–C circuit according to (4). In addition, the calculated $1/g$ and C_p is 80.0 Ω and 0.057 pF, respectively, for the parallel R–C circuit according to (5). It is clear that the output impedance follows the track of a constant r circle at low frequencies and then a constant g circle at high frequencies precisely. This is because the collector–emitter resistance r_o in InGaP–GaAs HBTs is usually very large (in this case, it is about 2.25 $\times$ 10^5 Ω, as shown in Fig. 1). This is very different from MOSFETs or GaAs FETs whose drain–source resistance R_{ds} is usually small (in the range of 10^1–10^3 Ω). Therefore, the S_{22} starts at a point near the open circuit point of the Smith chart, which makes the low frequency characteristics of S_{22} of HBTs follow a constant r circle.

IV. Conclusion

In this brief, the concept of dual-feedback circuit methodology was used to simplify the hybrid π model of InGaP–GaAs HBTs. The calculated S_{22} according to simplified circuit conform perfectly to the experimental data. It is also found that the derived output impedance of HBTs can be represented by a simple series R–C circuit at low frequencies and a simple parallel R–C circuit at high frequencies. It is this inherent ambivalent characteristic of the output impedance that results in the anomalous dip in scattering parameter S_{22} of InGaP–GaAs HBTs.

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A New 50-nm nMOSFET With Side-Gates for Virtual Source–Drain Extensions

Young Jin Choi, Byung Yong Choi, Kyung Rok Kim, Jong Duk Lee, and Byung-Gook Park

***Abstract*—We have proposed and fabricated a novel 50-nm nMOSFET with side-gates, which induce inversion layers for virtual source/drain extensions (SDE). The 50-nm nMOSFETs show excellent suppression of the short channel effect and reasonable current drivability [subthreshold swing of 86 mV/decade, drain-induced barrier lowering (DIBL) of 112 mV, and maximum transconductance (g_m) of 470 μS/μm at $V_D = 1.5$ V], resulting from the ultra-shallow virtual SDE junction. Since both the main gate and the side-gate give good cut-off characteristics, a possible advantage of this structure in the application to multi-input NAND gates was investigated.**

***Index Terms*—50-nm nMOSFET, NAND gate, side-gate, virtual source/drain extension (SDE).**

I. Introduction

In the era of sub-50-nm MOSFET, precise control of doping profile in the channel and source/drain region is needed [1]. Intensive searches have been done for a source/drain extension layer with ultra-shallow junction depth and reasonable resistance. However, it is difficult to implement ultrashallow junctions with a depth less than 10 nm by ion implantation or thermal diffusion. It has been reported that the electrically induced inversion layer is a candidate for ultra-shallow source/drain extensions and short-channel effect (SCE) could be suppressed by using this approach [2]–[4]. However, the reported works showed severe decrease of current level resulting from structural weakness. The structural weakness includes thick side-gate oxide, long side-gate length and gate-to-gate capacitance. In order to induce the inversion layer at a low voltage, a device structure with thin side-gate oxide is required. A long side-gate results in performance degradation due to increased series resistance, while too short side-gate provides little merit in SCE suppression. The overlapped

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The authors are with the Inter-University Semiconductor Research Center (ISRC) and School of Electrical Engineering, Seoul National University, Seoul 151-742, Korea (e-mail: nirvana@smdl.snu.ac.kr).

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