A Compact 2.4/5.2-GHz CMOS Dual-Band Low-Noise Amplifier

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***Abstract*—This letter presents a fully integrated 2.4/5.2-GHz dual-band low-noise amplifier (LNA) for WLAN applications. By switching the input transconductance and the output capacitance, the narrow-band gain and impedance matching are achieved at the 2.4-GHz and the 5.2-GHz frequency bands. Using a standard 0.18-μm CMOS process, a compact dual-band LNA with a chip size comparable to a single-band one is realized in the proposed topology for a minimum hardware cost. The fabricated circuit exhibits gains of 10.1 dB and 10.9 dB, and noise figures of 2.9 dB and 3.7 dB at the two frequency bands, respectively.**

***Index Terms*—Cascode amplifier, CMOS RF, dual-band, impedance matching, low-noise amplifier (LNA), multimode, source degeneration.**

I. Introduction

In THE past few years, wireless local-area networks (WLANs) have been deployed all over the world as office and home communication infrastructures. The increasing demand has motivated the introduction of new WLAN standards such as IEEE 802.11a and IEEE 802.11g to meet various application requirements. However, the diversification of the WLAN standards poses significant challenges in the design of the RF front-ends. It is desirable to have a system that can support multistandard operations while maintaining a competitive hardware cost.

One of the technical bottlenecks for a multistandard transceiver is the implementation of the low-noise amplifier (LNA) which can operate at two distinct frequency bands. Conventional dual-band architectures adopt two single-band LNAs in parallel [1]–[4], resulting in a high implementation cost due to the large chip area. Efforts have been made to realize a compact dual-band LNA by switched capacitors [5], [6], switched inductors [7], [8], and concurrent dual-band technique [9], [10]. However, most of the techniques still require additional inductors and excess chip area to provide the dual-band operation. In this letter, a novel circuit topology for the 2.4/5.2-GHz dual-band LNA is presented in a standard 0.18-μm CMOS process. By employing the proposed matching technique, the required LNA performance can be achieved at different frequency bands with a minimum hardware cost.

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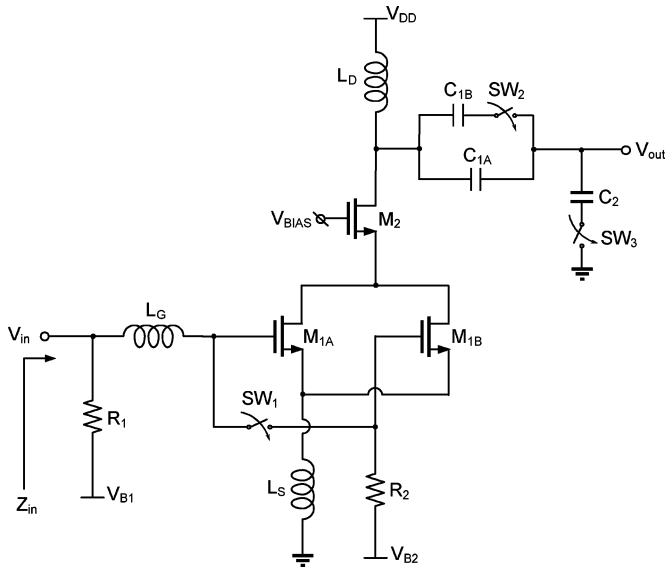

Fig. 1. Complete schematic of the proposed dual-band LNA.

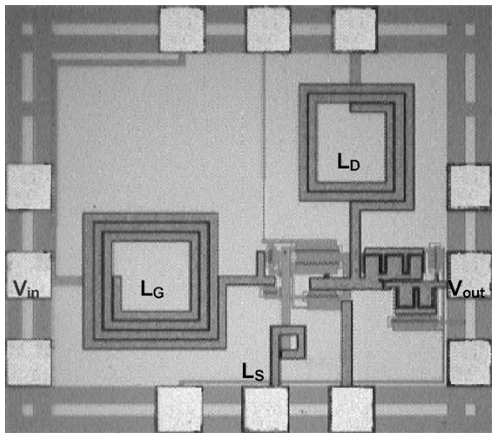

Fig. 2. Micrograph of the fabricated dual-band LNA.

Section II describes the design of the proposed dual-band LNA. Experimental results are shown in Section III and conclusions are given in Section IV.

II. LNA Topology and Circuit Design

In order to implement the 2.4/5.2-GHz dual-band LNA with a minimum chip area, a switching-type circuit topology with a novel matching technique is proposed. Fig. 1 shows the complete schematic of the dual-band LNA with all on-chip components. The LNA includes a source-degenerated cascode amplifier with switched transistors and capacitors for the band selection. The input stage is composed of L_S, L_G, M_{1A}, M_{1B}, R_1,

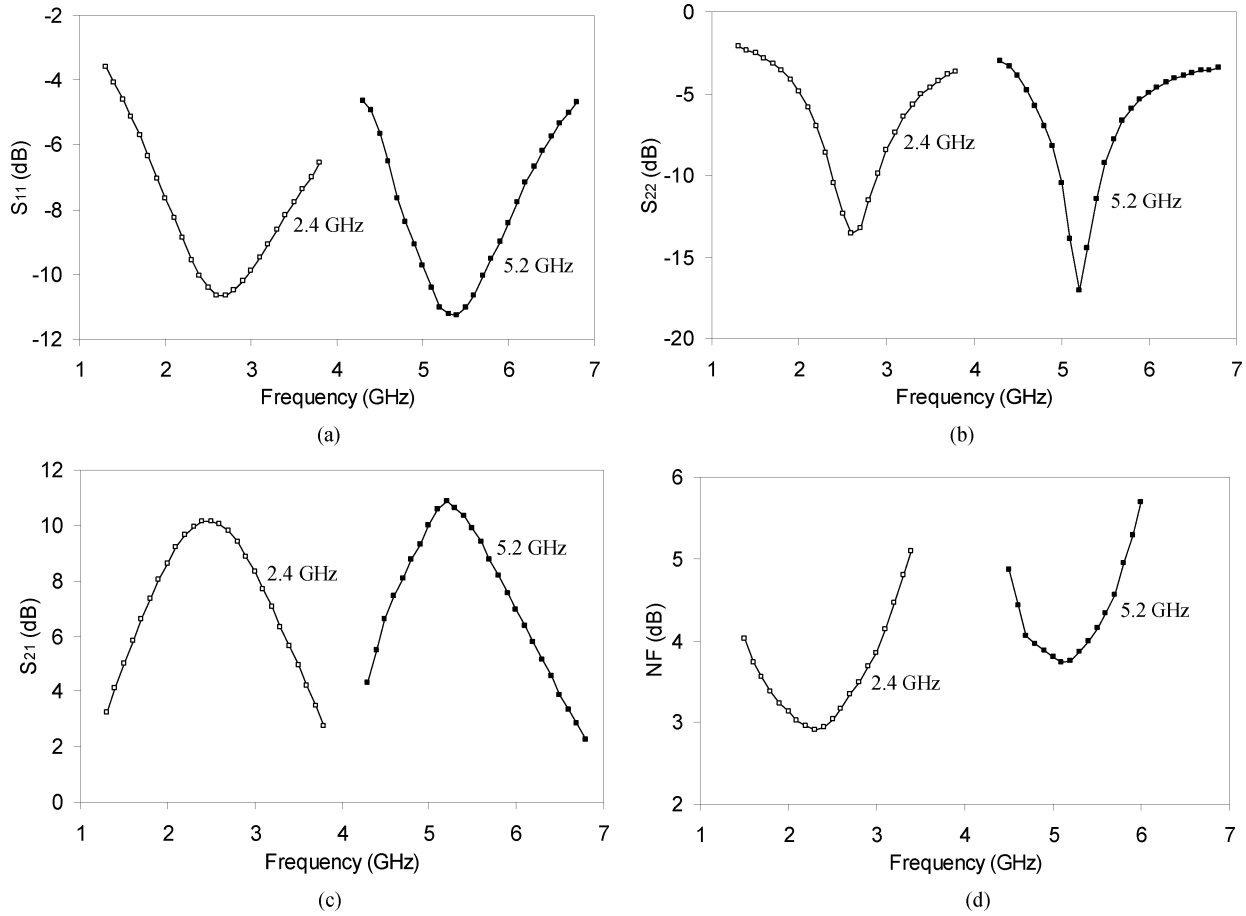

Fig. 3. Measurement results of the switching-type dual-band LNA. (a) S_{11}. (b) S_{22}. (c) S_{21}. (d) Noise figure.

R_2, and SW_1, and the output matching network consists of L_D, C_{1A}, C_{1B}, C_2, SW_2, and SW_3.

The circuit design starts with a single-band LNA at 5.2 GHz. When the LNA operates at the 5.2-GHz band, all of the switches SW_1-SW_3 are open. In this case, M_{1A} is used as the input transistor with a gate bias provided by V_{B1} through R_1. The input impedance of the LNA at the higher frequency band can be expressed as

$$Z_{in,H} \approx \frac{g_{m1A}L_S}{C_{gs1A}} + j\left[\omega_H(L_S+L_G) - \frac{1}{\omega_H C_{gs1A}}\right] \quad (1)$$

where g_{m1A} and C_{gs1A} are the transconductance and the gate capacitance of M_{1A}, respectively, and ω_H is the operating frequency at this band. The values of L_S, L_G, V_{B1}, and the aspect ratio $(W/L)_{1A}$ are determined to satisfy the required noise and impedance matching in a way similar to a conventional source-degenerated LNA design, while the output impedance is matched to 50 Ω by the shunt inductor L_D and the series capacitor C_{1A}.

When the LNA operates at the 2.4-GHz band, all the switches are closed. A parallel connection of the input transistors M_{1A} and M_{1B} is established in this mode. The resulting input impedance at the lower frequency band is

$$Z_{in,L} \approx \frac{(g_{m1A}+g_{m1B})L_S}{(C_{gs1A}+C_{gs1B})} + j\left[\omega_L(L_S+L_G) - \frac{1}{\omega_L(C_{gs1A}+C_{gs1B})}\right] \quad (2)$$

where g_{m1B} and C_{gs1B} are the transconductance and the gate capacitance of M_{1B}, respectively, and ω_L is the operating frequency at the lower band. Note that the gate bias voltage of M_{1A} and M_{1B} switches to $(R_2V_{B1}+R_1V_{B2})/(R_1+R_2)$ through the voltage divider R_1 and R_2. The transconductance g_{m1A} in (2) can be a design parameter independent of the one in (1), providing one more degree of freedom to meet the dual-band matching conditions. As a result, the input matching can be achieved at 2.4-GHz by switching the finger number and the gate voltage of the input transistor without additional on-chip inductors. In consideration of the required chip area, a switched capacitor matching network is adopted at the output. When operating at the lower frequency band, capacitors C_{1B} and C_2 are included in the matching network by the switches SW_2-SW_3 to provide a 50-Ω output impedance.

In the dual-band LNA design, the switches are realized by NMOS transistors. Since the MOS switches exhibit nonideal characteristics at both on and off states, the influence of the switches on the circuit performance should be carefully investigated. When a MOS switch is on, it is typically modeled as a finite on-resistance between the source and the drain. In general, the resistance tends to degrade the quality factor of the resonators, resulting in a higher noise figure and a lower amplifier gain. The on-resistance can be minimized by increasing the finger numbers of the switches. However, the excess parasitic capacitance associated with the MOS switches imposes a limitation on the transistor sizes. In this design, the MOS switches

TABLE I
PERFORMANCE SUMMARY OF THE DUAL-BAND LNA

	Unit	This Work	
Technology	-	0.18-μm CMOS	
Frequency	GHz	2.4	5.2
Power Dissipation	mW	11.7	5.7
Supply Voltage	V	1.8	
S_{21}	dB	10.1	10.9
Noise Figure	dB	2.9	3.7
S_{11}	dB	-10.1	-11
S_{22}	dB	-10.5	-17
$P_{in\text{-}1dB}$	dBm	-7	-16
IIP3	dBm	4	-5

are optimized to minimize the performance degradation in amplifier gain and noise figure. The simulation results indicate a 1.5-dB decrease in gain and a 0.7-dB increase in noise figure due to the parasitics of the switches.

III. EXPERIMENTAL RESULTS

Using a standard 0.18-μm CMOS process, the fully integrated dual-band LNA has been designed and implemented for the 2.4/5.2-GHz frequency bands. The micrograph of the fabricated LNA is shown in Fig. 2. On-wafer probing was performed to characterize the S-parameters and the noise figure of the LNA at both frequency bands. Fig. 3 shows the measurement results.

When the LNA is operating at the 5.2-GHz band, all the on-chip switches are turned off by the controlled voltage. With a power consumption of 5.7 mW from a 1.8-V supply, the LNA has a 10.9-dB gain and a 3.7-dB noise figure while maintaining an input return loss of 11 dB and an output return loss of 17 dB. The $P_{\mathrm{in}-1\mathrm{dB}}$ and *IIP3* of the LNA are -16 dBm and -5 dBm, respectively.

The LNA operates at the 2.4-GHz band by turning on the on-chip switches SW_1-SW_3. In this mode, the LNA consumes a dc power of 11.7 mW. According to the measured results, the LNA has a gain of 10.1 dB and a noise figure of 2.9 dB while the input and output return losses are better than 10 dB at 2.4 GHz. The $P_{\mathrm{in}-1\mathrm{dB}}$ and *IIP3* of the LNA are -7 dBm and 4 dBm, respectively. The performance of the dual-band LNA is summarized in Table I.

IV. CONCLUSION

A novel circuit topology for dual-band LNA is presented in this letter. The input matching conditions are satisfied by switching the finger number and the bias voltage of the input transistor, while the output matching is achieved by a switched capacitor matching network. Using a standard 0.18-μm CMOS process, a 2.4/5.2-GHz dual-band LNA was designed and implemented. The fabricated circuit exhibits a 10.1-dB gain and a 2.9-dB noise figure at the 2.4-GHz band, and a 10.9-dB gain and a 3.7-dB noise figure at the 5.2-GHz band. With a negligible increase in chip area compared with a single-band design, the dual-band LNA provides a cost-competitive solution to WLAN applications.

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