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Transport Mechanisms in n-Type Porous Silicon Obtained by Photoelectrochemical Etching

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The electrical conduction properties of metal/porous silicon/n-Si/metal have been investigated using current-voltage (I-V) measurements. The characteristics for all devices show a rectifying behavior with ideality factor close to unity. A value of 0.79 eV for the barrier height is found to increase with rising temperature. A band model is proposed in order to explain the observed characteristics.

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Since Canham [1-3] demonstrated visible light photoluminescence (PL) from porous silicon (PS), much effort has been focused on the possibility of producing optoelectronic devices using this new material. Electroluminescence (EL) is also observed from Schottky diodes formed from PS under forward bias [4, 5]. The origin of light emission has been extensively studied [6, 7]. The EL spectrum is similar to the PL indicating that a common recombination mechanism is involved in both cases. Reported values [4, 8-10] for the EL quantum efficiency ($\eta \sim 10^{i\ 2}\% - 10^{i\ 6}\%$) are significantly lower than the PL quantum efficiency (up to 7%) [10, 11]. The reasons for the low EL quantum efficiency are not understood, but just by considering the different excitation process, they must be linked to the transport mechanism inside the porous silicon layer and, in particular, the case with which these mechanisms can inject carriers into the states which luminescence efficiently. In order to improve the efficiency, it is important to study the influence of recombination centers, surface states, and electrical contacts on the EL and PL. For this purpose, much attention is being paid to the studies of electric and photoelectric of PS-based structures. For most of the previous works, the rectification in I-V curves is interpreted in terms of the existence of a Schottky barrier between the metal and PS interface [12]. However, the rectification has also been attributed to the PS/p-Si junction by the recent works [13, 14]. In this paper, we report the results of dc measurement on PS/n-Si structures sandwiched between two metal electrodes. We suggest that the rectification in I-V characteristics is due to the junction between the PS and its n-type Si substrate. We believe that the metal/PS junction is not a Schottky barrier but forms a non-ideal Ohmic contact.

Porous Silicon samples were prepared by electrochemical anodization of (1,1,1) n-type silicon substrates in 1:1 solution of HF acid (40%) and ethanol at a current density of 60 mA/cm^2 for 10 min. A 100W tungsten lamp was used for illumination from 15 cm distance. Samples

were rinsed in flowing de-ionized water and blown dry by nitrogen gas immediately after chemical etching. Au or Al films were used to create an intimate backside contact. After etching, we put the PS into a vacuum chamber to deposit thin Au or Al films onto the PS surface to make electrical contacts. The metal spot was performed at a glancing angle between the metal beam and PS in order to prevent direct contact between the silicon and the metal. The active area S of the device is found to be 4-mm-diem. A Keithley 236 source-measuere unit was used to record the I(V) curve as reported previously [15, 16].

I(V) measurements were recorded on a number of samples of Au/PS/n-Si/Au structure at various temperatures. Fig. 1 shows a typical current-voltage I(V) characteristics at different temperatures. The characteristic curves show a rectifying behavior for all of the measurements. The I(V) curves were also performed on the samples fabricated under different anodization currents, and they show similar rectifying characteristics. The use of other metal as a top electrode has produced no major effects on the result. This observation is in keeping with the previously published data' [13, 14] with calcium, magnesium, and antimony as a top electrode material. It has been found that the current turns on at the same value irrespective of the metal used as the top electrode. The present results indicate the interface between metal and PS layer may not be responsible for rectification.

From Fig. 1, we can see that the reverse current does not appear to be saturating, but shows voltage dependence. This is the indication of carrier transport through a heterostructure. Generally, this type of nonlinear dependence of the current I on the applied bias voltage V at temperature T can be written in the form [17, 18]:

$$I = I_s e^{\frac{q(V_j IR_S)}{nkT}}(1 - e^{i\ \frac{q(V_j IR_S)}{kT}}), \tag{1}$$

where

$$I_s = SA^{\text{¤¤}}T^2 e^{i\ \frac{q\copyright b}{nkT}}, \tag{2}$$

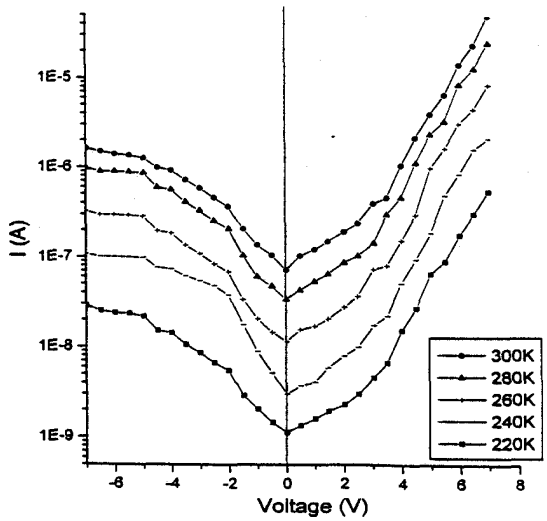

FIG. 1. I(V) curves of a Au/porous silicon/n-Si/Au structure at different temperatures.

where S is the diode area, $A^{\square\square}$ is the effective Richardson constant, T is the temperature in Kelvin, k is the Boltzman constant, q is the electronic charge, Φ_b is the barrier height, and R_s is the diode series resistance. The form of equation (1) includes the effects of thermionic-field emission and recombination of electron-hole pairs in the depletion region on transport mechanisms. Equation (1) is reduced to the law governing diffusion current due to thermionic emission for $n = 1$ and $Rs_{=}0$. Then, the factor $[(1 - \exp(-qV/kT)]$ is the most effective within the reverse bias range and the forward voltage regime up to 3 kT/q. The relationship is physically significant since the factors which are responsible for the non-ideal behavior under the forward bias are active under the reverse bias.

Fig. 2 shows a plot of $\ln[I/(1 - \exp(-qV/kT))]$ against V at 300 K (room temperature). In Fig. 2, we can obtain the value of n from the slope of linear portion of the graph. By substituting the value for n and I_s into Eq. (2), an approximate value of R_s is obtained. Fig. 3 shows the dependence of R_s on temperature T. It is found that series resistance R_s decreases with temperature T in an exponential fashion of the type: $R_s = R_0 \exp(\Delta E/kT)$. In Fig. 4, we can clearly see that the ideality factor increases linearly with the reciprocal of temperature. However, the result shows the departure from the ideality is not large.

Fig. 5 shows a plot of $\ln(I_s/T^2)$ against the reciprocal of the product of the ideality factor and temperature. It is find that the relationship is not linear which implies the barrier Φ_b is dependent on temperature. This behavior can be attributed to the fact that there exist two competing conduction processes in high and low temperature regimes. The transition between two conduction processes takes place gradually. The plot of $\ln(I_s/T^2)$ versus $T^{i\ 1}$ is also included in Fig. 5 for comparison. In high temperature regime, the two plots converge, and therefore, it appears that thermionic emission diffusion dominates the conduction process in high temperature. This observation is in agreement with the fact that the ideality factor n approaches to unity at high temperature. In the low temperature regime, the relatively small activation is believed to be associated with recombination currents. Furthermore, in Fig. 6 we can see that the barrier height Φ_b increases with rise in temperature. The room temperature value of Φ_b is about 0.79 eV. The temperature coefficient of the barrier height is about 0.3 meVK$^{i\ 1}$ obtained from the plot.

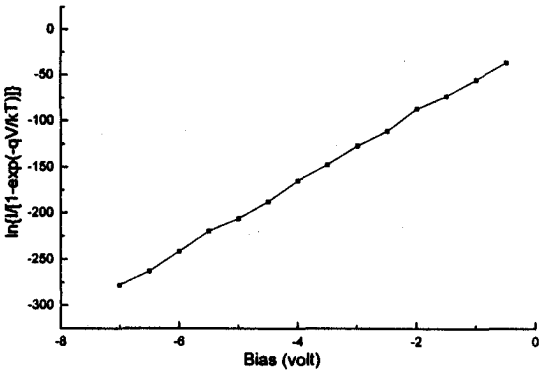

FIG. 2. Plots of $\ln\{I/[1 - \exp(-qV/kT)]\}$ against V for the same structure as in Fig. 1.

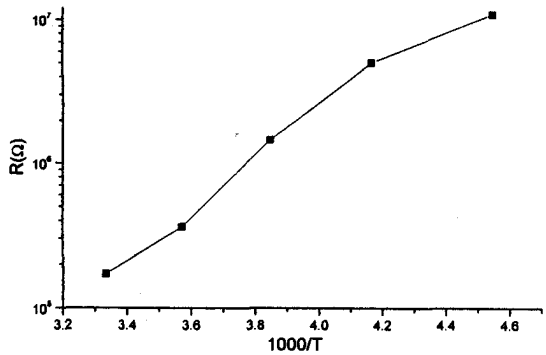

FIG. 3. A plot of series resistance R_s with respect to temperature T.

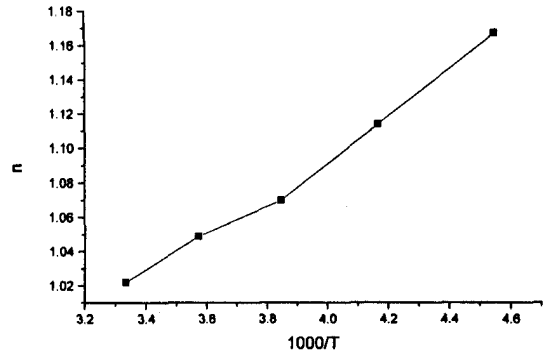

FIG. 4. A graph of ideality factor n with respect to temperature T.

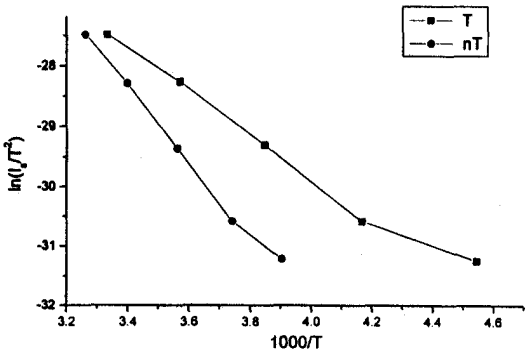

FIG. 5. Plots of $\ln(Is/T^2)$ against the reciprocal of nT and T.

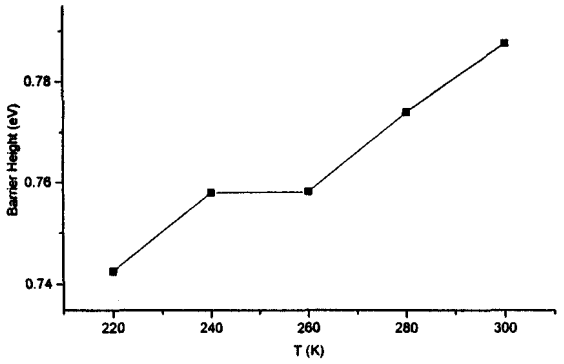

FIG. 6. The temperature dependence of equilibrium barrier height Φ_b.

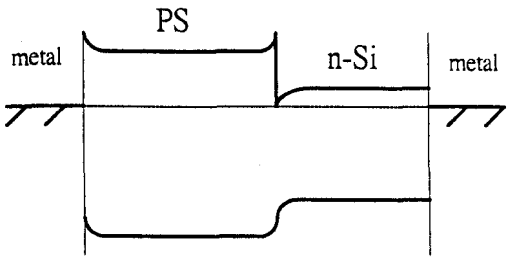

FIG. 7. A model of band structure for metal/PS/n-Si/metal devices.

Let us now provide a possible mechanism to interpret the conduction process in our devices. In a recent report [13], it was found that the surface of silicon is usually charged due to the presence of surface states either on the silicon surface or in the native oxide. Therefore, it is expected that the PS is depleted. The depth of depletion depends on carrier concentration and the surface charge of silicon, and it extends over a distance of a few tenth of micros into silicon. Depleted PS forms an Ohmic contact with metal top electrode. The nature of PS implies a very large effective surface area and has a large of dangling bonds. The dominance of a very high surface charge density in PS is expected to fix the Fermi level in a certain position near conduction band edge. Based on the above facts, we propose a band model as shown in Fig. 7 to account for the conduction in metal/PS/n-Si/metal devices. Because of the band gap difference between PS and Si substrate, a heterojunction is formed at the interface. The barrier between PS and n-Si that can cause an observed rectification controls the electron current through the PS/n-Si interface. The position of the Fermi level with respect to the conduction band in the PS layer is influenced by the thermal generation of minority carriers. The value of series resistance R_s is determined by the thermal

generation of minority carriers in PS layer. Thus, the experimental facts, such as the increase of barrier height Φ_b and the decrease of series resistance R_s with increase of temperature can be easily understood.

In summary, we report electrical conduction properties of metal/PS/n-Si/metal devices. According to the experimental results, the rectification of I(V) is found to be caused by the barrier between n-Si and PS heterojunction. The value of the ideality factor close to unity is evidence that the Si/PS junction properties are controlled by carrier diffusion in PS. The proposed band model can give a qualitative explanation for the characteristics of dc conduction in metal/PS/n-Si/metal structures.

Acknowledgment

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