Fabrication and Simulation of High-Power High-Speed $Ga_{0.51}In_{0.49}P$/GaAs Airbridge Gate MISFET's Grown by GSMBE

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Abstract - $Ga_{0.51}In_{0.49}P$/GaAs MISFET's, where a $Ga_{0.51}In_{0.49}P$ insulator layer was inserted between the gate metal and the channel layer, were compared with MESFET's experimentally and theoretically in terms of dc and microwave performance. Devices' performance were evaluated by varying the thickness of the insulating layer. Wide and flat characteristics of g_m, f_t and f_{max} versus drain current (or gate voltage) together with a high maximum current density (above 610 mA/mm) were achieved for devices with insulator thicknesses (t) of 50 nm and 100 nm. Moreover, the maximum values of f_t's and f_{max}'s for a 1 μm gate length device both occurred when t was between 50 nm and 100 nm. We also observed that parasitic capacitances and gate leakage currents were minimized by using the airbridge gate structure, and thus high frequency and breakdown characteristics were greatly improved. These results demonstrate that $Ga_{0.51}In_{0.49}P$/GaAs airbridge gate MISFET's with insulator thickness between 50 nm and 100 nm were very suitable for microwave high power device applications.

I. INTRODUCTION

An electronic device with high-linearity, high-power and high-speed performance is very important for microwave power applications. A device with good linear characteristics can reduce the intermodulation of high frequency signals, and therefore the distortion of signals at high power level operation is suppressed. It has been demonstrated that if a low-doped or an undoped layer is inserted between the gate metal and the active channel of a MESFET structure, the linearity, current drivability and breakdown voltage characteristics are greatly improved [1]. Even though the transconductance is lower than that of the conventional MESFET's, yet the reduced gate terminal capacitance C_g (i.e., gate-source capacitance C_{gs} plus gate-drain capacitance C_{gd}) makes the ratio, g_m/C_g, higher [2], and hence the high frequency performance is also improved.

There are several advantages by using the $Ga_{0.51}In_{0.49}P$/GaAs material system compared with the AlGaAs/GaAs system [3]. Therefore, we would like to study the performance of the metal-undoped $Ga_{0.51}In_{0.49}P$-n GaAs MISFET's with different insulator thickness t and compare them with similar MESFET's (t = 0 nm). The undoped $Ga_{0.51}In_{0.49}P$ can also be used as the airbridge for the gate metal to run over it between the active region and gate pad. This feature not only can reduce the gate leakage current but also decrease parasitic gate-source and gate-drain capacitances and therefore enhance devices' breakdown voltages and speeds.

II. CRYSTAL GROWTH AND DEVICE TECHNOLOGY

The heterostructures were grown by gas source molecular beam epitaxy (GSMBE) [4]. Schematic diagram of the cross section of MISFET's (t = 50 nm and 100nm) and MESFET's (t = 0 nm) is shown in Fig. 1. Conventional optical lithography and mesa type wet etching technique were used to fabricate the $Ga_{0.51}In_{0.49}P$/GaAs traditional gate MISFET's and MESFET's [4]. The separation between source and drain contacts was 4 μm. The gate length was 1 μm. Note that for traditional gate, the gate feeder, from the gate pad to the gate upon the active channel was lying on top of mesa edge. As for $Ga_{0.51}In_{0.49}P$/GaAs airbridge gate MISFET's, an additional step was needed for the formation of the $Ga_{0.51}In_{0.49}P$ airbridge, which was fabricated by selectively etching the GaAs. layer underneath the $Ga_{0.51}In_{0.49}P$. This means that the gate feeder, instead of contacting on the surface of the mesa edge, was lying on top of the $Ga_{0.51}In_{0.49}P$ airbridge between the active mesa region and gate pad. Hence, the gate metal feeder can be protected by photoresist and $Ga_{0.51}In_{0.49}P$ during the formation of the $Ga_{0.51}In_{0.49}P$ airbridge. This is one advantage compared with the method reported in [5]. It was also found that the $Ga_{0.51}In_{0.49}P$ airbridge structure was very robust for practical use even after shaking. A finished airbridge gate MISFET is shown in Fig. 2.

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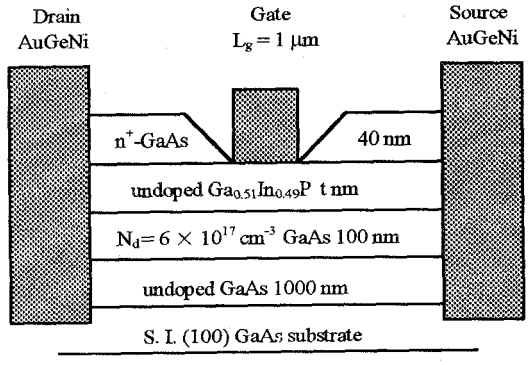

Fig. 1 Device cross section of $Ga_{0.51}In_{0.49}P$/GaAs MISFET's (t = 50nm,100 nm) and MESFET's (t=0 nm).

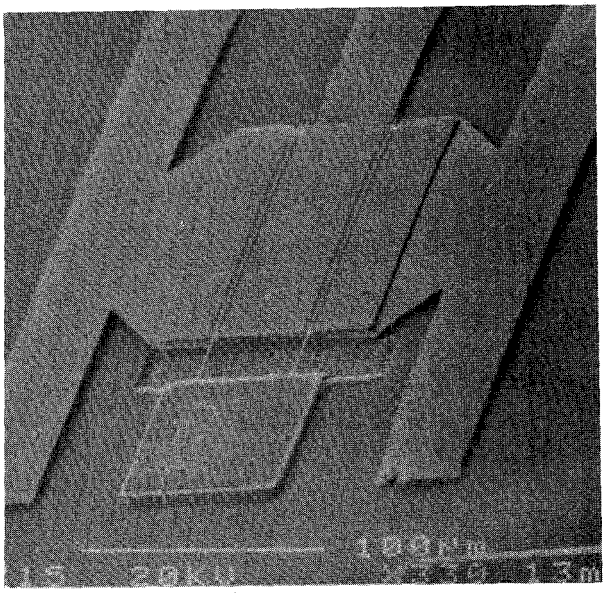

Fig. 2 The SEM picture of a finished $Ga_{0.51}In_{0.49}P$/ GaAs airbridge gate MISFET's

III. EXPERIMENTAL RESULTS AND DISCUSSIONS

A. DC Characteristics

The DC characteristics of $Ga_{0.51}In_{0.49}P$/GaAs MISFET's (t = 50 nm and 100 nm) and MESFET's (t = 0 nm) were measured with an HP4145B semiconductor parameter analyzer. Typical drain-source current versus drain-source voltage (I_{ds} - V_{ds}) characteristics of an airbridge gate MISFET's with insulator thickness t = 100 nm is shown in Fig. 3. High current drivability of 670 mA/mm and high drain-source voltage of 16 V were achieved with excellent pinched-off characteristics. The simulated I_{ds} - V_{ds} curves for this structure by MEDICI (2 - dimensional simulation) were also shown in Fig. 3. for comparison. As can be seen, the simulated curves fit the experimental curves very well. Fig. 4 shows the dependence of transconductance (g_m) on drain-source current (I_{ds}) of the airbridge gate MISFET's (t = 50 and 100 nm) and MESFET's (t = 0 nm) at V_{ds} = 4V. A distinct feature of MISFET's, compared to MESFET's, was the significant increase of maximum channel current $I_{ds,max}$. The characteristic curves of g_m v.s. I_{ds} for MISFET's extended not only to higher I_{ds} values but also exhibited flatter g_m characteristics with wider drain bias current conditions, namely, 390 mA/mm for t = 50 nm and 520 mA/mm for t = 100 nm in contrast with 115 mA/mm for t = 0 nm. The " width " of flat region was defined as the difference of two current densities corresponding to 10 % drop from the maximum g_m. The above results demonstrated that MIS-like structure indeed could achieve higher current drivability and better linearity. The gate-drain current (I_{gd}) versus gate-drain voltage (V_{gd}) characteristics of the airbridge gate MISFET's and MESFET's were conducted. It was found that the breakdown voltage (V_{gd}) increased systematically with increasing insulator thickness, i.e., 20 V for t = 0, 25 V for t = 50 nm and 29 V for t =100 nm. On the other hand, the prebreakdown I_{gd} current decreased systematically with increasing insulator thickness. These were attributed to the higher resistivity and breakdown field of the undoped wide-bandgap $Ga_{0.51}In_{0.49}P$.

B. Microwave Characteristics

Microwave on-wafer S-parameters for $Ga_{0.51}In_{0.49}P$/GaAs MISFET's (t = 50 nm and 100 nm) and MESFET's (t = 0 nm) with 1.0 μm-long gate were measured from 45 MHz to 40 GHz by an HP8510C network analyzer. Table I is a summary of the results of f_t's, f_{max}'s and extracted C_g (i.e., $C_{gs}+C_{gd}$) from measured S parameters for all devices (insulator thickness t = 0, 50 and 100 nm) biased at V_{ds} =4V, with V_{gs} tuned for a maximum S_{21}. From this table one can find that f_t's and f_{max}'s were greatly improved for all MISFET's and MESFET's with airbridge gate structure compared with those of traditional gate structure devices. The airbridge gate MISFET's with t = 50 nm exhibited f_t = 20.5 $\pm$ 0.3 GHz and f_{max} = 39 $\pm$ 0.5 GHz. These valus were roughly 45 % and 49 % higher than those (f_t = 14.1 $\pm$0.3 GHz and f_{max} = 26.1 $\pm$ 0.3 GHz) of the airbridge

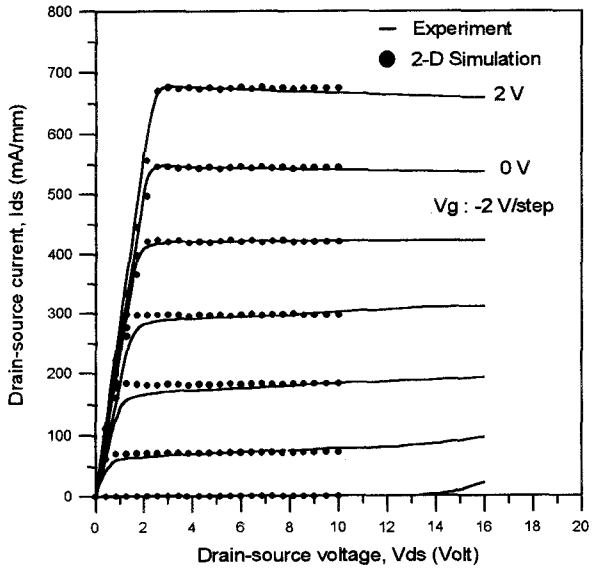

Fig. 3 The measured and simulated common-source current-voltage characteristics (I_{ds}-V_{ds}) of the $Ga_{0.51}In_{0.49}P$/ GaAs airbridge gate MISFET's with insulator thickness t = 100 nm.

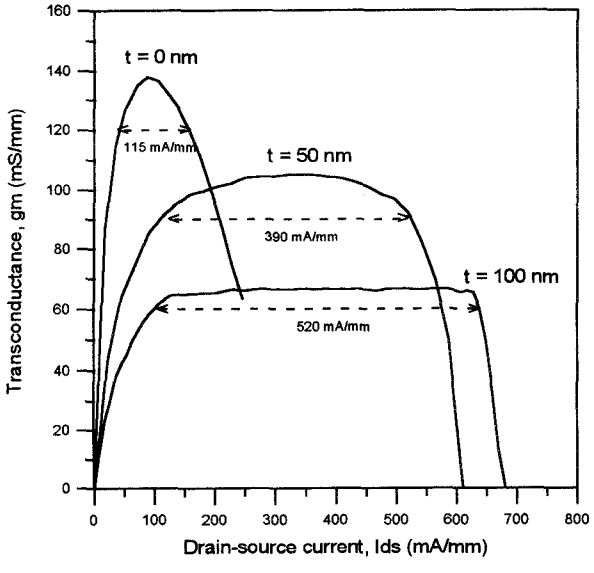

Fig. 4 The measured transconductance (g_m) versus drain-source current (I_{ds}) characteristics of $Ga_{0.51}In_{0.49}P$/GaAs airbridge gate MISFET's with insulator thickness t = 0 nm, 50 nm and 100 nm.

gate MESFET's (t = 0 nm) but slightly lower than those (f_t = 20.7±0.4 GHz, f_{max} = 40.1±0.5 GHz) of the airbridge gate MISFET's with t = 100 nm. However, the f_t's and f_{max}'s of traditional gate MISFET's with t = 50 nm were larger than that of traditional MISFET's with t = 100 nm. This could be explained by Fig. 5 in which the MISFET model of Ref. [2] was extended to include parasitic gate terminal capacitances C_g^p (i.e., interelectrode capacitance C_g^e plus geometric pad capacitance C_g^{pad}) in the total capacitance C_g. That is, $C_g = C_g^i + C_g^e + C_g^{pad}$, where C_g^i is the intrinsic gate terminal capacitance. As can be seen clearly from Fig. 5, at small t value (t < 50 nm), even though the transconduntance g_m decreased monotonically with increasing insulator thickness, yet the reduced gate terminal capacitance C_g made the ratio, g_m/C_g higher with increasing insulator thickness. This means that f_t's ($\sim \frac{g_m}{2\pi C_g}$) were improved with increasing insulator thickness for small t, as shown in Fig. 6. In the theory of Ref. [2] only C_g^i was considered, and hence they predicted that MISFET's have slightly higher or nearly the same values of f_t's and f_{max}'s with increasing t even if t is up to 300 nm. But, in real case, C_g^p is not a negligible constant and must be considered in the calculation. The C_g^i decreases with increasing t and hence f_t's and f_{max}'s first increase with increasing t due to the decrease of C_g^i but begin to decay when C_g^p is comparable to C_g^i. The simulated peak of f_t's of traditional gate structure appeared earlier (50 nm) than that (75 nm) of airbridge gate structure due to the larger C_g^p. For airbridge gate MISFET's, the parasitic geometric pad capacitance C_g^{pad} was negligible and hence its total gate capacitance C_g was approximately equal to $C_g^i + C_g^e$. This value, of course, was lower than that ($C_g = C_g^i + C_g^e + C_g^{pad}$) of traditional MISFET's because C_g^{pad} of traditional MISFET's was not negligible as shown in Fig. 5. Therefore, airbridge gate MISFET's exhibited higher f_t's than traditional gate MISFET's as previously seen in Fig. 6. In addition, the channel resistance R_i decreased systematically with increasing insulator thickness.

	t = 0 nm		t = 50 nm		t = 100 nm	
	traditional	airbridged	traditional	airbridged	traditional	airbridged
f_t(GHz)	12.9 ± 0.2	14.1 ± 0.3	17.6 ± 0.2	20.5 ± 0.3	16.2 ± 0.2	20.7 ± 0.4
f_{max}(GHz)	24.6 ± 0.3	26.1 ± 0.3	34.9 ± 0.4	39 ± 0.5	32.8 ± 0.3	40.1 ± 0.5
C_g (fF)	244.1 ± 2	223.9 ± 1.7	139.5 ± 1.4	119.4 ± 1.3	94.1 ± 1	73.9 ± 0.8

Table I Summary of RF characteristics of $Ga_{0.51}In_{0.49}P$/GaAs MISFET's and MESFET's

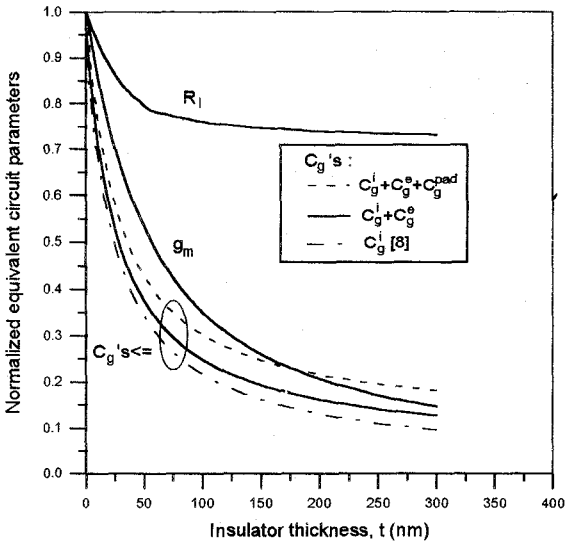

Fig.5 The simulated normalized depedance of the transconductance g_m, gate terminal capacitance C_g and channel resistance R_i versus insulator thickness t.

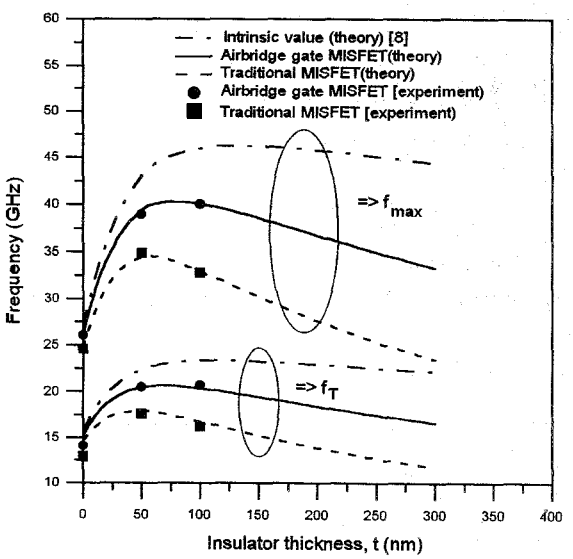

Fig.6 The simulated and measured cutoff frequency f_t's and maximum oscillation frequency f_{max}'s of airbridge gate and traditional MISFET's versus insulator thickness t.

Output conductance for MISFET's fabricated in our laboratory were nearly a constant and about 0.062 mS/mm. This implies that, compared with f_t's , f_{max}'s were much more improved by increasing insulator thickness at small t values, as can be seen in Fig. 6. The measured f_t's and f_{max}'s of airbridge gate and traditional gate MISFET's and MESFET's were very consistent with the simulated data and demonstrate the validity of the simulation.

IV. CONCLUSION

The experimental results were very consistent with the simulated results. And, these results showed that $Ga_{0.51}In_{0.49}P$/GaAs airbridge gate MISFET's with GaAs active layer 100 nm and $Ga_{0.51}In_{0.49}P$ insulator layer 50 nm to 100 nm were very suitable for microwave high power device applications

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