A 0.6-22-GHz Broadband CMOS Distributed Amplifier

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Abstract — **A CMOS distributed amplifier (DA) covering 0.6 to 22 GHz is presented in this paper. Cascode gain cells and m-derived matching sections are used to enhance the gain and bandwidth performance. The DA chip achieves measured gain of 7.3 ± 0.8 dB with chip area of 0.9 x 1.5 mm^2 including testing pads. The amplifier was fabricated in a standard 0.18-μm CMOS technology and demonstrated the highest frequency and bandwidth of operation among previously reported amplifiers using regular CMOS processes to date.**

I. INTRODUCTION

Broadband amplifiers find many applications such as instrumentation, electronic warfare and broadband optical communication. Distributed amplifiers (DAs) were widely used for realizing broadband amplifiers in GaAs hybrid and MMIC technologies [1-4]. Recently, DAs in CMOS process were also reported because of the advantages of low cost and integration ability with baseband circuits [5-10].

A DA using packaging and bond-wire inductors was presented in a 0.8-μm CMOS process with 5 ± 1.2-dB gain form 300 kHz to 3 GHz [5]. Using the 0.6-μm CMOS process, a fully integrated DA using on-chip planar spiral inductors achieves a measured pass-band gain of 6.1 dB with 5.5-GHz unity-gain bandwidth [6]. On the other hand, a fully differential DA achieves 5.5-dB pass-band gain and 8.5-GHz unity gain bandwidth [7]. Using a SOS n-MOSFET process to avoid the substrate loss, a DA with a bandwidth of 10 GHz and 5-dB gain was demonstrated in a 0.5-μm SOS NMOS process [8]. For DAs using 0.18-μm CMOS process, a three stage DA designed with coplanar strip lines demonstrated a low frequency gain of 5 dB, sloping down to 1 dB at 15 GHz [9], and two DAs using high impedance coplanar waveguides as inductive elements demonstrated 8 and 10-dB gain up to 10 GHz, respectively [10]. The operating frequencies of the previously published DAs are all below than 10 GHz.

In this paper, we reported the first 0.6-22-GHz broadband CMOS DA using a standard 0.18-μm

Process	Bandwidth (GHz)	Gain (dB)	Chip Area (mm^2)	NF (dB)	Unit Gain Freq. (GHz)	S11 (dB)	S22 (dB)	V_{DD} (V)	P_{DC} (mW)	Chip Feature	
0.8mm CMOS	0.3 - 3	5 ± 1.2	0.72 x 0.32	5.1 - 7	4.7	< -6	< -9	3	54	Bondwire inductors	[5]
0.6mm CMOS	0.5 - 4	6.5 ± 1.2	1.4 x 0.8	5.3 - 8	5.5	< -7	< -10	3	83.4	Spiral inductors	[6]
0.6mm CMOS	0.5 - 7.5	5.5 ± 1.5	1.3 x 2.2	8.7 - 13	8.5	< -6	< -9.5	3	216	Fully differential, spiral inductors	[7]
0.5mm SOS MOS	2 - 10	5 ± 1	-	-	-	< -5	< -7	-	-	CPW	[8]
0.18mm CMOS	-	5	0.3 x 1.5	-	23	< -14	-	-	-	CPS	[9]
0.18mm CMOS	1 - 10	8 ± 1	1.8 x 1.3	-	-	-	-	-	-	Darlington CC., CPW	[10]
0.18mm CMOS	**0.6 - 22**	**7.3 ± 0.8**	**0.9 x 1.5**	**4.3 - 6.1**	**24**	**< -8**	**< -9**	**1.3**	**52**	**CC., sprial inductors**	**This work**

Table. 1. Recently reported performance of CMOS distributed amplifiers. SOS: Silicon-on-Sapphire. CPS: Coplanar strip lines. CC: Cascode topology.

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CMOS technology. With cascode gain cells and m-derived matching sections, this DA achieves measured results of 7.3 ± 0.8 dB gain and input/output return loss better than 8 dB from 0.6 to 22 GHz. Table 1 summarizes the recently reported performance of CMOS distributed amplifiers compared with this work. Our chip demonstrated the highest frequency and bandwidth of operation with good input and output return loss.

II. 0.18μm CMOS Technology

The DA chip was designed using a commercial 0.18-μm 1P6M CMOS process, which provides single poly layer for the gates of the MOS and six metal layers for inter-connection as shown in Fig. 1 [11]. The substrate conductivity is approximately 10 S/m. Using optimized CMOS topology and deep n-well, this technology provides a f_T of 60 GHz and f_{MAX} of 55 GHz at 10 mA, a f_T of 70 GHz and f_{MAX} of 58 GHz at maximum-transconductance bias, and a minimum noise figure of 1.5 dB without ground-shielded signal pad. High-Q inductors can be formed using the top AlCu metallization layer of 2-μm thickness without added mask. A MIM capacitor of 1fF/mm^2 has been developed using oxide inter-metal dielectric. Two types of polysilicon resistors, with several Ω/□ and kΩ/□, are provided by choosing the individual dose of ion-implantation separately form the gate electrode doping process.

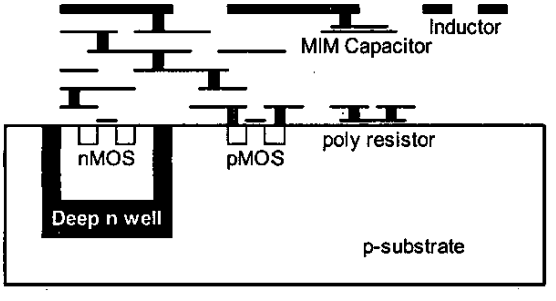

Fig. 1. The cross-section of the commercial 0.18-μm 1P6M CMOS process

III. Cascode Configuration

The cascode configuration, known for its high maximum available gain, wide bandwidth, improved input-output isolation, and variable gain control capability, have been utilized in may applications such as mixers, frequency multipliers and distributed amplifiers.

The maximum available gain of the FET device is strongly affected by the feedback capacitance and output conductance [12]. FETs in cascode configuration show a reduction of feedback capacitance and output conductance compared to standard FETs, so the power gain of a cascode pair is considerably higher than that of a common-source FETs. Fig. 2 compares the maximum available gain and maximum stable gain of cascode and common-source stages for the NMOSs with a total gate-width of 160 μm, based on the S-parameters of a common-source NMOS from 1 to 30 GHz.

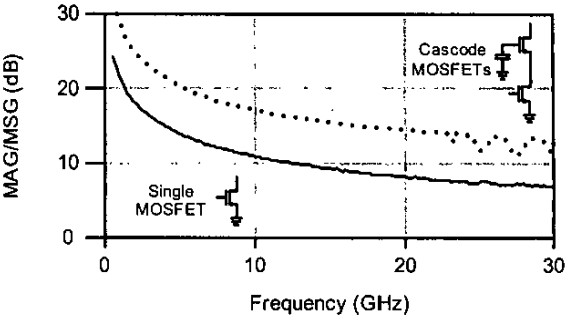

Fig. 2. Maximum available gain of a single transistor and cascode-connected transistors.

Conventional cascode FETs suffer from a large feedback capacitance, the drain-source capacitance of the common-gate transistor. This makes it tend to be unstable and thus more difficult to use in an amplifier circuit than a common-source FET. Since the stability is an important issue in an amplifier design, a small damping resister R_{gx} is usually added in the gate of common-gate transistor to improve the amplifier stability.

IV. Circuit Design and Fabrication

DAs are broadband circuits whose gain-bandwidth product substantially exceeds the transistor unit-gain frequency f_T, because the input and output capacitances of the active devices are absorbed in the distributed structures. A conventional DA consists of

an input and an output transmission lines coupled by the transconducatnces of the MOSFETs. The transmission lines are formed by using lumped inductors as shown and are referred to as the gate and drain lines. The gate line is periodically loaded by the MOSFET gate-source capacitance and is terminated in its characteristic impedance at the end. As the RF signal travels on the gate line, each transistor is exited by the traveling voltage wave and transfers the signal to the drain line through its transconductance. If the phase velocities on the gate line and drain line are equal, then the signals on the drain line add in the forward direction as they arrive at the output. The out-of-phase wave traveling in the reverse direction will be absorbed by the drain-line termination.

The proposed CMOS DA was designed using cascode gain cells and m-derived matching sections, as shown in Fig. 3. The models of the capacitors and resistors were provided by the foundry. The S-parameters of the inductors were simulated by the EM simulator, Sonnet 6.0 [13]. After layout optimization, the inductor gives the peak-Q of 12 at 1.9 GHz and 10 at 2.4 GHz for inductance of 1.5 nH and 4.1nH respectively. The MIM capacitor gives Q of 100 and 40 at 2.4 GHz and 5.3 GHz respectively at 1.1 pF. The cascode devices employ a 10-Ω damping resistor. A die micrograph is shown in Fig. 4. The chip size is approximately 0.9 x 1.5 mm^2 including testing pads.

V. Measurement Results

The CMOS DA was tested via on-wafer probing. Figs. 5 and 6 show the measured S-parameters and noise figure. The worst-case of the input return loss has a value of 8 dB at 4 GHz, and is 10 dB or better from 0.6 to 22 GHz. The worst-case of the output return loss has a value of 9 dB at 12 GHz and remains better than 10 dB over most of the bandwidth. The reverse isolation is 20 dB or better over the entire bandwidth as well. The measured results agree with the simulated results very well. The noise figure is between 4.3 dB and 6.1 dB over 0.6 to 18 GHz. The circuit is not optimized for noise performance, but the noise figure of the circuit is still comparable with other previously published CMOS DAs.

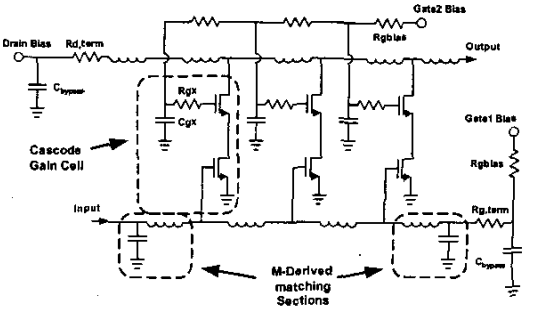

Fig. 3. Schematic circuit diagram of the cascode CMOS DA.

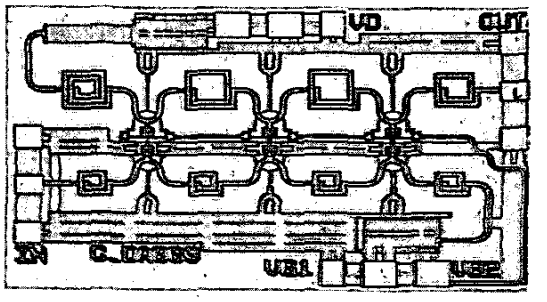

Fig. 4. Microphotograph of the CMOS DA.

VI. Conclusion

A fully integrated DA has been designed, fabricated and tested. This CMOS DA demonstrated 8-dB gain and 0.6-22-GHz bandwidth, which is the highest frequency and widest bandwidth of operation reported to date for broadband CMOS amplifiers. Since this DA was fabricated using a commercial 0.18-μm CMOS technology, it can be easily integrated with other front-end circuits to build CMOS transceivers without requiring any post-processing steps.

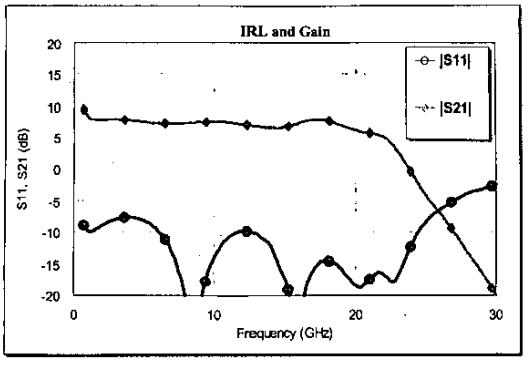

Fig. 5. Measured power gain S_{21} and input return loss S_{11}

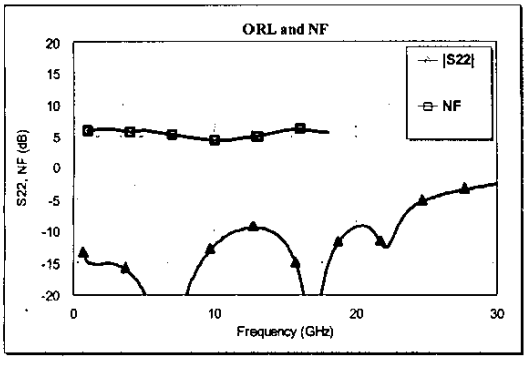

Fig. 6. Measured noise figure NF and output return loss S_{22}

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