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A fast *in situ* approach to estimating wafer warpage profile during thermal processing in microlithography

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Abstract
Wafer warpage can affect device performance, reliability and linewidth control in various processing steps in microelectronics manufacturing. Early detection will minimize cost and processing time. We have previously demonstrated an on-line approach for detecting wafer warpage and the profile of the warped wafer. The proposed approach demonstrates that the profile of the wafer can be computed during thermal processing steps in the lithography sequence. However, the approach is computationally intensive and information is made available at the end of the thermal processing step. Any attempts at real-time correction of the wafer temperature are thus not possible. In this paper, we proposed an *in situ* approach to detect wafer warpage and its profile midway through the thermal process. Based on first principles thermal modelling, we are able to detect and estimate the profile of a warped wafer from available temperature measurements. The proposed approach can be implemented on conventional thermal processing systems. Experimental results demonstrate the feasibility and repeatability of the approach. A 75% improvement in computational time is achieved with the proposed approach.

Keywords: *in situ* estimation, semiconductor manufacturing, fault detection, photoresist processing

(Some figures in this article are in colour only in the electronic version)

1. Introduction

Warped wafers are commonly found in microelectronics processing. Wafer warpages of up to 260 μm are observed [1] in silicon thinning and stress relief. Gettering and dislocation density in silicon wafers also affect wafer warpages; Kishino *et al* [2] reported a warpage range from 40 to 120 μm for a change of 1000 cm^{-3} in dislocation density. Fukui and Kurita [3] reported that warpage of up to 60 μm is induced during the processing of InP wafers. Warpage can also affect device performance, reliability and linewidth or critical dimension (CD) control in various microlithographic patterning steps. Warped wafers also result in different processing conditions in other processing steps such as rapid thermal processing [4]. Current techniques for measuring wafer warpage include capacitive measurement probe [5], shadow moiré technique [6] and pneumatic electro-mechanical technique [7]. These are mainly off-line methods where the wafer has to be removed from the processing equipment and placed in the metrology tool resulting in increased processing steps, time and cost.

In this work, we present an *in situ* approach to detect and estimate the profile of warped wafers during the lithography process in microelectronics processing. Figure 1 shows a typical lithography sequence [4]. When a wafer at room temperature is placed on the bake plate, the temperature of the bake plate drops at first but recovers gradually because

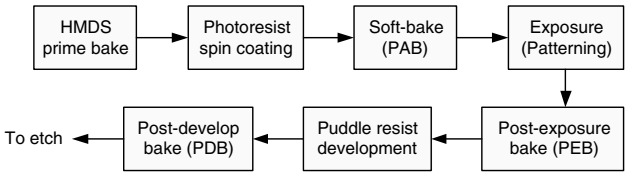

Figure 1. Typical steps in the microlithography sequence.

of closed-loop control. Different air-gap sizes will result in different temperature drops in the bake plate due to the difference in the air-gap/thermal resistance between the substrates and the bake plate. Warped wafers will affect the various baking steps in the lithography sequence [8]. In lithography, any drifts and variations in the process variables such as exposure doses, temperature, resist thickness, developer concentration, etc will affect the final CD. Among the process parameters, temperature is one of the most significant process parameters that can affect the CD. Warpage can result in a non-uniform temperature distribution across the wafer. For every degree variation in wafer temperature uniformity during the baking process, CD can vary by as much as 20 nm [9]. A 9% variation in CD per 1 °C variation in temperature has been reported for a deep ultraviolet (DUV) resist [10]. Temperature uniformity control is thus an important issue in photoresist processing with stringent specifications [11]. For some critical bake processes such as post-exposure bake (PEB), temperature uniformity as stringent as ± 0.1 °C is required. A number of recent investigations also showed the importance of proper bake-plate operation on linewidth or CD control [8, 12–16].

We have previously demonstrated that by monitoring the temperature drop of a conventional single-zone bake plate during the thermal processing steps in microlithography, we are able to detect wafer warpage fault [17]. We also showed that extension to a multi-zone system is possible with advanced signal processing techniques [18]. However, the method in [18] can only provide information on the warpage at the end of the bake process, as such any active correction of wafer temperature in real time is not possible. In this paper, we extend the approach in [17] to a multi-zone system for *in situ* estimation of the profile of the warped wafer. It can be shown that the maximum dropped point of the plate temperature at each zone is sufficient to extract information on the warped wafer. We note that the proposed technique requires no extra processing steps and is an *in situ* approach. The proposed approach is also simple and fast for implementation compared to our previous method [18].

This paper is organized as follows. In section 2, a detailed thermal model is presented for estimating the wafer warpage profile. Explicit solution of the bake-plate temperature profile will be provided. Experimental results are given in section 3 to demonstrate the proposed method. Finally, conclusions are given in section 4.

2. Modelling of the baking process

In this section, a brief description of the baking process is first provided. Next, the model for the baking process which will be used subsequently for the estimation of the wafer warpage profile is presented.

2.1. Baking of silicon wafers in lithography

Baking of semiconductor wafers is commonly performed by the placement of the substrate on a heated bake plate for a given period of time. The heated bake plate is usually of large thermal mass and held at a constant temperature by a feedback controller that adjusts the heater power in response to a temperature sensor embedded in the bake plate near the surface. The wafers are usually placed on proximity pins of the order of 100–200 μm to create an air gap so that the bake plate will not contaminate the wafers. As wafers can warp up to 100 μm from centre to edge, the percentage change in the air gap between the wafer and the bake plate can be substantial resulting in a significant variation in the bake-plate temperature [17].

When a wafer at room temperature is placed on the bake plate, the temperature of the bake plate drops to a minimum point and recovers gradually because of closed-loop control, as shown in figure 3. A flat wafer is used for experimental runs (a)–(c) and a warped wafer is used for experimental runs (d) and (e). Since the bake-plate temperature measurements are readily available, detection of wafer warpage is possible. We note that this is an *in situ* approach compared to conventional off-line methods discussed earlier. For a conventional thermal processing system, the proposed approach will provide the user with the information on the degree of warpage; information on the profile of the warpage is not possible due to the fact that the bake plate is single zone. To estimate the profile of the wafer, multiple-temperature measurement of the bake plate is required; this is only possible with a multi-zone bake plate with integrated temperature sensing within each zone. In this work, a programmable thermal processing module is developed to provide *in situ* estimation of the warped wafer profile. The multi-zone system is comprised of an array of heating zones that allow spatial control of temperature in non-symmetric configurations. A resistive heating element is embedded within each of the heating zones. Each heating zone is configured with its own temperature sensor and electronics for feedback control. Each heating zone is separated with a small air gap of approximately 50 mils. The fact that the zones are spatially disjoint ensures no direct thermal coupling between the zones, enhancing controllability. Its small thermal mass allows for fast dynamic manipulation of the temperature profile. Depending on the application, the number of zones of the bake plate can easily be configured. Figure 4 shows the multi-zone system.

The profile of the warped wafer can be estimated as follows. A detailed thermal model of the system is first developed. The relationship between the air gaps and the maximum temperature drops in the various zones can be obtained by solving the derived thermal equations. Next, the plate temperatures during the baking process are monitored and collected. The measured maximum temperature drops are then used to extract the various air gaps from which the profile of the wafer is estimated.

2.2. Thermal modelling

Spatial distribution of temperature and other quantities in a silicon wafer is most naturally expressed in a cylindrical

coordinate system. The assumed system consists of three sections: the bake plate, air gap and wafer. Expressed in terms of this cylindrical coordinate system, the partial differential equation of heat conduction in the wafer is

$$\frac{1}{r}\frac{\partial}{\partial r}\left(kr\frac{\partial T}{\partial r}\right)+\frac{1}{r^2}\frac{\partial}{\partial \phi}\left(k\frac{\partial T}{\partial \phi}\right)+\frac{\partial}{\partial z}\left(k\frac{\partial T}{\partial z}\right)=\rho C\frac{\partial T}{\partial t}, \tag{1}$$

where T is the temperature, k is the thermal conductivity, ρ is the mass density and C is the specific heat. The values of k and C are assumed to depend on temperature but not on time or position; if thermal expansion is neglected, the value of ρ can be fixed (note that the value of ρ is not fixed for air).

A commonly used numerical method of solution is the finite-difference method. The partial differential equation of heat conduction is approximated by a set of algebraic equations for temperature at a number of nodal points. The finite-difference form of the heat equations can be developed by replacing the partial derivatives of temperature in the heat conduction equation with their equivalent finite-difference form or by writing an energy balance for a differential volume element. The system is discretized spatially into N radial elements. The energy balance equations for the system are as follows:

$$C_{\mathrm{p}1}\dot{T}_{\mathrm{p}1}=-\frac{T_{\mathrm{p}1}-T_{\mathrm{p}2}}{R_{\mathrm{p}1}}-\frac{T_{\mathrm{p}1}-T_{\mathrm{w}1}}{R_{\mathrm{a}1}}+q_1, \tag{2}$$

$$C_{\mathrm{p}i}\dot{T}_{\mathrm{p}i}=\frac{T_{\mathrm{p}(i-1)}-T_{\mathrm{p}i}}{R_{\mathrm{p}(i-1)}}-\frac{T_{\mathrm{p}i}-T_{\mathrm{p}(i+1)}}{R_{\mathrm{p}i}}-\frac{T_{\mathrm{p}i}-T_{\mathrm{w}i}}{R_{\mathrm{a}i}}+q_i,\quad 2\leqslant i\leqslant N-1, \tag{3}$$

$$C_{\mathrm{p}N}\dot{T}_{\mathrm{p}N}=\frac{T_{\mathrm{p}(N-1)}-T_{\mathrm{p}N}}{R_{\mathrm{p}(N-1)}}-\frac{T_{\mathrm{p}N}}{R_{\mathrm{p}N}}-\frac{T_{\mathrm{p}N}-T_{\mathrm{w}N}}{R_{\mathrm{a}N}}+q_N, \tag{4}$$

$$C_{\mathrm{w}1}\dot{T}_{\mathrm{w}1}=\frac{T_{\mathrm{p}1}-T_{\mathrm{w}1}}{R_{\mathrm{a}1}}-\frac{T_{\mathrm{w}1}-T_{\mathrm{w}2}}{R_{\mathrm{w}1}}-\frac{T_{\mathrm{w}1}}{R_{\mathrm{w}z1}}, \tag{5}$$

$$C_{\mathrm{w}i}\dot{T}_{\mathrm{w}i}=\frac{T_{\mathrm{w}(i-1)}-T_{\mathrm{w}i}}{R_{\mathrm{w}(i-1)}}+\frac{T_{\mathrm{p}i}-T_{\mathrm{w}i}}{R_{\mathrm{a}i}}-\frac{T_{\mathrm{w}i}-T_{\mathrm{w}(i+1)}}{R_{\mathrm{w}i}}-\frac{T_{\mathrm{w}i}}{R_{\mathrm{w}zi}},\quad 2\leqslant i\leqslant N-1, \tag{6}$$

$$C_{\mathrm{w}N}\dot{T}_{\mathrm{w}N}=\frac{T_{\mathrm{w}(N-1)}-T_{\mathrm{w}N}}{R_{\mathrm{w}(N-1)}}+\frac{T_{\mathrm{p}N}-T_{\mathrm{w}N}}{R_{\mathrm{a}N}}-\frac{T_{\mathrm{w}N}}{R_{\mathrm{w}N}}-\frac{T_{\mathrm{w}N}}{R_{\mathrm{w}zN}}, \tag{7}$$

where $T_{\mathrm{w}i}$ is the ith wafer element temperature above ambient, $T_{\mathrm{p}i}$ is the ith bake-plate element temperature above ambient, $C_{\mathrm{p}i}$ is the thermal capacitance of the ith plate element, $C_{\mathrm{w}i}$ is the thermal capacitance of the ith wafer element, $R_{\mathrm{p}i}$ is the thermal conduction resistance between the ith and $(i+1)$th plate elements if $i<N$ or thermal convection loss of the ith plate element in the radial direction if $i=N$, $R_{\mathrm{w}i}$ is the thermal conduction resistance between the ith and $(i+1)$th wafer elements if $i<N$ or thermal convection loss of the ith wafer element in the radial direction if $i=N$, $R_{\mathrm{w}zi}$ is the thermal convection loss of the ith wafer element in the z-direction, $R_{\mathrm{a}i}$ is the thermal conduction resistance between the ith plate and ith wafer elements, and q_i is the power into the ith plate element.

The various thermal resistances and capacitances are given by

$$R_{\mathrm{p}i}=\frac{\ln\left(\frac{i+1/2}{i-1/2}\right)}{2\pi k_{\mathrm{a}}t_{\mathrm{p}}}\quad(\mathrm{K\,W^{-1}}),\quad 1\leqslant i\leqslant N-1,$$

$$R_{\mathrm{p}N}=\frac{1}{h(\pi Dt_{\mathrm{p}})}\quad(\mathrm{K\,W^{-1}}),$$

$$R_{\mathrm{w}i}=\frac{\ln\left(\frac{i+1/2}{i-1/2}\right)}{2\pi k_{\mathrm{w}}t_{\mathrm{w}}}\quad(\mathrm{K\,W^{-1}}),\quad 1\leqslant i\leqslant N-1,$$

$$R_{\mathrm{w}N}=\frac{1}{h(\pi Dt_{\mathrm{w}})}\quad(\mathrm{K\,W^{-1}}),$$

$$R_{\mathrm{w}zi}=\frac{1}{hA_{zi}}\quad(\mathrm{K\,W^{-1}}),$$

$$R_{\mathrm{a}i}=\frac{t_{\mathrm{a}}}{k_{\mathrm{a}}A_{zi}}\quad(\mathrm{K\,W^{-1}}),$$

$$C_{\mathrm{p}i}=\rho_{\mathrm{p}}c_{\mathrm{p}}(t_{\mathrm{p}}A_{zi})\quad(\mathrm{J\,K^{-1}}),\quad 1\leqslant i\leqslant N,$$

$$C_{\mathrm{w}i}=\rho_{\mathrm{w}}c_{\mathrm{w}}(t_{\mathrm{w}}A_{zi})\quad(\mathrm{J\,K^{-1}}),\quad 1\leqslant i\leqslant N,$$

$$A_{zi}=\pi\Delta r^2[i^2-(i-1)^2]\quad(\mathrm{m^2}),\quad 1\leqslant i\leqslant N,$$

where A_{zi} is the cross-sectional area of element i normal to the axial heat flow, t_{p} and t_{w} are the bake-plate thickness and wafer thickness, respectively, and t_{ai} is the air gap between the ith wafer and bake-plate elements. k_{a}, k_{p} and k_{w} are the thermal conductivities of air, bake plate and wafer, respectively. h is the convective heat transfer coefficient. ρ_{p} and ρ_{w} are the densities of the bake plate and wafer, respectively. c_{p} and c_{w} are the specific heat capacities of the bake plate and wafer, respectively. The width of each element is given by $\Delta_r=D/(2N)$.

Our objective here is to obtain an analytical expression for the minimum point of the bake-plate temperature profile. Without loss of generality, we will demonstrate our proposed approach on a two-zone system as shown in figure 2. For the two-zone system, equations (3)–(7) reduce to

$$C_{\mathrm{p}1}\dot{T}_{\mathrm{p}1}=-\frac{T_{\mathrm{p}1}-T_{\mathrm{p}2}}{R_{\mathrm{p}1}}-\frac{T_{\mathrm{p}1}-T_{\mathrm{w}1}}{R_{\mathrm{a}1}}+q_1, \tag{8}$$

$$C_{\mathrm{p}2}\dot{T}_{\mathrm{p}2}=\frac{T_{\mathrm{p}1}-T_{\mathrm{p}2}}{R_{\mathrm{p}1}}-\frac{T_{\mathrm{p}2}}{R_{\mathrm{p}2}}-\frac{T_{\mathrm{p}2}-T_{\mathrm{w}2}}{R_{\mathrm{a}2}}+q_2, \tag{9}$$

$$C_{\mathrm{w}1}\dot{T}_{\mathrm{w}1}=\frac{T_{\mathrm{p}1}-T_{\mathrm{w}1}}{R_{\mathrm{a}1}}-\frac{T_{\mathrm{w}1}-T_{\mathrm{w}2}}{R_{\mathrm{w}1}}-\frac{T_{\mathrm{w}1}}{R_{\mathrm{w}z1}}, \tag{10}$$

$$C_{\mathrm{w}2}\dot{T}_{\mathrm{w}2}=\frac{T_{\mathrm{w}1}-T_{\mathrm{w}2}}{R_{\mathrm{w}1}}+\frac{T_{\mathrm{p}2}-T_{\mathrm{w}2}}{R_{\mathrm{a}2}}-\frac{T_{\mathrm{w}2}}{R_{\mathrm{w}2}}-\frac{T_{\mathrm{w}2}}{R_{\mathrm{w}z2}}. \tag{11}$$

From equations (10) and (11), the relationships between the wafer and bake-plate steady-state temperatures, $T_{\mathrm{w}1}(\infty)$, $T_{\mathrm{w}2}(\infty)$, $T_{\mathrm{p}1}(\infty)$ and $T_{\mathrm{p}2}(\infty)$, are given as

$$T_{\mathrm{w}1}(\infty)=\frac{R_2}{R_{\mathrm{a}1}R}T_{\mathrm{p}1}(\infty)+\frac{1}{R_{\mathrm{w}1}R_{\mathrm{a}2}R}T_{\mathrm{p}2}(\infty), \tag{12}$$

$$T_{\mathrm{w}2}(\infty)=\frac{1}{R_{\mathrm{w}1}R_{\mathrm{a}1}R}T_{\mathrm{p}1}(\infty)+\frac{R_1}{R_{\mathrm{a}2}R}T_{\mathrm{p}2}(\infty), \tag{13}$$

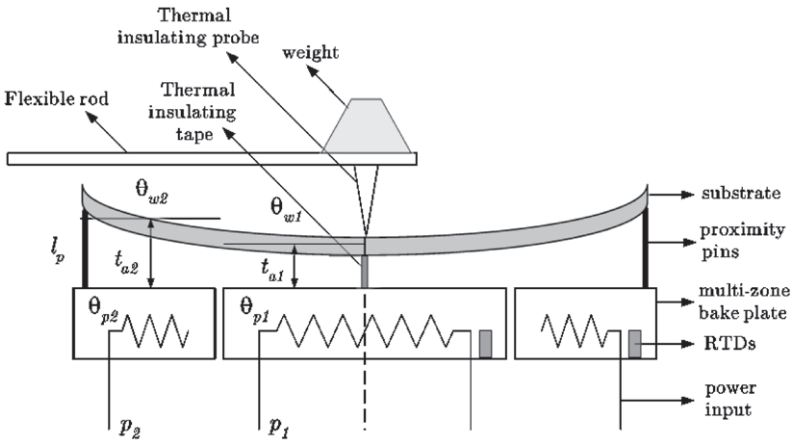

Figure 2. Schematic of warpage setup and thermal modelling of a two-zone thermal processing system.

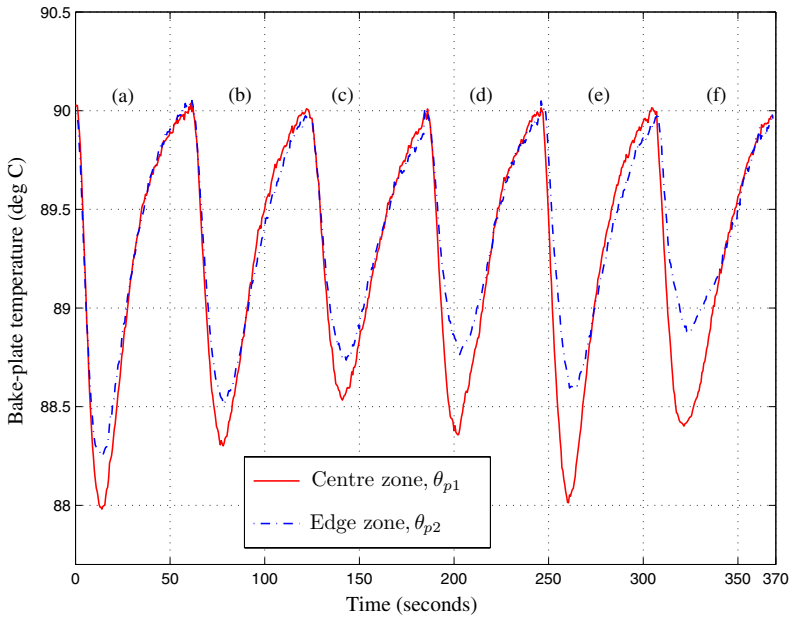

Figure 3. Results for six experimental runs to demonstrate that different air-gap sizes cause different magnitudes of bake-plate temperature drops before recovery for a two-zone baking system. Experimental runs (a)–(f) represent different experimental conditions outlined in section 3 and table 3.

where

$$R_1 = \frac{1}{R_{a1}} + \frac{1}{R_{w1}} + \frac{1}{R_{wz1}},$$
$$R_2 = \frac{1}{R_{w1}} + \frac{1}{R_{a2}} + \frac{1}{R_{w2}} + \frac{1}{R_{wz2}},$$
$$R = R_1 R_2 - \frac{1}{R_{w1}^2}.$$

Next, at the start of an experiment ($t = 0$), a wafer at ambient temperature ($T_{wi}(0) = 0$) is placed on the bake plate which is maintained at a particular steady-state temperature. Note in figure 3 that the bake-plate temperature drops before it recovers to its original temperature, i.e. $T_{pi}(0) = T_{pi}(\infty)$. To simplify our analysis, the following new variables are introduced:

$$\theta_{pi}(t) = T_{pi}(t) - T_{pi}(\infty),$$
$$\theta_{wi}(t) = T_{wi}(t) - T_{wi}(\infty),$$
$$u_i(t) = q_i(t) - q_i(\infty).$$

Equations (8)–(11) can now be expressed as

$$C_{p1}\dot{\theta}_{p1} = -\frac{\theta_{p1} - \theta_{p2}}{R_{p1}} - \frac{\theta_{p1} - \theta_{w1}}{R_{a1}} + u_1, \tag{14}$$

$$C_{p2}\dot{\theta}_{p2} = \frac{\theta_{p1} - \theta_{p2}}{R_{p1}} - \frac{\theta_{p2}}{R_{p2}} - \frac{\theta_{p2} - \theta_{w2}}{R_{a2}} + u_2, \tag{15}$$

$$C_{w1}\dot{\theta}_{w1} = \frac{\theta_{p1} - \theta_{w1}}{R_{a1}} - \frac{\theta_{w1} - \theta_{w2}}{R_{w1}} - \frac{\theta_{w1}}{R_{wz1}}, \tag{16}$$

$$C_{w2}\dot{\theta}_{w2} = \frac{\theta_{w1} - \theta_{w2}}{R_{w1}} + \frac{\theta_{p2} - \theta_{w2}}{R_{a2}} - \frac{\theta_{w2}}{R_{w2}} - \frac{\theta_{w2}}{R_{wz2}}. \tag{17}$$

Taking Laplace transformation of equations (14)–(17) (note that we have used $\Theta(s)$ to denote the Laplace transform of $\theta(t)$), we have

$$\Theta_{p1}(s)\left(sC_{p1}+\frac{1}{R_{p1}}+\frac{1}{R_{a1}}\right) = C_{p1}\theta_{p1}(0)+\frac{\Theta_{p2}(s)}{R_{p1}}+\frac{\Theta_{w1}(s)}{R_{a1}}+u_1(s), \tag{18}$$

$$\Theta_{p2}(s)\left(sC_{p2}+\frac{1}{R_{p1}}+\frac{1}{R_{p2}}+\frac{1}{R_{a2}}\right) = C_{p2}\theta_{p2}(0)+\frac{\Theta_{p1}(s)}{R_{p1}}+\frac{\Theta_{w2}(s)}{R_{a2}}+u_2(s), \tag{19}$$

$$\Theta_{w1}(s)\left(sC_{w1}+\frac{1}{R_{w1}}+\frac{1}{R_{wz1}}+\frac{1}{R_{a1}}\right) = C_{w1}\theta_{w1}(0)+\frac{\Theta_{w2}(s)}{R_{w1}}+\frac{\Theta_{p1}(s)}{R_{a1}}, \tag{20}$$

$$\Theta_{w2}(s)\left(sC_{w2}+\frac{1}{R_{w1}}+\frac{1}{R_{w2}}+\frac{1}{R_{wz2}}+\frac{1}{R_{a2}}\right) = C_{w2}\theta_{w2}(0)+\frac{\Theta_{w1}(s)}{R_{w1}}+\frac{\Theta_{p2}(s)}{R_{a2}}, \tag{21}$$

where

$$\theta_{w1}(0) = T_{w1}(0)-\frac{R_2\frac{1}{R_{a1}}}{R}T_{p1}(\infty)-\frac{\frac{1}{R_{w1}}\frac{1}{R_{a2}}}{R}T_{p2}(\infty),$$

$$\theta_{w2}(0) = T_{w2}(0)-\frac{\frac{1}{R_{w1}}\frac{1}{R_{a1}}}{R}T_{p1}(\infty)-\frac{R_1\frac{1}{R_{a2}}}{R}T_{p2}(\infty),$$

$$\theta_{p1}(0)=\theta_{p2}(0)=0.$$

In this work, conventional proportional-integral (PI) controllers are used to control the two heater zones. The control efforts, u_1 and u_2 in equations (18) and (19), can be obtained from equations (A.3) and (A.4).

Next, solving equations (18)–(21) (detailed derivation is provided in the appendix), explicit expressions for the plate temperature in the respective zones are given by

$$\theta_{p1}(t) = \frac{1}{E_1}\theta_{w1}(0)\sum_{i=1}^{8}\left[\frac{G(-a_i)}{P_{ti}(-a_i)}\,e^{-a_i t}\right] + \frac{1}{E_1}\theta_{w2}(0)\sum_{i=1}^{8}\left[\frac{H(-a_i)}{P_{ti}(-a_i)}\,e^{-a_i t}\right], \tag{22}$$

$$\theta_{p2}(t) = \frac{1}{E_1}\theta_{w1}(0)\sum_{i=1}^{8}\left[\frac{I(-a_i)}{P_{ti}(-a_i)}\,e^{-a_i t}\right] + \frac{1}{E_1}\theta_{w2}(0)\sum_{i=1}^{8}\left[\frac{J(-a_i)}{P_{ti}(-a_i)}\,e^{-a_i t}\right]. \tag{23}$$

The bake-plate temperature in each zone dropped to a minimum temperature before recovering. These two minimum temperature points (or maximum temperature drop points) can be found by differentiating equations (22) and (23) and equating to zero. The average air gap between the wafer and the plate in each zone can then be obtained based on the maximum drop point of the plate temperature profile as illustrated in the next section.

3. Experimental results

The experimental setup follows that of Tay *et al* [18] and is shown in figure 2. A photograph of the experimental setup is shown in figure 4. In order to demonstrate the proposed approach, the warpage of the wafer was created mechanically as shown in figure 2. By mechanically pressing the centre of the wafer, a wafer of known warpage is created. The amount of displacement is determined via the thickness of the thermal insulating tape. A micrometre resolution gauge can also be used to verify this by positioning it on the top of the rod. The PI controller parameters for the centre and edge zones are given by $K_{C1} = 14.0$, $T_{I1} = 300$ and $K_{C2} = 45.0$, $T_{I2} = 300$, respectively. Resistive temperature detectors (RTDs) embedded in each zone of the bake plate were used for temperature measurement. The experiments were conducted at a set point of 90 °C with a sampling and control interval of 0.5 s. This temperature corresponds to a soft-bake condition for photoresist processing [19].

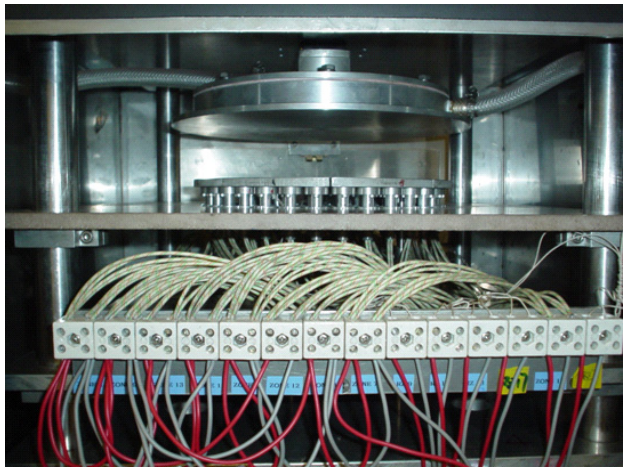

Figure 4. A programmable multi-zone thermal processing system.

Table 1. Thermophysical properties of materials.

Thermophysical properties	Values
Density of silicon	$\rho_w = 2330$ kg m^{-3}
Density of aluminium	$\rho_p = 2700$ kg m^{-3}
Specific heat capacity of silicon	$c_w = 0.75$ kJ kg^{-1} K^{-1}
Specific heat capacity of aluminium	$c_p = 0.917$ kJ kg^{-1} K^{-1}
Thermal conductivity of air	$k_a = 0.03$ W m^{-1} K^{-1}
Thermal conductivity of silicon	$k_w = 99$ W m^{-1} K^{-1}
Natural convection coefficient	$h = 3$ W m^{-2} K^{-1}
Thickness of wafer	$t_w = 750$ μm

3.1. System calibration

Most thermophysical properties are temperature dependent. However, for the temperature range of interest from 15 °C to 150 °C, it is reasonable to assume that they remain fairly constant and can be obtained from handbooks [20, 21] and are tabulated in table 1. The various thermal capacitances and resistances are computed and tabulated in table 2. To obtain a more accurate and realistic model, parameters that we do not have full knowledge of are estimated. For a given bake plate, the bake-plate element thermal capacitances (C_{p1} and C_{p2}) are expected to be fixed and hence can be determined *a priori*. Experimental run (a) in figure 3 was used to determine the plate element thermal capacitances, C_{p1} and C_{p2}, respectively.

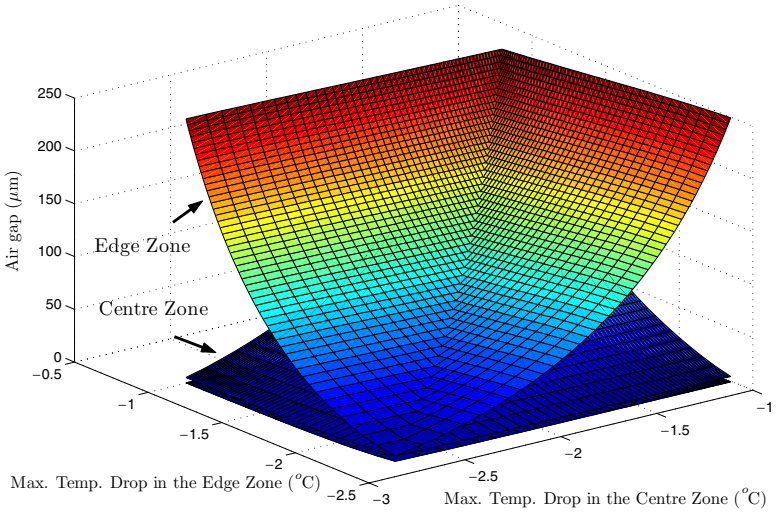

Figure 5. Maximum temperature drops versus air gaps (for a two-zone system).

Table 2. Thermal capacitances and resistances of the bake plate.

Thermal capacitances and resistances	Values
C_{w1}	0.0103 kJ K^{-1}
C_{w2}	0.0309 kJ K^{-1}
R_{wz1}	42.19 K W^{-1}
R_{wz2}	14.06 K W^{-1}
R_{w1}	2.355 K W^{-1}
R_{w2}	707.4 K W^{-1}
R_{p1}	544.7 K W^{-1}
R_{p2}	49.58 K W^{-1}

The experiment was conducted by dropping a flat wafer on the bake plate with a known air gap of $t_a = 55$ μm. Since the respective air gaps are known (i.e. t_{a1} and t_{a2}), the air-gap resistances R_{a1} and R_{a2} can be computed as

$$R_{a1} = \frac{t_{a1}}{k_a A_{z1}} = 0.2321 \text{ K W}^{-1},$$
$$R_{a2} = \frac{t_{a2}}{k_a A_{z2}} = 0.0774 \text{ K W}^{-1}.$$

From experimental run (a), the maximum temperature drops in the two zones are given by $\theta_{p1}(t) = -2.02$ and $\theta_{p2}(t) = -1.75$, respectively. Substituting the various variables into equations (22) and (23), and solving them numerically gives $C_{p1} = 0.208$ kJ K^{-1} and $C_{p2} = 0.738$ kJ K^{-1}.

3.2. Estimation of wafer warpage

Once the wafer, bake-plate and PI controller parameters are known, values of the average air gaps in the two zones, t_{a1} and t_{a2}, can be used to obtain R_{a1} and R_{a2} after which the model in equations (22) and (23) can be solved for the maximum drops in temperature. A plot of the air gaps, t_{a1} and t_{a2}, versus the maximum temperature drops in $\theta_{p1}(t)$ and $\theta_{p2}(t)$ is shown in figure 5.

Experimental runs (b) and (c) in figure 3 show the results when a flat wafer is dropped on the bake plate. The proximity pin heights, l_p, for runs (b) and (c) are 110 μm and 165 μm, respectively. The maximum temperature drops in $\theta_{p1}(t)$ and $\theta_{p2}(t)$ for the experiments and the corresponding average air gaps, t_{a1} and t_{a2}, read from the two surfaces in figure 5 are tabulated in table 3. A good measure of the warpage extent is to measure the deviation of the average air gap from the proximity pin height. δ_1 and δ_2 in experimental runs (b) and (c) are close to zero as expected since the wafer is flat.

Experimental runs (d) and (e) in figure 3 show the results when a wafer with centre-to-edge warpage of 110 μm is dropped on the bake plate with different proximity pin heights. The proximity pin heights, l_p, for runs (d) and (e) are 220 μm and 165 μm, respectively. The maximum temperature drops and the estimated air gaps for the two runs are also tabulated in table 3. δ_1 and δ_2 in experimental runs (d) and (e) are approximately the same. Based on the estimated δ_1 and δ_2 together with the proximity pin height, the profile of the wafer can be obtained by extrapolation as shown in figure 6 (based on experimental run (e)). An estimated warpage of 106 μm from centre-to-edge for the warped wafer is obtained. Experimental run (f) in figure 3 shows the results for the case of a wafer with a centre-to-edge warpage of 165 μm and a proximity pin height of 275 μm.

These two sets of experimental runs ((b), (c) and (d), (e)) demonstrate the feasibility of the approach in that different bake systems might have different proximity pin heights, however the degree of warpage should be the same for the same wafer. We expect accuracy to improve if the number of zones in the bake plate is increased. The repeatability of the approach is also demonstrated in figure 6. Each experimental run ((b)–(e)) is repeated five times, and deviations obtained are all within ± 10 μm of the actual profile.

In this work, we only use a single point (the maximum temperature drop point in each zone of the bake plate) for warpage estimation. It is faster for implementation compared to our previous method in which the complete temperature trajectory of the bake plate is used for warpage estimation. Once the model of maximum temperature drops versus air gaps in figure 5 is obtained, using functions from Matlab toolbox, it only takes about 0.02 s (tic.m, toc.m) to obtain the

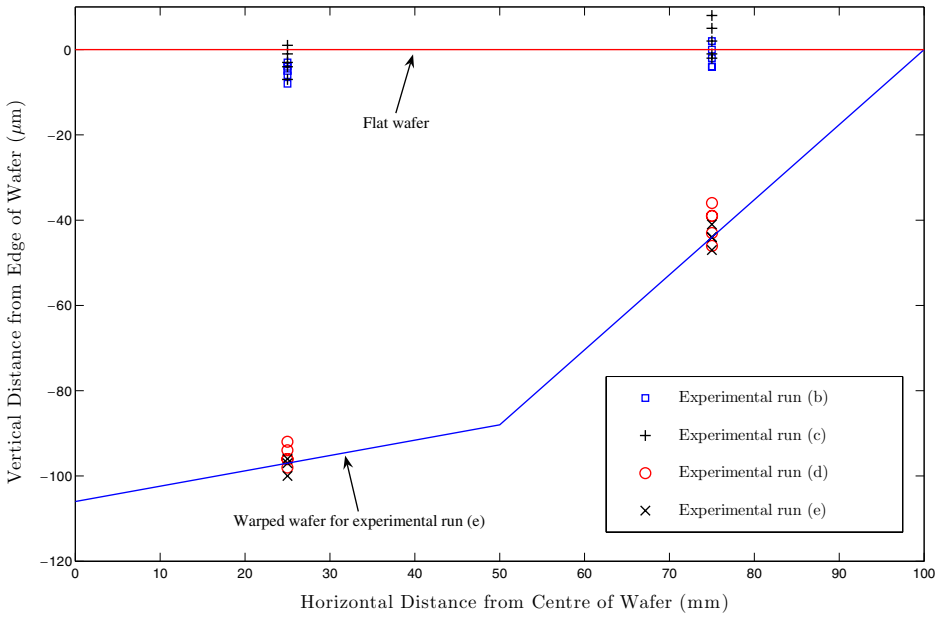

Figure 6. Estimated air gaps in each zone based on the different experimental conditions.

Table 3. Estimation of the air gap.

Experimental run	Proximity pin height, l_p (μm)	Maximum drop in $\theta_{p1}(t)$ (°C)	Maximum drop in $\theta_{p2}(t)$ (°C)	Estimated air gap: Centre zone, t_{a1} (μm)	Estimated air gap: Edge zone, t_{a2} (μm)	Deviation from flat wafer: Centre zone, $\delta_1 = t_{a1} - l_p$ (μm)	Deviation from flat wafer: Edge zone, $\delta_2 = t_{a2} - l_p$ (μm)
(b)	110	−1.70	−1.49	107	106	−3	−4
(c)	165	−1.47	−1.26	162	170	−3	+5
(d)	220	−1.64	−1.24	125	174	−95	−46
(e)	165	−1.99	−1.41	68	121	−97	−44
(f)	275	−1.60	−1.13	137	216	−138	−59

air gaps with the values of maximum drops on a Pentium® M 1033 MHz processor. However, using the method in [18], it takes about 1.5 s to identify the air gap (idgrey.m, pem.m) with the temperature trajectory of the bake plate.

A further advantage of the proposed approach includes the possibility of real-time control of the wafer temperatures. Since the degree of wafer warpage can be detected once the maximum drop point is known, the wafer temperature can also be estimated (using equations (12) and (13)) and hence controlled in real time to the desired set point. This would not be possible using the method in [18] which will only provide the warpage information at the end of the baking process.

4. Conclusions

The lithography manufacturing process will continue to be a critical area in semiconductor manufacturing that limits the performance of microelectronics. Enabling advancements by computational, control and signal processing methods is effective in reducing the enormous costs and complexities associated with the lithography sequence. In this paper, we have presented a fast and *in situ* approach to detect and estimate warpage in semiconductor substrates. Based on first principles modelling of the thermal system and by monitoring the bake-plate temperature during the baking of a wafer in microlithography, we are able to estimate the profile of the wafer from available temperature measurements in real time. Experimental results have demonstrated the feasibility and repeatability of the approach.

Appendix. Detailed derivation of the plate temperatures

This appendix shows the derivations of equations (22) and (23) from equations (18)–(21).

First, $\Theta_{w1}(s)$ and $\Theta_{w2}(s)$ in equations (20) and (21) can be expressed as

$$\Theta_{w1}(s) = \frac{C_{w1}W_2(s)}{W(s)}\theta_{w1}(0) + \frac{C_{w2}\frac{1}{R_{w1}}}{W(s)}\theta_{w2}(0) + \frac{W_2(s)\frac{1}{R_{a1}}}{W(s)}\Theta_{p1}(s) + \frac{\frac{1}{R_{w1}}\frac{1}{R_{a2}}}{W(s)}\Theta_{p2}(s), \quad \text{(A.1)}$$

$$\Theta_{w2}(s) = \frac{C_{w1}\frac{1}{R_{w1}}}{W(s)}\theta_{w1}(0) + \frac{C_{w2}W_1(s)}{W(s)}\theta_{w2}(0) + \frac{\frac{1}{R_{w1}}\frac{1}{R_{a1}}}{W(s)}\Theta_{p1}(s) + \frac{W_1(s)\frac{1}{R_{a2}}}{W(s)}\Theta_{p2}(s), \quad \text{(A.2)}$$

where

$$W_1(s) = sC_{w1} + R_1 = sC_{w1} + \frac{1}{R_{w1}} + \frac{1}{R_{wz1}} + \frac{1}{R_{a1}},$$

$$W_2(s) = sC_{w2} + R_2 = sC_{w2} + \frac{1}{R_{w1}} + \frac{1}{R_{w2}} + \frac{1}{R_{wz2}} + \frac{1}{R_{a2}},$$

$$W(s) = W_1(s)W_2(s) - \frac{1}{{R_{w1}}^2}$$

$$= C_{w1}C_{w2}s^2 + (C_{w1}R_2 + C_{w2}R_1)s + R_1R_2 - \frac{1}{R_{w1}^2}.$$

The Laplace transforms of the two proportional-integral (PI) controllers are given as

$$u_1(s) = K_{C1}\left(\frac{1}{sT_{I1}} + 1\right)(0 - \Theta_{p1}(s)), \tag{A.3}$$

$$u_2(s) = K_{C2}\left(\frac{1}{sT_{I2}} + 1\right)(0 - \Theta_{p2}(s)). \tag{A.4}$$

Substituting equations (A.1)–(A.4) into equations (18) and (19) gives

$$\Theta_{p1}(s) = \frac{G(s)}{E(s)}\theta_{w1}(0) + \frac{H(s)}{E(s)}\theta_{w2}(0), \tag{A.5}$$

$$\Theta_{p2}(s) = \frac{I(s)}{E(s)}\theta_{w1}(0) + \frac{J(s)}{E(s)}\theta_{w2}(0), \tag{A.6}$$

where

$$E(s) = C_1(s)C_2(s) - R_{pp}^2(s)D_1(s)D_2(s),$$

$$G(s) = sT_{I1}\left[C_2(s)W_2(s)\frac{C_{w1}}{R_{a1}} + R_{pp}(s)D_2(s)C_{w1}\frac{1}{R_{w1}}\frac{1}{R_{a2}}\right],$$

$$H(s) = sT_{I1}\left[C_2(s)C_{w2}\frac{1}{R_{w1}}\frac{1}{R_{a1}} + R_{pp}(s)D_2(s)W_1(s)\frac{C_{w2}}{R_{a2}}\right],$$

$$I(s) = sT_{I2}\left[C_1(s)C_{w1}\frac{1}{R_{w1}}\frac{1}{R_{a2}} + R_{pp}(s)D_1(s)W_2(s)\frac{C_{w1}}{R_{a1}}\right],$$

$$J(s) = sT_{I2}\left[C_1(s)W_1(s)\frac{C_{w2}}{R_{a2}} + R_{pp}(s)D_1(s)C_{w2}\frac{1}{R_{w1}}\frac{1}{R_{a1}}\right],$$

$$D_1(s) = W(s)sT_{I1},$$

$$D_2(s) = W(s)sT_{I2},$$

$$C_1(s) = B_1(s)sT_{I1} + W(s)K_{C1}(1 + sT_{I1}),$$

$$C_2(s) = B_2(s)sT_{I2} + W(s)K_{C2}(1 + sT_{I2}),$$

$$B_1(s) = \left(sC_{p1} + \frac{1}{R_{p1}} + \frac{1}{R_{a1}}\right)W(s) - W_2(s)\frac{1}{R_{a1}^2},$$

$$B_2(s) = \left(sC_{p2} + \frac{1}{R_{p1}} + \frac{1}{R_{p2}} + \frac{1}{R_{a2}}\right)W(s) - W_1(s)\frac{1}{R_{a2}^2},$$

$$R_{pp}(s) = \frac{1}{R_{p1}} + \frac{1}{R_{w1}R_{a1}R_{a2}W(s)}.$$

Next, we note that $E(s)$ is an eighth-order polynomial of s with the first coefficient $E_1 = \left(C_{p1}C_{p2}C_{w1}^2C_{w2}^2\right)T_{I1}T_{I2}$.

Finally, taking the inverse Laplace transform of equations (A.5) and (A.6), $\theta_{p1}(t)$ and $\theta_{p2}(t)$ can be obtained as shown in equations (22) and (23) where

$$P_{ti(s)} = \frac{P_t(s)}{s + a_i} \quad (i = 1, 2, \ldots, 8)$$

and

$$P_t(s) = \frac{E(s)}{E_1} = (s + a_1)(s + a_2)\cdots(s + a_8),$$

where $a_1, a_2, \ldots, a_8$ are the roots of

$$P_t(s) = 0.$$

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