a standard 1.2μm CMOS technology, and the parasitic capacitances have been extracted from a layout which will be used for the integration of a multilayer perceptron with on-chip learning. The size of a complete 5bit storage cell is 120μm × 69μm (120μm × 19μm for the current sources). The weighted current sources are made, respectively, of 8-, 4-, 2-, 1-unit transistors in parallel and 2-unit transistors in series for the LSB. This configuration optimises the active-to-total area ratio and consequently the current sources matching. Fig. 3 shows the transient simulation of a 4bit version of this storage cell, with $I_{LSB}$ = 1nA. The initial state of the cell is $B$ = 1100 (or $Bb$ = 0011), which represents a stored current of 12nA. The input current to the cell before conversion is $|I_w|$ = 5.1nA, which must produce the code $B$ = 0101 (or $Bb$ = 1010). This situation shows the four possible bit transitions. The input current $I_{in3}$ is the drain current of $M_C$. The complete conversion cycle can be described as follows: (3) $I_{MSB} = I_{B3}$ is larger than $I_{in3}$ and pulls $Bb_3$ high; (2) the input current to cell 2 is $I_{in2} = I_{in3}$ and $Bn_2$ is pulled down, which maintains $Bb_2$ low. The mirror output transistor $M_C$ unsaturates to the value $I_{B2}$ =4nA; (1) the input current $I_{in1}$ of cell 1 is then $I_{in3} - I_{B2}$ = 1.1nA < $I_{B1}$ = 2nA. The internal node $B_{n1}$ is therefore maintained high; (0) the input current $I_{in0}$ of cell 0 is then $I_{in3} - I_{B2}$ = 1.1nA > $I_{B0}$ = 1nA. The internal node $Bn_0$ falls slowly, pulling $Bb_0$ low. The mirror output transistor $M_C$ unsaturates to the value $I_{B2} + I_{B0}$ = 5nA, which represents the desired quantised stored value.

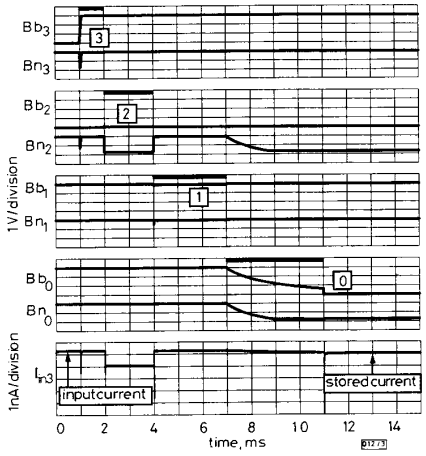


**Fig. 3** *Transient simulation of 4bit storage cell (see text)*

*Conclusion:* A simple long-term storage cell has been proposed which can be used to memorise the synaptic weights of analogue neural networks after the learning process. Its size is reasonable and it can therefore be used in practical applications where reliable long-term storage is required. A complete synapse is currently under investigation, whose short-term memory can be reset to the long-term stored value, such that the learning process can be restared from the current state of the network.

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## Low voltage CMOS four-quadrant multiplier

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*Indexing terms: CMOS integrated circuits, Multiplying circuits*

A new low voltage CMOS four-quadrant multiplier is presented. Simulation results show that, for a power supply of ±1.5V the differential linear range is over ±0.8V with the linearity error less than 2%. The total harmonic distortion is less than 1% with the input range up to ±0.6V. The simulated –3dB bandwidth of this multiplier is about 12MHz. The proposed circuit is expected to be useful in low-voltage analogue signal processing applications.

*Introduction:* The trend toward higher device densities per unit chip area requires short channel length devices and consequently lower supply voltages in the VLSI chip. Multipliers [1–4] are very important building blocks in many applications, such as adaptive filters, frequency doublers and modulators. Few four-quadrant multipliers suitable for low supply voltages are presented in the literature [5–8]. In this Letter, a low voltage CMOS four-quadrant multiplier using transistors in the triode region is presented.

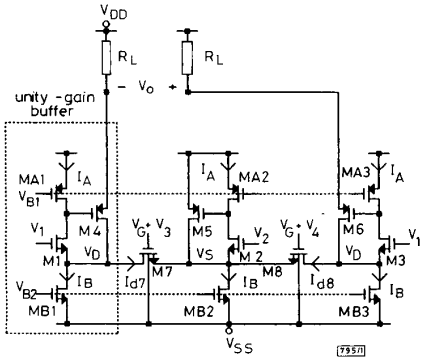


**Fig. 1** *Proposed low voltage CMOS four-quadrant multipler*

*Circuit description:* The proposed CMOS four-quadrant multiplier is shown in Fig. 1. Basically, it consists of three unity-gain buffers [9] and two *n*MOS transistors (i.e. $M_7$ and $M_8$) biased in the triode region. The drain current $I_d$ for an *n*MOS transistor in the triode region [10] can be given as

$$I_d = K\{(V_{GS} - V_{FB} - \phi_B)V_{DS} - \frac{V_{DS}^2}{2} - \frac{2\gamma}{3}[(\phi_B + V_{SB} + V_{DS})^{3/2} - (\phi_B + V_{SB})^{3/2}]\} \quad (1)$$

where $K$ ( = $\mu WC_{ox}/L$ ) is the transconductance parameter and the undefined parameters have the usual meanings. The unity-gain buffer [9] consists of the transistors $M_1$, $M_A$, $M_{A1}$, and $M_{B1}$ as shown in Fig. 1, where the negative feedback is used to keep $M_1$ in the constant current mode. $M_{Ai}$ and $M_{Bi}$ (for $i$ = 1 to 3) are biased to be two direct current sources $I_A$ and $I_B$ (if $I_B > I_A$), respectively.

Let the transconductance parameter and the threshold voltage of $M_1$ to $M_3$ be $K$ and $V_T$, respectively. The voltages $V_D$ and $V_S$ in Fig. 1 can be given as

$$V_1 - V_D = \sqrt{\frac{2I_A}{K}} + V_T \quad (2)$$

and

$$V_2 - V_S = \sqrt{\frac{2I_A}{K}} + V_T \quad (3)$$

The voltages $V_D$ and $V_S$ are the drain and source voltages for transistors $M_7$ and $M_8$, respectively. This will keep the drain-source voltages of $M_7$ and $M_8$ constant, which is proportional to the difference between $V_1$ and $V_2$. According to eqns. 2 and 3, the difference between the drain currents of $M_7$ and $M_8$ will be proportional to the product of the drain-source voltage and the difference of their gate voltages. This will result in the multiplication operation as follows. The difference between the drain currents $I_{d7}$ and $I_{d8}$ in Fig. 1 can be given as

$$I_{d7} - I_{d8} = K_7(V_3 - V_4)(V_D - V_S) = K_7(V_3 - V_4)(V_1 - V_2) \quad (4)$$

where $K_7$ is the transconductance parameter of $M_7$ and $M_8$. The output voltage $V_o$ of this multiplier can be expressed as

$$V_o = (I_{d7} - I_{d8})R_L = R_L K_7(V_3 - V_4)(V_1 - V_2) \quad (5)$$

To guarantee linear operation for this circuit, the following constraints should be satisfied:

$$\max(V_1, V_2) < V_G + \sqrt{\frac{2I_A}{K}} + V_T - V_{T7} + \min(V_3, V_4) \quad (6)$$

where $V_{T7}$ is the threshold voltage of $M_7$. Because transistors $M_7$ and $M_8$ are biased with equal source-substrate voltages, they need not be built in individual wells, which will result in a saving of chip area.

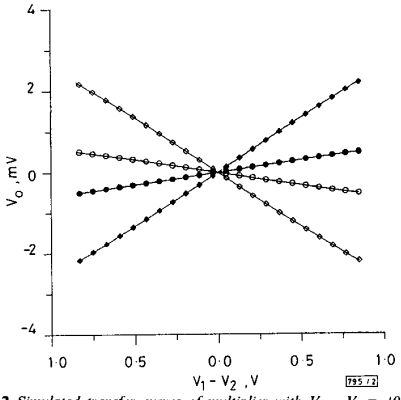


**Fig. 2** *Simulated transfer curves of multiplier with $V_3 - V_4 = \pm 0.8$ V, $\pm 0.2$ V and $R_L = 1$ kΩ*

$V_1 - V_2$ changes from −0.85 to 0.85V

DC sweep ($V_3 - V_4$)
◊ −0.8V
○ −0.2V
● 0.2V
● 0.8V

*Simulation results:* The following simulation results are obtained using SPICE together with 2μm *p*-well process parameters and MOSFETs with $V_{Tn} = 0.99$V, $V_{Tp} = -0.8$V, $K_n = 6.13\mu A/V^2$, $K_p = 25.9\mu A/V^2$, $\theta_n = 0.15V^{-1}$ and $\theta_p = 0.4V^{-1}$. The aspect ratios for all transistors in Fig. 1 are listed in Table 1. The simulation conditions are $R_L = 1$kΩ, $I_B = 24.4\mu$A, $I_A = 0.51\mu$A and the power supply is ±1.5V. The following simulations are obtained with the substrate of all *n*MOS transistors being connected to the most negative power supply. Fig. 2 shows the transfer curves of the multiplier circuit. This multiplier has a linear differential input range up to ±0.8V with a nonlinearity error of less than 2%. The total harmonic distortion of the output voltage was also evaluated and it is found to be less than 1% for $|V_1 - V_2| < 0.6$V and $V_3 - V_4 = 0.8$V. The simulated −3dB bandwidth was ~12MHz.

**Table 1**: Aspect ratios of devices in Fig. 1

| Devices | $M_1$–$M_3$ | $M_4$–$M_6$ | $M_7$–$M_8$ | $M_{A1}$–$M_{A3}$ | $M_{B1}$–$M_{B3}$ |
|---|---|---|---|---|---|
| $W$[μm]/$L$[μm] | 50/10 | 30/10 | 5/50 | 10/30 | 200/10 |

*Conclusions:* A low voltage CMOS four-quadrant multiplier is presented. SPICE simulation results show that for a power supply of ±1.5V the differential input range is over ±0.8V with a linearity error of less than 2%. The total harmonic distortion is less than 1% with input range up to ±0.6V. The simulated −3dB bandwidth is about 12MHz. This multiplier is expected to be useful in many analogue signal processing applications.


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## Fabrication of submicrometre parallelogramic-shaped gratings in $SiO_2$

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*Indexing terms: Grating filters, Reactive ion etching*

The fabrication process of submicrometre parallelogramic-shaped gratings is reported, which involves an image reversal resist process and a novel oblique reactive ion etching (RIE) configuration. A submicrometre parallelogramic grating with 40° blaze angle is fabricated using this method.

*Introduction:* Recent study has revealed that gratings with parallelogramic profiles can provide the optimum performance for waveguide grating couplers [1]. Parallelogramic gratings also have potential application in grating-coupled surface-emitting (or GSE) lasers [2]. The fabrication of gratings with rectangular or trapezoidal profiles has been widely studied, whereas the fabrication of submicrometre parallelogramic gratings still remains to be investigated. In this Letter, we report our recent experimental results on